A 48-dB Dynamic Gain Range/Stage Linear-in-dB Low Power Variable Gain Amplifier for Direct-Conversion Receivers

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***Abstract*—In this paper, a low power Variable Gain Amplifier (VGA) circuit with an approximation to exponential gain characteristic is presented. It is achieved using current mirrors to generate appropriate current signals to bias the input stage of the VGA circuit working in triode region, and the output stage working in saturation region, respectively. The VGA circuit presented herein comes with a 549 μW maximum power consumption given a 1.8 V supply, and most important of all, it has a linear-in-dB 48-dB dynamic gain range per stage. The effect of the input trasconductance and the output resistance on the linearity of gain control is also discussed. This circuit is fabricated using a 0.18 μm standard CMOS process with a core area of 0.0045 mm^2.**

***Index Terms*—VGA, AGC, pseudo exponential gain characteristic, linear-in-dB.**

I. Introduction

A Wireless sensor network (WSN) is a network comprising autonomous sensors which are spatially distributed to cooperatively monitor physical or environmental conditions, e.g., temperature, sound, vibration, pressure, movement or pollutants [1]. In WSN and other modern communication systems, the received signals often undergo a wide range of variable attenuation in different channels. To accurately retrieve information from these waveforms, an automatic gain control (AGC) circuit must be included in the receivers to adjust the amplitude such that downstream circuits can operate in the desired manner [2]. To realize constant settling time AGC circuits that are independent of the amplitude of the incoming waveforms, the variable gain amplifier (VGA) utilized to amplify the incoming waveforms is required to adjust its gain linearly in decibels with a gain controlling voltage [3].

Unfortunately, with the absence of devices providing an exponential characteristic with a standard CMOS process, it is much more difficult to design such a VGA than with a process offering bipolar transistors. To overcome this problem, pseudo-exponential functions that attempt to approximate the real exponential function have been reported [3]-[7], and circuits with a pseudo-exponential function behavior have also been proposed [4]-[7]. In this paper, a novel VGA with a gain pseudo-exponentially controlled by the gain controlling voltage is presented. With design consideration that transceivers for WSN have relatively low data rates and power consumption, this VGA requires a maximum power no more than 549 μW and occupies merely 47 μm $\times$ 96 μm on silicon.

This research was partially supported by National Science Council under grant NSC 99-2221-E-110-082-MY3, NSC 99-2220-E-110-001, NSC 99-2923-E-110-002-MY2, and EZ-10-09-44-98. It was also partially supported by Ministry of Economic Affairs, Taiwan, under grant 99-EC-17-A-01-S1-104, and 99-EC-17-A-19-S1-133.

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II. Circuit Architecture

A. Approximation of Exponential Gain Characteristics using MOS transistors

By using Taylor series expansion, the exponential function can be expanded as follows.

$$e^{ax} = 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 + \cdots + \frac{a^n}{n!}x^n \tag{1}$$

The terms in Eqn. (1) with $n > 3$ has negligible influence to the function. Thus the function can be approximated by [7]:

$$e^{ax} \approx 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 = \frac{1}{2}\cdot[1 + (1+ax)^2] \tag{2}$$

However, this approximation does not work well unless $a << 1$. Fortunately, the decibel linear range can be improved by changing the constant 1 into a decimal number 0.12 [5] and using the relation, $e^{2ax} = e^{ax}/e^{-ax}$. To allow an easier circuit realization, a decimal 0.125 is used instead, and can be realized by using a current mirror with a ratio of 1:8 with no loss of linearity. This results in the following equation:

$$e^{2ax} = \frac{e^{ax}}{e^{-ax}} \approx \frac{0.125 + (1+ax)^2}{0.125 + (1-ax)^2} \tag{3}$$

To obtain a circuit capable of carrying out a relationship dictated by Eqn. (5), a current generator is built consisting of M_{N1}, M_{N2}, M_{P1}, M_{P2}, and 4 sets of current mirrors, as shown in Fig. 2. The current paths of this circuit can be expressed with as follows.

$$I_{D,M_{N1}} = 8 \cdot I_{D,M_{N2}} = \beta \cdot (V_{control} - V_{thn})^2 \tag{4}$$

$$I_{D,M_{P1}} = 8 \cdot I_{D,M_{P2}} = \beta \cdot (V_{DD} - |V_{thp}|)^2 \tag{5}$$

From KCL, I_{C1} and I_{C2} are the sum of M_{P1}, M_{P2} and M_{N1}, M_{N2} drain currents, respectively. With some algebraic manipulation, we obtain:

$$
\begin{aligned}
I_{C1} &= [\frac{1}{8}\cdot\beta\cdot(V_{DD}-V_{control}-|V_{thp}|)^2+ \\
&\quad \beta\cdot(V_{DD}-|V_{thp}|)^2]\cdot A_{I1} \\
&= \beta\cdot(V_{DD}-V_{control}-|V_{thp}|)^2 \\
&\quad \cdot\left[\frac{1}{8}+\left(\frac{V_{DD}-|V_{thp}|}{V_{DD}-V_{control}-|V_{thp}|}\right)^2\right]\cdot A_{I1} \\
&= \beta\cdot(V_{DD}-V_{control}-|V_{thp}|)^2 \\
&\quad \cdot\left[\frac{1}{8}+\left(1-\frac{V_{control}}{V_{DD}-V_{control}-|V_{thp}|}\right)^2\right]\cdot A_{I1}
\end{aligned} \tag{6}
$$

and

$$
\begin{aligned}
I_{C2} &= [\frac{1}{8}\cdot\beta\cdot(V_{control}-V_{thn})^2+\beta\cdot(V_{DD}-V_{thn})^2]\cdot A_{I2} \\
&= \beta\cdot(V_{control}-V_{thn})^2\cdot \\
&\quad \left[\frac{1}{8}+\left(\frac{V_{DD}-V_{thn}}{V_{control}-V_{thn}}\right)^2\right]\cdot A_{I2} \\
&= \beta\cdot(V_{control}-V_{thn})^2\cdot \\
&\quad \left[\frac{1}{8}+\left(1-\frac{V_{control}-V_{DD}}{V_{control}-V_{thn}}\right)^2\right]\cdot A_{I2}
\end{aligned} \tag{7}
$$

where A_{I1} and A_{I2} are the current gains of the respective current mirrors. Now, by selecting an appropriate $V_{control}$ such that $V_{control}-V_{thn}=V_{DD}-V_{control}-|V_{thp}|$ and $V_{DD}=2\cdot V_{control}-V_{thn}+|V_{thp}|$, and assuming $V_{DD}>>V_{thn}-|V_{thp}|$, the following equation is attained by dividing I_{C2} with I_{C1}:

$$
\begin{aligned}
\frac{I_{C2}}{I_{C1}} &= \frac{\beta\cdot(V_{control}-V_{thn})^2\cdot A_{I2}}{\beta\cdot(V_{DD}-V_{control}-|V_{thp}|)^2\cdot A_{I1}}\cdot \\
&\quad \frac{\left[\frac{1}{8}+\left(1-\frac{V_{control}-V_{DD}}{V_{control}-V_{thn}}\right)^2\right]}{\left[\frac{1}{8}+\left(1-\frac{V_{control}}{V_{DD}-V_{control}-|V_{thp}|}\right)^2\right]} \\
&= \frac{A_{I2}}{A_{I1}}\cdot\frac{\left[\frac{1}{8}+\left(1-\frac{V_{control}-2\cdot V_{control}+V_{thn}-|V_{thp}|}{V_{DD}-V_{control}-|V_{thp}|}\right)^2\right]}{\left[\frac{1}{8}+\left(1-\frac{V_{control}}{V_{DD}-V_{control}-|V_{thp}|}\right)^2\right]} \\
&\approx \frac{A_{I2}}{A_{I1}}\cdot\frac{\left[0.125+\left(1-\frac{-V_{control}}{V_{DD}-V_{control}-|V_{thp}|}\right)^2\right]}{\left[0.125+\left(1-\frac{V_{control}}{V_{DD}-V_{control}-|V_{thp}|}\right)^2\right]}
\end{aligned} \tag{8}
$$

If the factor of the variation in the control voltage is assumed to be x, then

$$
V_{control}-V_{thn}>>|xV_{control}-V_{control}| \tag{9}
$$

and Eqn. (8) can be simplified as:

$$
\frac{I_{C2}}{I_{C1}} = \frac{[0.125+(1+\frac{V_{control}}{(V_{control}-V_{thn})})^2]\cdot A_{I2}}{[0.125+(1+\frac{V_{control}}{(V_{DD}-V_{control}-|V_{thp}|)})^2]\cdot A_{I1}} \tag{10}
$$

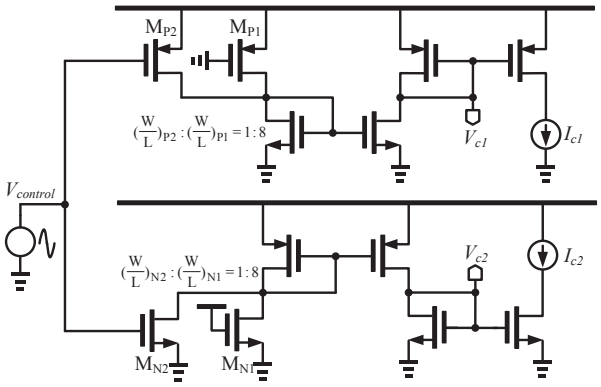

Fig. 1. I_{C1} and I_{C2} current generator.

which can be further simplified as:

$$
\frac{I_{C2}}{I_{C1}} = \frac{A_{I2}}{A_{I1}}\cdot\left[\frac{0.125+(1+ax)^2}{0.125+(1-ax)^2}\right]\approx\frac{A_{I2}}{A_{I1}}\cdot e^{ax} \tag{11}
$$

where $a=\frac{V_{control}}{V_{control}-V_{thn}}=\frac{V_{DD}-|V_{thp}|}{V_{DD}-V_{control}-|V_{thp}|}$.

Apparently, if the gain of an amplifier is a linear function of Eqn. (8), the particular amplifier will provide pseudo-exponential gain characteristics, and linear-in-dB characteristics is achieved as long as Eqn. (9) is valid.

B. Realization of a VGA Circuit with Exponential Gain Characteristics using MOS transistors

To realize an amplifier with the required pseudo-exponential gain characteristics, we will have the current mirror to act as a V-to-I circuit, which converts the control voltage $V_{control}$ into I_{C1} and I_{C2}, as shown in Fig. 2. The current will be mirrored to both Main VGA and Half Circuit, while Half Circuit will generate additional bias voltages supplied to Main VGA as functions of I_{C1} and I_{C2}. As shown in Fig. 3 and Fig. 4, I_{C2} is mirrored to M_{R1} through V_{C1}, and flows through R_1 and R_2 to generate voltages $I_{C2}\times R_1$ and $I_{C2}\times R_2$, respectively. Hence, the transconductance of M_{common}, M_{in1}, and M_{in2} becomes:

$$
\begin{aligned}
g_m &= \frac{\partial I_D}{\partial V_{gs}} = \frac{\partial\left\{\mu_p C_{ox}(\frac{W}{L})[(V_{gs}-V_{th})V_{ds}-\frac{1}{2}V_{ds}^2]\right\}}{\partial V_{gs}} \\
&= \mu_p C_{ox}(\frac{W}{L})V_{ds} = \mu_p C_{ox}(\frac{W}{L})I_{C2}R_{1,2}
\end{aligned} \tag{12}
$$

Referring to the Half Circuit shown in Fig. 3, to ensure that the drain node of M_{T1} remains constant regardless of I_{C2}, an error amplifier EA_1 is used to regulate the drain of M_{T1} to V_{Bias} by adjusting the gate of M_{T1} with V_3. EA_2 senses the drain node of M_{R1} and regulate the drain of M_{common} to be consistent by adjusting the gate of M_B with V_2. This ensures that the source and drain nodes of transistor M_{common} are regulated at V_{Bias} and $V_{Bias}-I_{C2}R_1$, respectively. Since both V_2 and V_3 are used to bias the Main VGA shown in Fig.

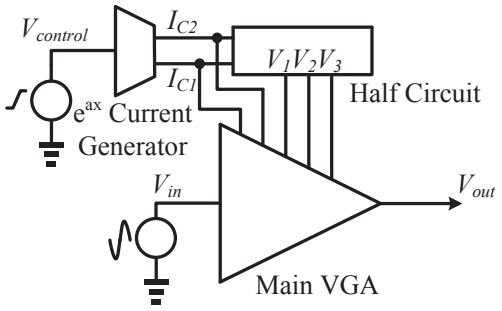

Fig. 2. The block diagram of the proposed VGA.

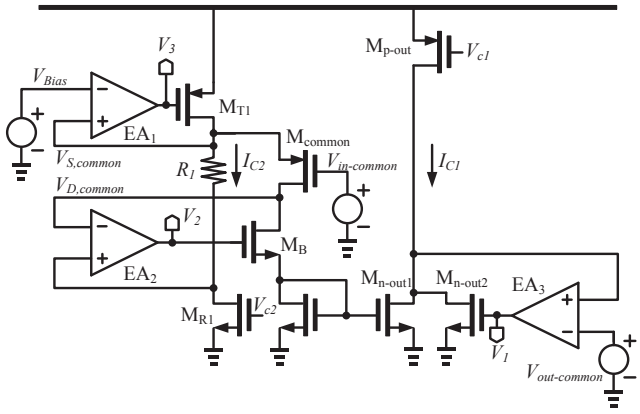

Fig. 3. The Half Circuit of the proposed VGA.

4, the input transistors M_{in1} and M_{in2} are also biased in the triode region and their transconductances will be governed by Eqn. (18).

The output resistance of an amplifier is determined by:

$$r_o = \frac{1}{\lambda I_D} = (\lambda_p I_{D,M_{p-out}} + \lambda_n I_{D,M_{n-out1}} + \lambda_n I_{D,M_{n-out2}})^{-1} \tag{13}$$

which is the shunted output resistance of $M_{p\text{-out}}$, $M_{n\text{-out1}}$ and $M_{n\text{-out2}}$. Since $I_{D,M_{p-out}} = I_{D,M_{n-out1}} + I_{D,M_{n-out2}}$ and let $I_{D,M_{p-out}} = I_{C1}$, we have:

$$r_o = \frac{1}{\lambda_p I_{C1} + \lambda_n I_{C1}} = \frac{1}{(\lambda_p + \lambda_n) I_{C1}} \tag{14}$$

By multiplying Eqn. (12) with Eqn (14), the overall gain of the main VGA becomes:

$$\begin{aligned} A_{VGA} &= \frac{\mu_p C_{ox}(\frac{W}{L}) I_{C2} R_2}{(\lambda_p + \lambda_n) I_{C1}} \\ &= \frac{\mu_p C_{ox}(\frac{W}{L}) R_2 A_{I2}}{(\lambda_p + \lambda_n) A_{I1}} \cdot \left[\frac{0.125 + (1+ax)^2}{0.125 + (1-ax)^2}\right] \approx \eta \cdot e^{ax} \end{aligned} \tag{15}$$

where $\eta = \frac{\mu_p C_{ox}(\frac{W}{L}) R_2 A_{I2}}{(\lambda_p + \lambda_n) A_{I1}}$. Current balancing is achieved using EA_3, $M_{n\text{-out1+}}$, $M_{n\text{-out2-}}$, and $M_{n\text{-out2}}$. EA_3 can be interpreted as a linear regulator, which attempts to regulate the drain nodes of $M_{p\text{-out}}$, $M_{n\text{-out1}}$ and $M_{n\text{-out2}}$ to a predefined voltage, $V_{out-common}$. As $V_{out-common}$. As EA_3 controls the gate voltage of $M_{n\text{-out1+}}$and $M_{n\text{-out2-}}$ are simultaneously

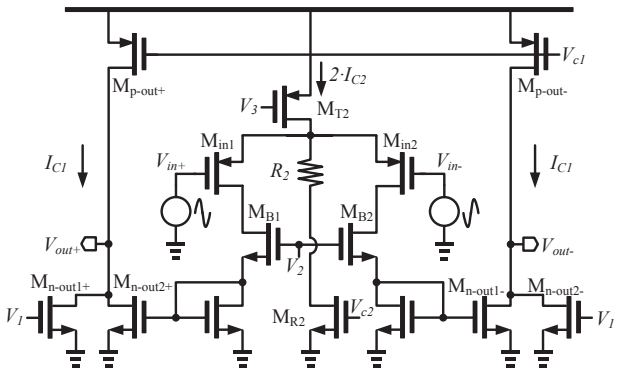

Fig. 4. The Main VGA of the proposed VGA.

controlled. Hence, the DC controlled. Hence, the DC level of the output nodes of both Main VGA and Half Circuit will remain at $V_{out-common}$, which is chosen to be ½ × V_{DD} because we need to ensure $M_{p\text{-out}}$, $M_{n\text{-out1}}$, $M_{n\text{-out2}}$, $M_{p\text{-out+}}$, $M_{n\text{-out1+}}$, $M_{n\text{-out2+}}$, $M_{p\text{-out-}}$, $M_{n\text{-out1-}}$, and $M_{n\text{-out2-}}$, all working in saturation so that the VGA operates in a manner dictated by Eqn. (15). Furthermore, the outputs of the VGA is biased at ½ × V_{DD} to attain the maximum voltage swing. However, if the input stage of the circuit cascaded to the output of the VGA requires a DC bias other than ½ × V_{DD}, $V_{out-common}$ can be preset to a corresponding value by external adjustments.

III. Measurement Results

This design has been implemented using the TSMC 0.18 μm standard CMOS process. Simulation results show that the VGA has a minimum bandwidth of 3 MHz with no RC load, and 5 kHz with 50 pF loading on both outputs, which is similar to measurement results. The measurement was conducted with Personal Computer-controlled Audio Precision Sys-2712, which has approximately 50 pF capacitive load on both probes. ABM PRT3230 was used to supply power, provide bias voltages, and generate gain control voltage. The measurement setup is shown in Fig. 5, and the measured and simulated Bode plots are given in Fig. 6 and Fig. 7, respectively. Measurement results plotted in Fig. 8 also show that $V_{control}$ is capable of adjusting forward gain from -3 dB to 45 dB, which is 12 dB narrower than the simulated result of -18 dB to 42 dB shown in Fig. 10. Nevertheless, the gain tuning range of two such cascaded VGAs is still more than enough for most wireless receivers [2].

The proposed VGAs have a simulated power consumption ranging from 433 μW to 549 μW depending on its gain. Limited by the current detector of ABM PRT3230, we can only verify that the current of this VGA is less than 1 mA, which implies the overall power consumption is less than 1.8 mW. The micrograph of this VGA is shown in Fig. 9, with a core area of 0.0045 mm^2. A tabulated comparison of this VGA along with other prior works is shown in Table I.

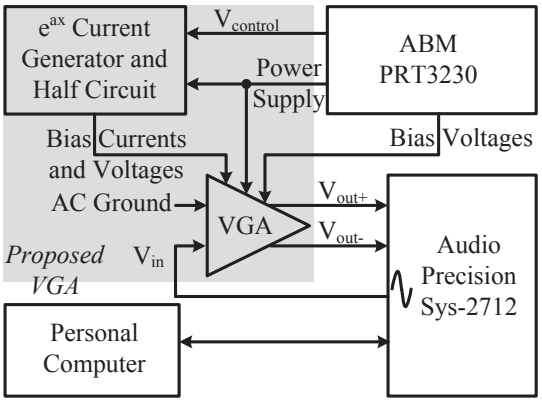

Fig. 5. The measurement setup for the proposed VGA.

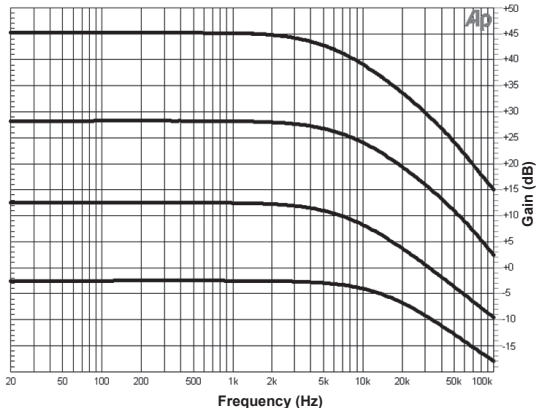

Fig. 6. The measured Bode plot with gain ranging from -3 dB to 45 dB.

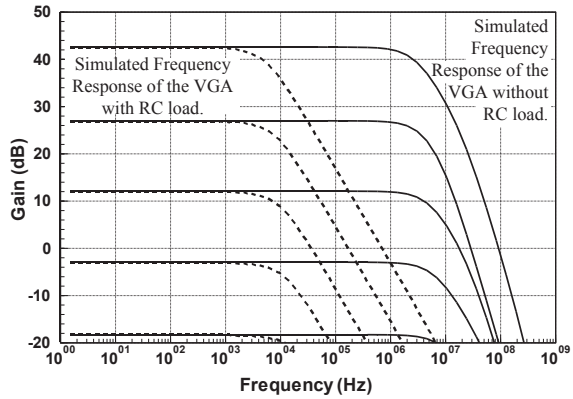

Fig. 7. The simulated Bode plot with gain ranging from -18 dB to 42 dB.

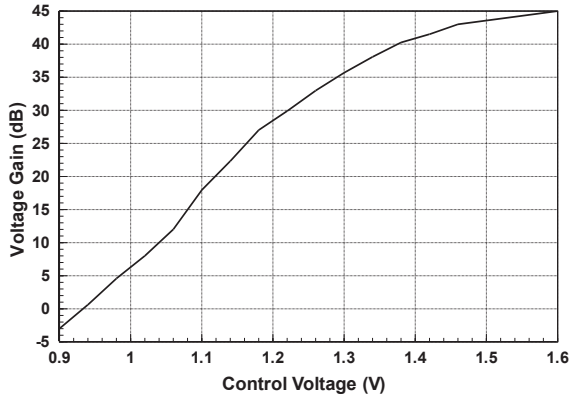

Fig. 8. The measured gain with respect to the gain control voltage, $V_{control}$.

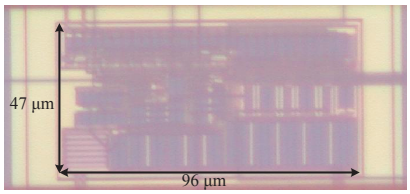

Fig. 9. Die photo of the proposed VGA.

TABLE I
SYSTEM PARAMETERS

	Proposed	[4]	[6]	[7]
Gain (dB)	-3 to 45	0 to 95	-10 to 17	-5 to 10
Stages	1	3†	2	1
Bandwidth	3 MHz Min.	32 MHz	1.25 GHz	150 MHz
Core Area (mm^2)	0.0045	0.4	0.0887	0.15
Supply voltage (V)	1.8	1.8	1.8	3.3
Power (mW)	0.433-0.549	6.48	43.2	2.5
Process (μm)	0.18	0.18	0.18	0.5
Year	2010	2006	2008	1998

†2 Variable Gain Stage + 1 Constant Gain Stage

IV. CONCLUSION

In this study, a VGA with linear-in-dB gain characteristics is presented. The approximation to exponential gain characteristic is derived, and a feasible realization is proposed. The power consumption of this VGA is below 0.549 mW, with a dynamic range of 48 dB per stage. Hence, dynamic range specifications of a wireless sensor network are easily met, making this VGA practical in many applications.

ACKNOWLEDGEMENT

This research was partially supported by the National Science Council, Taiwan under grants NSC99-2221-E-110-082-MY3, NSC99-2923-E-110-002-MY2, NSC-99- 2221-E-110-081-MY3, NSC-99-2220-E-110-001, and EZ-10-09-44-98. This research was also partially supported by the Ministry of Economic Affairs, Taiwan under grant 99-EC-17-A-01-S1-104 and 99-EC-17-A-19-S1-133. The authors would also like to acknowledge the Chip Implementation Center (CIC), Taiwan, for funding the chip fabrication cost.

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