On-Chip Process and Temperature Compensation and Self-Adjusting Slew Rate Control for Output Buffer

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***Abstract*—A novel process corner detection technique as well as process and temperature compensation method for sub-2×VDD output buffer is proposed. The threshold voltage (Vth) of PMOSs and NMOSs varying with process and temperature deviation could be detected, respectively. By adjusting output currents, the slew rate of output signal could be compensated over 117 %. The maximum data rate with compensation is 120 MHz in contrast with 95 MHz without compensation, which is measured on silicon with an equivalent probe capacitive load of 10 pF.**

***Index Terms*—Process and temperature variation, threshold voltage detection, mixed-voltage-tolerant, I/O buffer, floating N-well circuit, gate-oxide reliability**

I. Introduction

THE sensitivity of modern VLSI circuits to process, and temperature (PT) variation restricts its performance and yield, especially when the technology is evolved toward nano-scale. The performance of VLSI circuit can be interpreted as a function of PT variation, as shown in Fig. 1 [1]. In past ten years, many prior works proposed different techniques to enhanse capability against PT variation and enlarge the acceptable envelop as much as possible to increase the yield. Though the logic delay method has been widely utilized to detect PVT variation [2]-[7], it can only recognize three corners, TT, FF, and SS. Therefore, from a perspective of transistor level, a novel corner detection technique is proposed to detect all process corners, i.e., TT, FF, SS, SF, FS. That is, the process variation of PMOS and NMOS could be examined, respectively. Moreover, for the high-speed interface circuits, the specification of slew rate is varied by different communication systems. Hence, a compensation mechanism with the NMOS and PMOS threshold voltage detectors is needed to self-adjust the slew rate of output buffers, as shown in Fig. 2 (a).

II. 2×VDD Output Buffer with PT Compensation

Fig. 2 (b) shows the block diagram of the proposed system comprising of a clock generator, a NMOS threshold voltage detector, a PMOS threshold voltage detector, comparators including comparatorN and comparatorP, Digital circuits for NMOS and PMOS, and a sub-2×VDD output buffer.

A. NMOS Threshold Voltage Detector

An output signal, VN, is generated by the NMOS threshold voltage detector, as revealed in Fig. 3 (a). When reset_N is at 1.8 V and CLK is at 0 V to activate the NMOS threshold voltage detector, the voltage of net902 is discharged to 0 V.

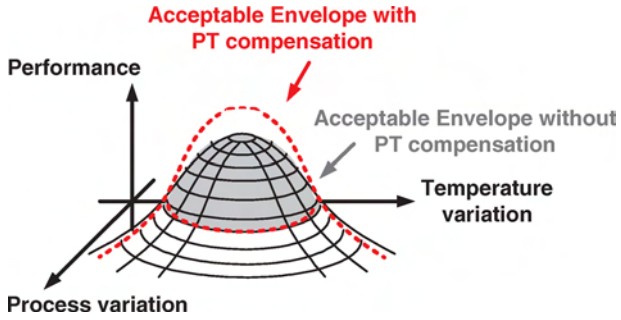

Fig. 1. Performance envelop as a function of process and temperature varitaion.

At the same time, the voltage of net901 is charged to (1.8-Vthn) V, which equals to the voltage across the capacitor C90. Then, CLK is pulled up from 0 V to 1.8 V, the voltage of net902 is pulled down to (Vthn-1.8) V, while the voltage of net901 is charged to -Vthn V. When CLK is dropped from 1.8 V to 0 V again, the voltage of net902 is pulled up to (1.8-2×Vthn) V. Hence, VN is charged to (1.8-3×Vthn) V after the first charging cycle. When the above operation is repeated in the second charging cycle, VN is pulled up to (3.5-6×Vthn) V. The function of VN can be obviously derived as

$$\mathrm{VN}(n) = (\mathrm{VDD} - 3 \times \mathrm{Vthn}) \times n \tag{1}$$

where VDD is the supply voltage, Vthn is the threshold voltage of NMOS, and n is the number of clock cycles. The voltage level of VN is rising with the cycle count. Meanwhile, the rising speed is determined by Vthn and VDD. Therefore, the clock count needed for VN to reach the reference voltage level, VREFN, will vary with different corners, as shown in Fig. 4 (a). By recognizing the clock counts, corner variations could be detected precisely.

B. PMOS Threshold Voltage Detector

The design concept is similar with that of the NMOS threshold voltage detector, as shown in Fig. 3 (b). The difference from the NMOS threshold voltage detector is that the voltage level of the output signal, VP, is falling with the clock count. Besides, the falling speed is determined by the threshold of PMOS, Vthp, and VDD. The function of VP can be obtained as follows.

$$\mathrm{VP}(m) = 3m \times \mathrm{Vthp} - (m-1) \times \mathrm{VDD} \tag{2}$$

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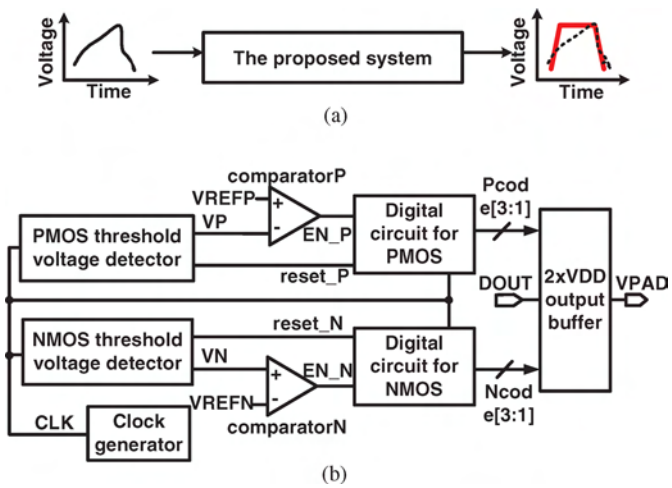

Fig. 2. (a)The slew rate is compensated through our system. (b)The block diagram of the proposed system.

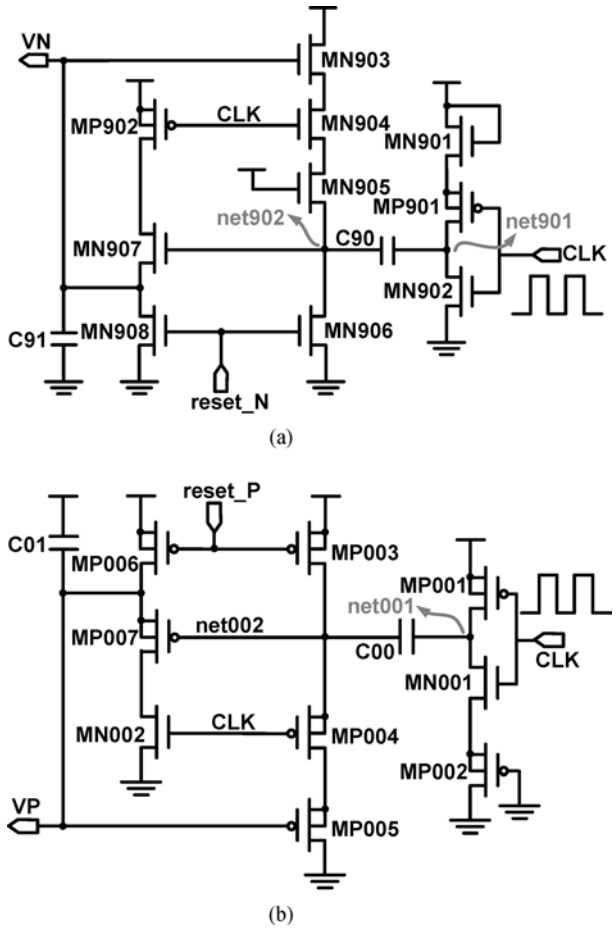

Fig. 3. (a) NMOS threshold voltage detector. (b) PMOS threshold voltage detector.

Where m is the number of clock cycle different from n in Eqn. (1). By reading the clock counts when VP meets the reference voltage VREP, different PVT corners could also be detected separately, as shown in Fig. 4 (b).

C. Digital Circuits for NMOS and PMOS

Fig. 5 illustrates the block diagram of Digital circuits for NMOS and PMOS, respectively, where a 4-bit counter, an encoder, and D flip-flops are included in one Digital circuit. According to various corners, the encoder will create a code to be latched in D flip-flops. When VP and VN reach the reference voltage VREFP and VREFN, respectively, comparators deliver, EN_P and EN_N, respectively, to latch D flip-flops. The code loaded into the D flip-flops indicates the required compensation status to control the output currents.

D. Sub-2×VDD Mixed-Voltage Tolerant Output Buffer

The sub-2×VDD mixed-voltage output buffer is composed of a Pre-driver, a Vg1 generator, a VDDIO detector, and an output stage, as shown in Fig. 6. Pre-driver is used to encode three control signals, DOUT, Pcode[3:1], and Ncode[3:1], to adjust output currents for slew rate compensation. VDDIO detector and Vg1 generator can generate appropriate gate drive voltages in different voltage modes without leakage currents and overstress problems [7].

E. Output stage

Since the supply voltage (VDD) of the core circuits is 1.8 V in 0.18 μm CMOS process, the output stage must be realized with two groups of stacked PMOS and NMOS transistors, respectively, for transmitting 2×VDD signals, as depicted in Fig. 6. PMOSs P_{1a}∼P_{1c} are connected in parallel so that the slew rate of the output signal can be improved by adjusting the currents flowing through P_{1a}∼P_{1c}. According to different process and temperature variation quantity, control signal, Pcode[3:1] and Ncode[3:1], can decide the number of turned on PMOSs of output stage. The operating mechanism of N_{1a}∼N_{1c} are same as PMOSs mentioned above. P_{1a}∼P_{1c} and N_{1a}∼N_{1c} are designed with different sizes to generate different currents, which could successfully achieve coarse and precise adjustment.

III. Measurement Results

This work is fabricated using TSMC 0.18 μm CMOS technology without thick-oxide devices. Fig. 7 shows the die photo of the proposed system, where the overall chip size is 1064 μm × 586 μm and the compensation circuit area is only 160 μm × 65 μm. Fig. 8 shows the measurement settings for process and temperature compensation. In Fig. 8 (a), the body voltage of PMOSs, Vnewll, are varied from 0.5∼0.7 V to generate different process corners. Besides, VDDIO are given 3.3/1.8/0.9 V, respectively, in different transmitting modes while VDD remains at 1.8 V. Fig. 8 (b)(c) show that our chip is heated by a thermo chamber between -40^{o}C∼100^{o}C. Referring to Fig. 9 (a)(b)(c), the maximum data rate of VPADs without compensation are measured to be 85/95/75 MHz when VDDIO is at 3.3/1.8/0.9 V given core VDD=1.8 V, respectively. The worst improvement of slew rate compensation, from 1.28 V/ns to 2.79 V/ns, occurs at [TT, 25^{o}C] corner when VDDIO=3.3 V, as shown in Fig. 8 (d). The maximum data rate is measured to 120 MHz with compensation. The performance comparison with prior works is tabulated in Table I. Our design has the

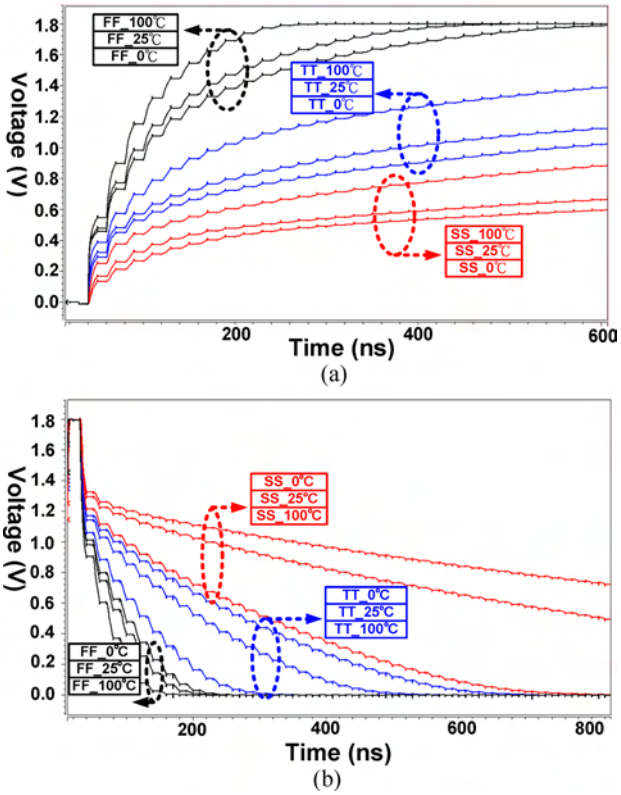

Fig. 4. Simulation waveform of (a) NMOS threshold voltage detector, (b) PMOS threshold voltage detector for different corners.

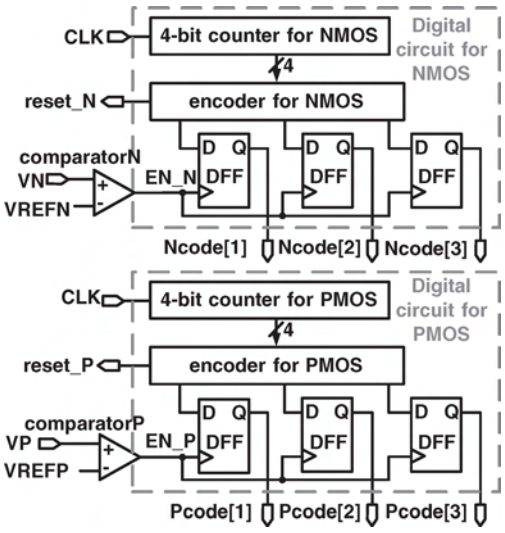

Fig. 5. Digital circuits for NMOS and PMOS.

edge of maximum slew rate improvement and the capability to detect all corners.

IV. Conclusion

An on-chip process and temperature compensation and self-adjusting slew rate control technique for output buffer is proposed in this paper. The maximum slew rate improvement can be achieved over 117 %. Besides, the effects of gate-oxide overstress and the leakage current are both eliminated.

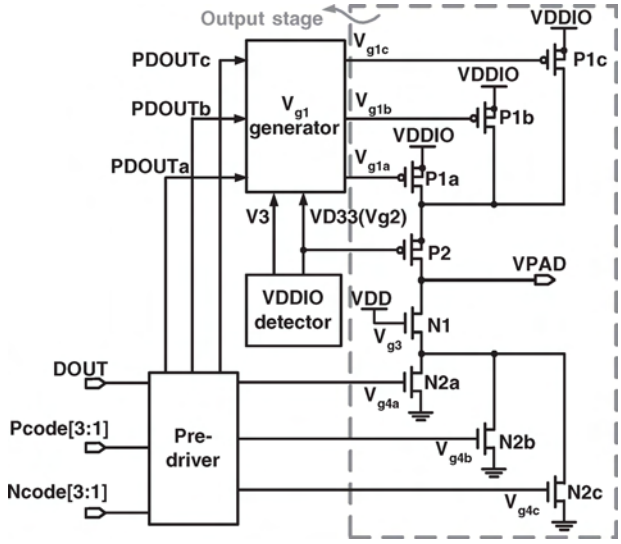

Fig. 6. Sub-2×VDD mixed-voltage tolerant output buffer.

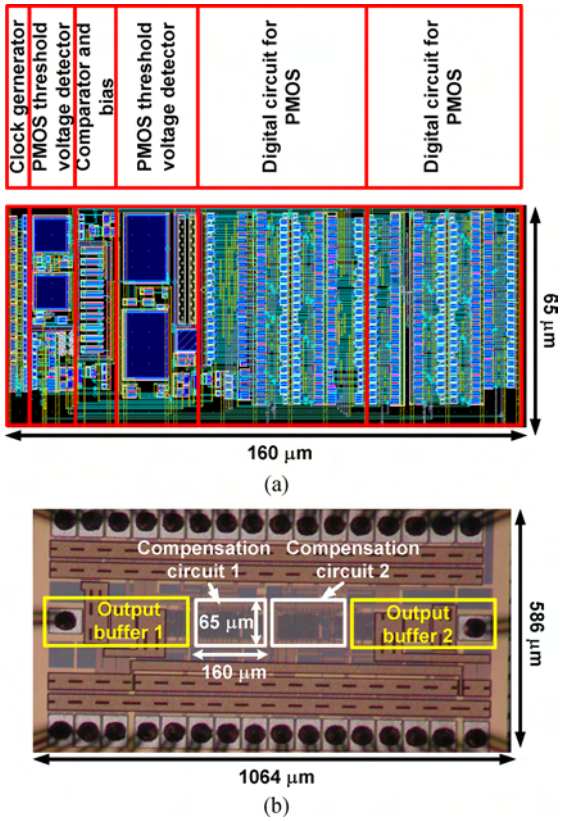

Fig. 7. (a) Layout of the compensation circuit. (b) Die photo of the proposed system.

V. Acknowledgment

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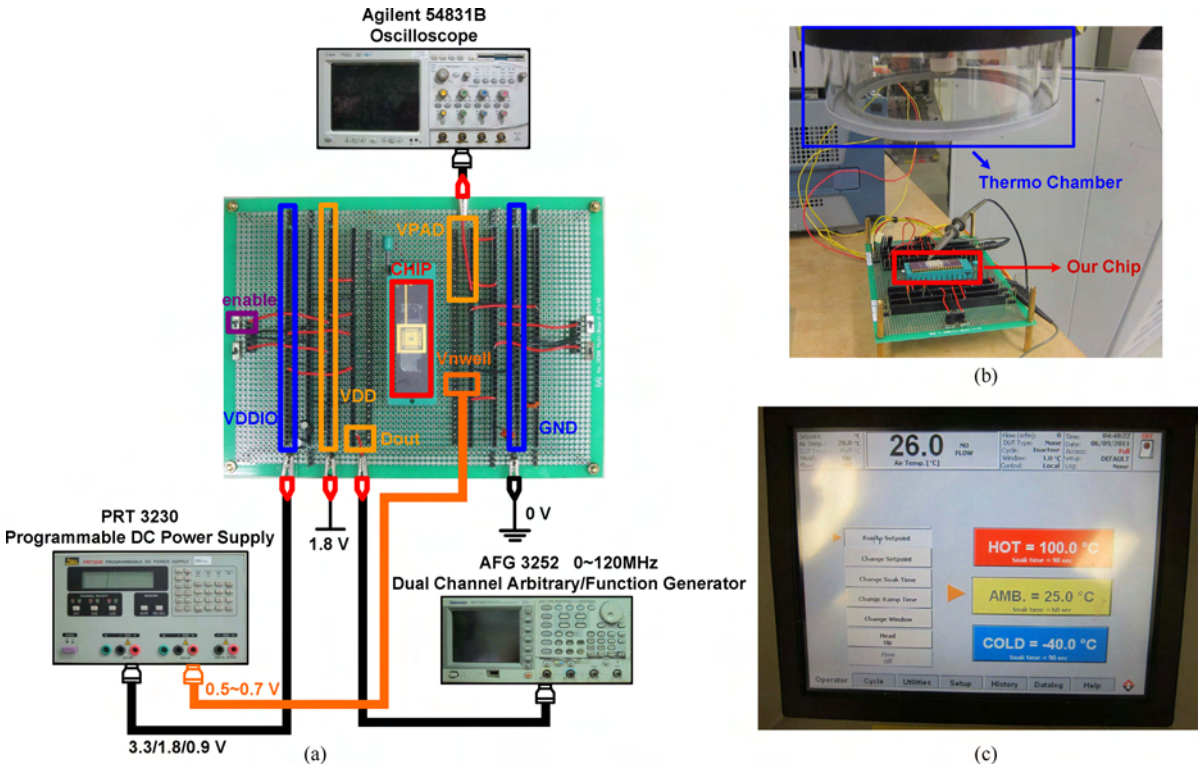

Fig. 8. The measurement settings of the proposed system. (a)In different transmitting modes when VDDIO is at 3.3/1.8/0.9 V. (b)The chip is heated and cooled down by a thermo chamber. (c)Thermo test is between -40°C∼100°C.

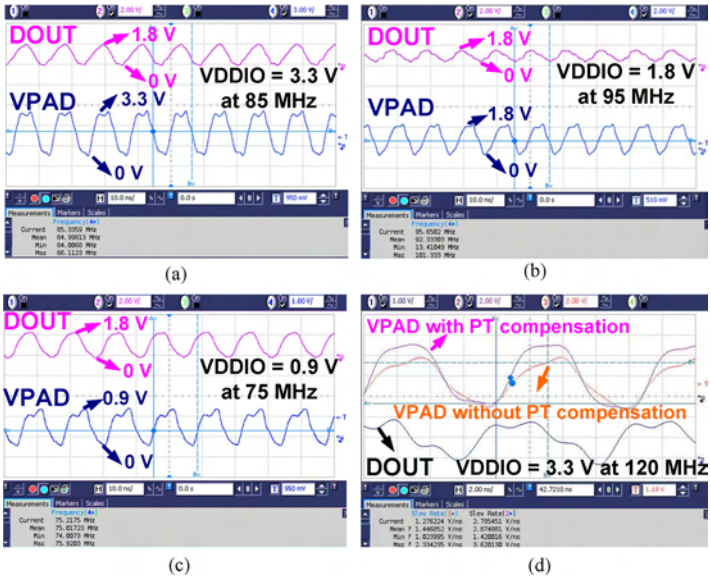

Fig. 9. The maximum data rate of VPAD when (a) VDDIO is at 3.3 V. (b) VDDIO=1.8 V. (c) VDDIO=0.9 V. (d) When VDDIO=3.3 V @120 MHz, the slew rate of VPAD can be compensated over 117 %.

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TABLE I
PERFORMANCE CAPARISON OF MIXED-VOLTAGE I/O BUFFER

	Ours	[?] *ISSCC*	[?] *JSSC*	[?] *JSSC*
Year	2010	2007	2003	2003
Process (μm)	0.18	0.18	0.35	0.18
Results	Measured	Post-sim	Measured	Measured
Slew rate (V/ns)	1.28-2.79	2.10-3.58	1.60-2.20	0.40-0.99
Process corners detected	TT, FF, SS FS, SF	TT, FF, SS	TT, FF, SS	TT, FF, SS
Power (mW)	0.427	13.7	N/A	N/A
Slew rate improvement	>117%	N/A	N/A	>32%

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