Domestic Indirect Feedback Compensation of Multiple-Stage Amplifiers for Multiple-Voltage Level-Converting Amplification

Shang-Hsien Yang and Chua-Chin Wang
Department of Electrical Engineering, National Sun Yat-Sen University
No. 70, Lienhai Rd., Kaohsiung, Taiwan
ccwang@ee.nsysu.edu.tw

***Abstract*—This investigation presents a Domestic Indirect Feedback Compensation (DIFC) operational amplifier for systems with both low voltage and high voltage circuits. The DIFC operational amplifier is capable of converting a voltage signal from a low voltage circuit and amplifying it into a large voltage signal to drive high voltage load. Since the Metal-Insulator-Metal (MIM) capacitors are not designed for high voltage applications and the feed-forward compensation causes pole-zero doublet as a result from the deviation of high voltage transistor characteristics from shuttle to shuttle, the DIFC is performed only using low voltage circuits. In other words, the feedback by connecting the output node of the operational amplifier is avoided. The proposed design is carried out using the TSMC 0.25 μm 1-poly 3-metal BCD process.**

***Index Terms*—Analog circuits, operational amplifiers, multi-stage amplifiers, frequency compensation, high voltage integrated circuits.**

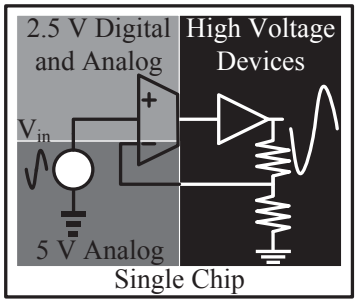

Fig. 1. An operational amplifier capable of converting an analog voltage signal from the circuits in the 5 V domain and amplifying it into a signal of large voltage swing in the high voltage domain, suitable for systems with 2.5 V digital circuits, low power analog circuits, 5 V analog circuits, and high voltage devices all in one single chip.

I. Introduction

RECENT advance in semiconductor technology allows a digital process to fabricate an integrated circuit with high voltage devices. It is achieved by adding a certain number of extra masks to existing masks needed for the fabrication of digital circuits. Such a semiconductor process, e.g., TSMC 0.25 μm 1-poly 3-metal BCD process, used for this design has a price advantage over conventional high voltage analog process. With the aid of this process and the selection over several high voltage tolerant devices, System-on-chip (SOC) of digital cell-based, low voltage analog, and high voltage driving devices is feasible.

The 0.25 μm 1-poly 3-metal BCD process used to carry out this design offers 0.25 μm transistors for digital cell-based design and low voltage analog circuits operating in 2.5 V, 0.5 μm transistors for analog circuits operating in 5 V, and power devices for high voltage applications supporting up to 60 V. Converting an analog voltage signal from the 2.5 V circuit domain and amplifying it into the 5 V circuit domain, which can be achieved with operational amplifiers designed using 0.5 μm transistors probably would not be too much a problem. However, problems arise when attempting to convert an analog voltage signal from the circuits in the 5 V domain and amplify it into a signal of large voltage swing in the high voltage domain. One major reason of the difficulty lies in the design of these operational amplifiers. First of all, the high voltage transistors offered in this process are bilateral devices. The gate to source voltage is limited to a low voltage of 5 V even when their drain to source voltage can sustain up to 60 V. For this reason, it would be meaningless to design the input stage of an operational amplifier with high voltage transistors. In fact, each high voltage transistor requires an independent isolation rings, which can be several times larger than the actual dimensions of high voltage transistors. On the other hand, all the 5 V transistors can all be fitted into a single isolation ring. Apparently, we should avoid using an excessive number of high voltage transistors, especially if their functionalities can be achieved using 5 V transistors. Thus, the stages of an operational amplifier should be divided into a 5 V voltage domain and a high voltage domain. Furthermore, the Metal-Insulator-Metal (MIM) capacitors offered in this process are not meant to sustain high voltage. This fact prevents the use of Miller capacitors which connect one of its nodes to the output of the operational amplifier working in the high voltage domain, while the other is connected to the node in the 5 V voltage domain.

To resolve this problem, the feed-forward compensation

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Prof. C.-C. Wang is with the Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan 80424. (e-mail: ccwang@ee.nsysu.edu.tw)

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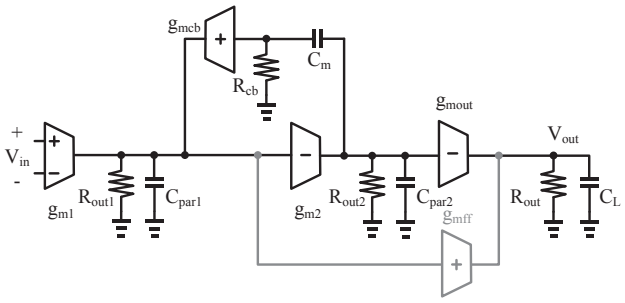

Fig. 2. The proposed DIFC topology.

schemes that do not require any Miller capacitor proposed in [1] may seem promising at first. Unfortunately, such frequency compensation schemes would require additional high voltage transistors. Furthermore, according to many prior empirical experiments, the measurement results of these high voltage transistors often deviate from the characteristic obtained through simulation. It will cause a problem to carry out pole-zero cancelation, which is the main idea of feed-forward compensation. The doublet caused by pole-zero mismatches further degrade the settling time of the operational amplifier. For the sake of robustness, such a compensation scheme should be avoided. In comparison with high voltage transistors, the characteristics of 0.5 μm transistors are found to be more consistent. Hence, reliability of the frequency compensation can be ensured if the compensation is merely carried out in the 5 V voltage domain.

In this paper, a novel frequency compensation scheme is proposed. This scheme solely performs compensation in 5 V voltage domain. The Miller capacitor, C_m, is entirely positioned in the 5 V voltage domain. Additional discussions on applying feed-forward compensation to the proposed DIFC amplifier are also taken into account. Simulation results of gain, frequency response, distortion and slew rate are reported to demonstrate the performance of this operational amplifier. Device dimensions of both 0.5 μm transistors and high voltage transistors are provided for reference.

II. Circuit Architecture

The small signal model of the proposed DIFC amplifier without the grey feed-forward amplifier is shown in Fig. 2, and the transfer function can be obtained using KCL.

$$A_v(s) = \frac{A_{DC} \cdot (1 + \frac{s}{\omega_1} + \frac{s^2}{\omega_2})}{(1 + \frac{s}{\omega_3} + \frac{s^2}{\omega_4} + \frac{s^3}{\omega_5} + \frac{s^4}{\omega_6} + \frac{s^5}{\omega_7})} \tag{1}$$

The symbols shown in (1) are defined by (2)-(9), and some of the expressions are approximated by truncating terms that are relatively much smaller than the others.

$$A_{DC} = g_{m1} g_{m2} g_{mout} R_{out1} R_{out1} R_{out} \tag{2}$$

$$\omega_1 = \frac{1}{C_m R_{out2} + R_{cb} C_m} \tag{3}$$

$$\omega_2 = \frac{1}{R_{cb} C_m^2 R_{out2}} \tag{4}$$

$$\omega_3 \approx \frac{1}{2C_m R_{out2} + C_L R_{out} + C_m g_{m2} g_{mcb} R_{out1} R_{out2} R_{cb}} \tag{5}$$

$$\omega_4 \approx \frac{1}{g_{m2} g_{mcb} R_{out1} R_{out2} R_{cb} C_m (C_L R_{out} + C_m R_{out2}^2)} \tag{6}$$

$$\omega_5 \approx \frac{1}{C_L C_m^2 g_{m2} g_{mcb} R_{out1} R_{out2}^2 R_{out} R_{cb}} \tag{7}$$

$$\omega_6 \approx \frac{1}{C_L C_m^2 R_{out2} R_{cb} R_{out} (C_{par2} R_{out2} + 2C_{par1} R_{out1})} \tag{8}$$

$$\omega_7 = \frac{1}{C_{par1} C_{par2} C_L C_m^2 R_{out1} R_{out2}^2 R_{cb} R_{out}} \tag{9}$$

and the dominant pole can be approximated to:

$$|p_{-3dB}| \approx \frac{1}{C_m g_{m2} g_{mcb} R_{out1} R_{out2} R_{cb}} \tag{10}$$

Hence, the gain-bandwidth product can be approximated by

$$\omega_t = 2\pi GBW = A_{DC} |p_{-dB}| \approx \frac{g_{m1} g_{mout} R_{out}}{C_m g_{mcb} R_{cb}} \tag{11}$$

If the grey feed-forward amplifier is taken into account, (1) becomes:

$$A_v(s) = \frac{A_{DC} \cdot (1 + \frac{s}{\omega_1} + \frac{s^2}{\omega_2} + \frac{s}{\omega_{f1}} + \frac{s^2}{\omega_{f2}}) + A_{FF}(1 + \frac{s}{\omega_{f3}})}{(1 + \frac{s}{\omega_3} + \frac{s^2}{\omega_4} + \frac{s^3}{\omega_5} + \frac{s^4}{\omega_6} + \frac{s^5}{\omega_7})} \tag{12}$$

and

$$A_{FF} = g_{m1} g_{mff} R_{out1} R_{out} \tag{13}$$

$$\omega_{f1} \approx \frac{1}{C_m R_{out2} + R_{cb} C_m} \tag{14}$$

$$\omega_{f2} \approx \frac{1}{R_{cb} C_m^2 R_{out2}} \tag{15}$$

$$\omega_{f3} \approx \frac{1}{C_m (R_{out2} + R_{cb})} \tag{16}$$

The denominators of (1) and (12) are the same, except the fact that C_{par1} will be slightly increased. The added terms of the numerator in (12) is composed of the additional DC gain contributed by (13) and the zeros contributed by (14), (15), and (16). As will be revealed later, the addition of the feed-forward stage does not affect R_{out}. The gain-bandwidth product can be doubled, while still maintaining the same phase margin of 85 degrees. However, the addition of the g_{mff} is not always beneficial. This will be addressed later. A complete list of system parameters are tabulated below.

As shown in Fig. 3, the proposed DIFC amplifier consists of two 5 V stages and a high voltage stage. The first stage, g_{m1}, is

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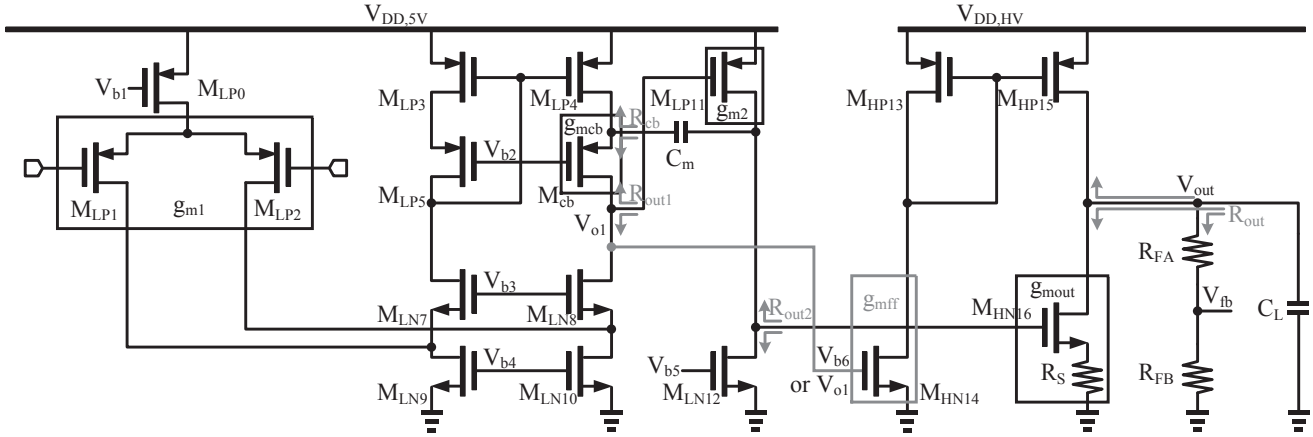

Fig. 3. The proposed DIFC operational amplifier.

TABLE I
SYSTEM PARAMETERS

g_{m1}	2.15 μA/V	R_{out1}	565 MΩ
g_{m2}	19.03 μA/V	R_{out2}	2.25 MΩ
g_{mout}	457.7 μA/V	R_{out}	240 kΩ
g_{mcb}	2.56 μA/V	R_{cb}	1.09 MΩ
g_{mff}	501 μA/V	C_m	577 fF

realized using a classical folded cascode differential amplifier, consisting of 0.5 μm transistors M_{LP1} to M_{LN10}. The output resistance, R_{out1} is made large to produce a high RC time constant. 0.5 μm transistors M_{LP11} and M_{LN12} form g_{m2}, i. e., a common source amplifier used to provide large DC gain and multiply the Miller capacitor, C_m. The capacitor connects to the output of the common source amplifier the source of M_{cb} to avoid the RHP zero. This forms the domestic indirect feedback path. M_{cb} serves as a current buffer, with a transconductance of g_{mcb}, which also prevents the high frequency shorting effect of the output terminals of the folded cascode differential amplifier and the common source amplifier.

The high voltage part of this operational amplifier has 2 high voltage N-type transistors, M_{HP14}, M_{HP16} (NLD60G5 1 μm transistor in 0.25 μm BCD process), and 2 P-type transistors, M_{HP13}, M_{HP15} (PA60G5 0.8 μm transistor in TSMC 0.25 μm BCD process). Depending on configuration, the gate of M_{HN14} is either connected to the output terminal of the folded cascode differential amplifier, V_{o1}, or to a bias voltage V_{b6}. If it is connected to V_{b6}, it will provide a DC bias current to M_{HP13}, and mirrored to M_{HP15}. M_{HN16} serves as g_{mout}, which is the third stage of the operational amplifier, and uses M_{HP15} as an active load. The output resistance of the third common source stage is kept small to prevent loading effect of the operational amplifier when driving resistors. Furthermore, an external source degeneration is added to M_{HN16} to adjust g_{mout} corresponding to any possible process variation. Feedback resistors R_{FA} and R_{FB} with values of 220.1 kΩ and 19.9 kΩ are selected to reduce the quiescent current consumption caused by the DC path these resistors introduced. The output resistance of the DIFC operational amplifier, R_{out} is the shunt resistance of R_{FA} + R_{FB} with r_{oHN16} and r_{oHP15}. By connecting the gate of M_{HN14} to V_{o1}, the feed-forward stage, g_{mff}, is realized. Since its transconductance is mirrored to the output through current mirror formed by M_{HP13} and M_{HP15}, R_{out} will not be affected. However, due to the uncertainty in transconductance of high voltage transistors, implementing the feed-forward stage might result in undesired pole-zero doublets, prolonging settling time of the operational amplifier. It is clearly evident by inspecting (12), (13), and (16). If the zero dominated by g_{mff} if shifted to high frequency, the stability of the operational amplifier may possibly be jeopardized. Similarly to other multi-stage operational amplifiers [2][3], the slew rate of this amplifier is constrained by the slowest stage. Generally, the slew rate can be estimated with:

$$SR = min(\frac{I_{D1}}{C_m}, \frac{I_{Dout}}{C_L}) \tag{17}$$

where I_{D1} and I_{Dout} represent the currents of the folded cascode differential amplifier and the output stage, respectively. Apparently, (17) is dependent of the capacitive load driven by the operational amplifier.

The device parameters used in this operational amplifier are shown in Table II.

TABLE II
DEVICE PARAMETERS

M_{LP0}	0.7 μm / 1 μm	M_{LP11}	1.65 μm / 0.5 μm
M_{LP1}	1 μm / 1 μm	M_{LN12}	0.6 μm / 0.5 μm
M_{LP2}	1 μm/ 1 μm	M_{HP13}	70 μm / 0.8 μm
M_{LP3}	0.6 μm / 2.4 μm	M_{HN14}	8 μm / 3 μm
M_{LP4}	0.6 μm / 2.4 μm	M_{HP15}	70 μm / 0.8 μm
M_{LP5}	8 μm / 0.5 μm	M_{HN16}	4.4 μm / 1 μm
M_{cb}	8 μm / 0.5 μm	C_m	577 fF
M_{LN7}	0.6 μm / 1.5 μm	R_S	900 Ω
M_{LN8}	0.6 μm / 1.5 μm	R_{FA}	220.1 kΩ
M_{LN9}	0.73 μm / 1.5 μm	R_{FB}	19.9 kΩ
M_{LN10}	0.73 μm / 1.5 μm	C_L	10 pF

III. SIMULATION RESULTS

This design is carried out using TSMC 0.25 μm 1-poly 3-metal BCD process. It consumes 15 μW from the 5 V supply and 127.7 mW from the 60 V supply. The simulation result

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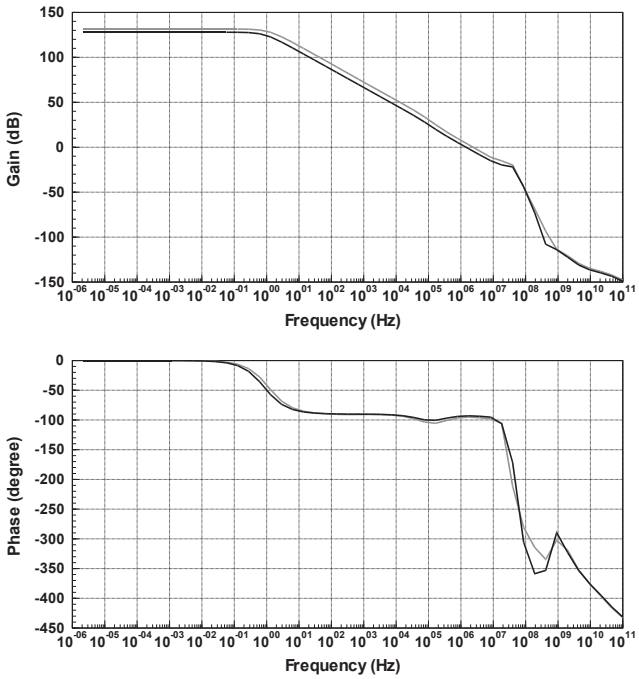

Fig. 4. The Bode plot of proposed operational amplifier with feed-forward stage (gray) and without (black).

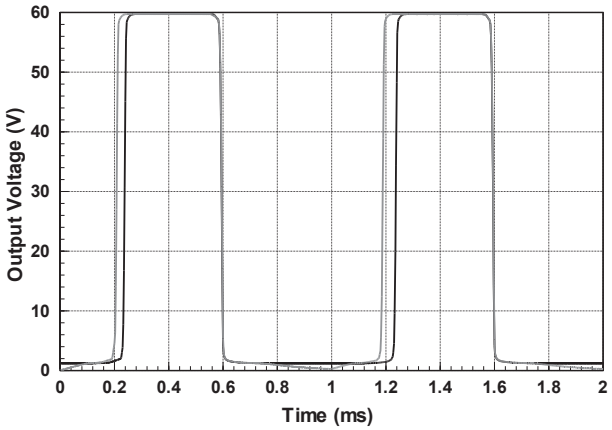

Fig. 5. The slew rate of proposed operational amplifier with feed-forward stage (gray) and without (black).

in Fig. 4 suggests that the gain-bandwidth of this operational amplifier is 2.6 MHz and 1.3 MHz with or without the feed-forward stage, respectively. Both configurations have a phase margin of 85 degrees. DC gains are 133 dB with the feed-forward stage and 128 dB without the feed-forward stage, respectively. As shown in Fig. 5, the slew rate is 3.6 V/μs, but it will require an additional delay of 48 μs for the output stage to charge the capacitive load. The feed-forward stage has minor significance discharging the capacitive load. By performing Discrete Fourier Transform on the output waveform of the operational amplifier, we can assume that the distortion caused by this operational amplifier is negligible.

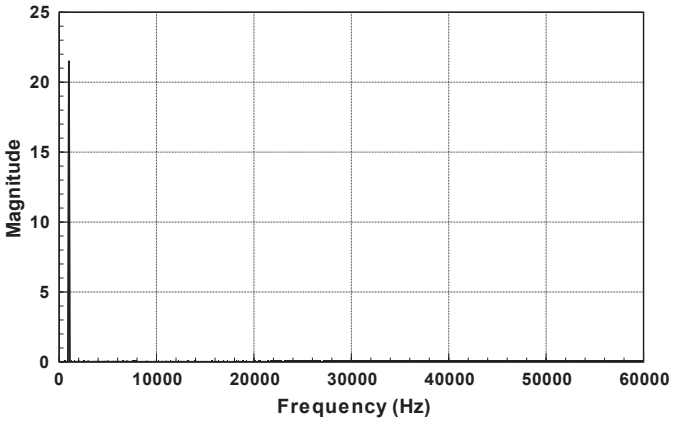

Fig. 6. The Discrete Fourier Transform of a 10 mHz sine wave output with a 50 V voltage swing.

TABLE III
SYSTEM PARAMETERS

C_L	10 pF	A_{DC}	133 / 128 dB
GBW	2.6 / 1.3 MHz	PM	85 ^{o}
Power	15 μW + 127.7 mW	GM	24 dB
V_{DD}	5V, 60V	SR	3.6 V/μs

IV. CONCLUSION

In this work, we have presented a novel multiple-stage operational amplifier dedicated to multiple-level level-converting amplification. It has been shown that the domestic indirect feedback compensation can avoid connecting a MIM capacitor terminal to couple a high voltage node, while still maintaining acceptable performance in gain, phase margin, slew rate, and power consumption.

ACKNOWLEDGEMENT

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