A High Speed Transceiver Front-end Design with Fault Detection for FlexRay-based Automotive Communication Systems

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***Abstract*—This paper presents a high speed transceiver design with fault detection circuit compliant with FlexRay standards V2.1. An LVDS-like transmitter is utilized to drive the twisted pair of the bus. A current detector is included in the transceiver to detect the operating current so as to prevent over-current hazard. By contrast, a 3-comparator scheme is used to carry out the required bit-slicing and state recognition in the receiver of the bus. A bus line short-circuit detector is also included in the proposed receiver design.**

***Keywords*—FlexRay, transceiver, automobile electronics, in-car networking, failure detection.**

I. Introduction

Car electronics has been deemed as the 4th "C" right after the Computer, Communication and Consumer electronics. The car electronics include power train, chassis safety, peripheral electronics control system, telematics communication system, in-vehicle networking, etc. Many novel electronic devices have been introduced and installed in recently publicized cars, e.g., car TVs. Therefore, an in-vehicle network has been proposed to control and supervise all of the automobile electronics. Prior in-vehicle networks were mainly composed of CAN (controller area network) or LIN (Local Interconnect Network) which emphasized safety and reliability. However, the limited 1 Mbps bandwidth is not sufficient for rapid growth of the data/signal required by in-vehicle networking. By contrast, the MOST (Media Oriented Systems Transport) network provided a very efficient mechanism for transporting high volumes of media information, but lack of control capability.

FlexRay V2.1 is the latest communication protocol [1] proposed by several automobile power houses, including BMW, Daimler-Chrysler, General Motors, Freescale, Philips, Robert Bosch, Volkswagen, etc, in 2005. It is designed to provide message and data exchange among electronic devices installed in a vehicle. FlexRay will not replace the existing network. By contrast, it can integrate and co-exist with existing network systems, including CAN, LIN, MOST and J1850 protocol, etc. FlexRay requires 10 Mbps data rate in either one of the two channel of an ECU (electronic control unit) [2]. If a single channel is used alone, the speed of the total data rate is expected to be 20 Mbps. Therefore, even the video signals, multimedia and control signals can communicate via the FlexRay network in such a high data rate. The ultimate goal is that the automobile is X-by-wire (X = steer, break, accelerate, A/V, safety, etc.). Table I shows the comparison between FlexRay and prior CAN systems. Fig. 1 shows that the explosive view of a FlexRay network in a vehicle.

TABLE I
Comparison between FlexRay and CAN system

	CAN	FlexRay
Bit rate	1 Mbps	10 Mbps
Channel	1 channel	2/1 channel (optional)
Network topology	Bus type	Mix. of bus and star type
Communication	Event triggered	Time + Event triggered
Oscillator	Ceramic/Crystal	Crystal oscillator
Network management	Software	Hardware
Network synchronization	Sync segment	Rate compensation

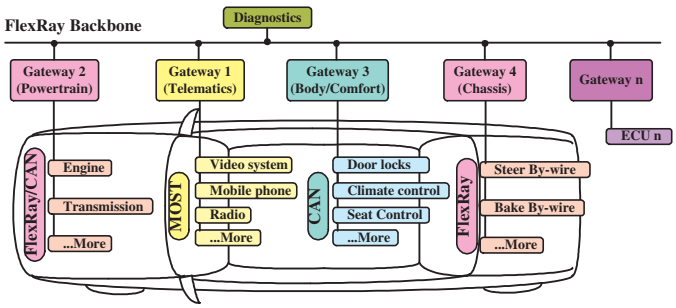

Fig. 1. Explosive view of a FlexRay network

II. Transceiver Design for FlexRay System

Fig. 2 shows the block diagram of ECU nodes in a FlexRay system. The component of each node contains a host microcontroller (μC), a communication controller (CC), a bus guardian (BG) and two bus drivers (BD). Traditionally, the transceiver in the bus driver should be implemented by a high-voltage silicon process [4]. However, we propose an LVDS-like Tx/Rx design which can be implemented by a typical 0.18 μm mixed-signal CMOS process. Hence, the proposed design can be integrated with other digital blocks easily besides cost down.

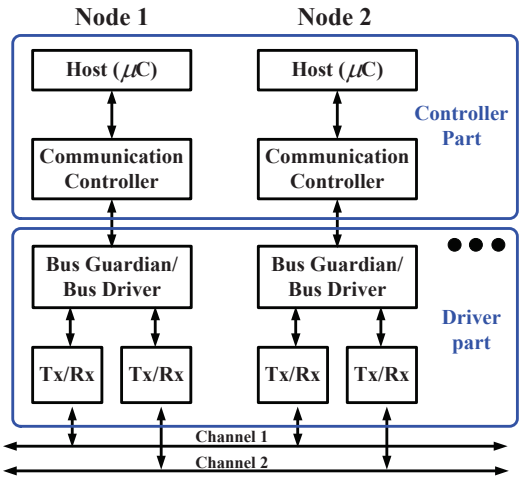

Fig. 2. ECU node on the FlexRay bus

According to the FlexRay physical layer standards [2], two signals of the bus driver, denoted as BP (Bus Plus) and BM (Bus Minus) are carried over the bus. BP and BM in fact are a pair of differential signals which can reduce the noise on a connection by rejecting common-mode interference and ground offsets. The timing and amplitude characteristics of BP and BM required by the FlexRay standards are shown in Fig. 3.

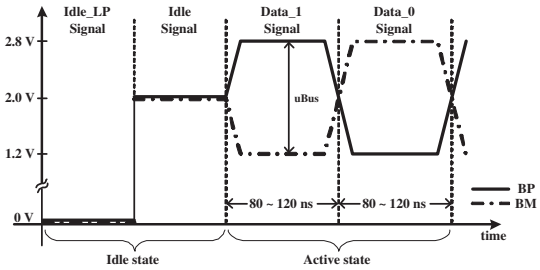

Fig. 3. The characteristics of BP and BM.

The block diagram of the proposed design is shown in Fig. 4, including a transmitter circuit, Tx, a receiver circuit, Rx, and a failure detector circuit. Data0_C, Data1_C, Idle_C, and Idle_LP_C are one-hot encoded control signals for Tx to transmit the data and the state. On the other hand, Rdata and Ridle are signals generated by the Rx after the received differential signals are recovered and decoded. O1, O2, and O3 are the failure signals which depends on different short circuit situations. The functions associated with those signals and the differential bus signals are summarized in Table II.

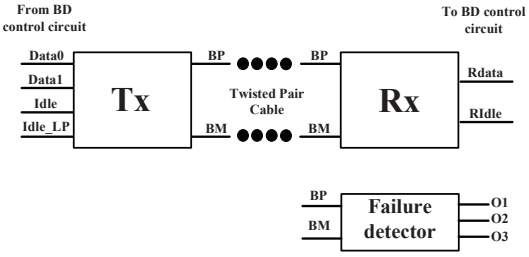

Fig. 4. The block diagram of proposed design.

TABLE II
Functions of the control signals, BP, and BM.

Control signal of transmitter	Differential signal of BP	Differential signal of BM
Data0	Low	High
Data1	High	Low
Idle	Idle_bias[1]	Idle_bias
Idle_LP	Idle_LP_bias[2]	Idle_LP_bias

Differential signal on the bus	Rdata	Ridle
Data0	Low	Low
Data1	High	Low
Idle	High	High
Idle_LP	High	High

([1])Idle_bias = 2 V
([2])Idle_LP_bias $\approx$ 0 V

A. Design of the transmitter

There are a total of four types of "Signals" in FlexRay systems, which are Data_1 Signal and Data_0 Signal in the Active State, and Idle_LP Signal, Idle Signal in the Idle State. We utilize an LVDS-like transmitter design as show in Fig. 5. Data0_C, Data1_C, Idle_C and Idle_LP_C are control signals fed into the bus driver. Data0_C and Data1_C are a pair of digital differential signals generated by Communication Controller (CC) to notify the bit to be transmitted over the bus. Idle_C and Idle_LP_C are a pair of idle signals. When the Idle_C is asserted, BP and BM must be locked on the same Vref, which is 2 V in this work. By contrast, as soon as the Idle_LP_C is asserted, indicating that the low power mode is chosen, Both BP and BM are pulled down to GND. Notably, Vdd33V denotes that the supply voltage is 3.3 V. EN and EnB are an enable and a disable signals, respectively, generated by Idle_C and Idle_LP_C to select the gate drives of M101, M102, M103, and M104.For instance, if Data1_C = 1, Data0_C = 0, Idle_C = Idle_LP_C = 0, then En = 0 and EnB = 1, such that M103 and M102 are both on, which in turn pull down BM and pull up BP to generate Data_1 signal. That is, a "1" is transmitted. Notably, the resistor, RC, and comparator,

CMP, are used to detect the operating current (tail current) of the proposed transmitter. When the operating current over a pre-defined current, the comparator output signal, Resout, will pull up to a high logic level to notify the microcontroller.

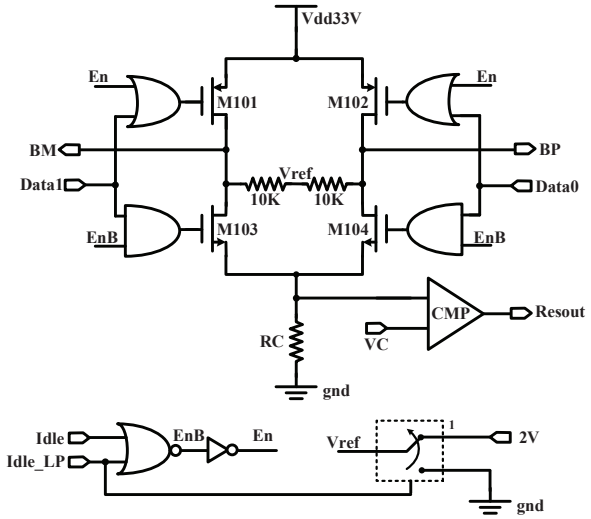

Fig. 5. The schematic of the transmitter.

B. Design of the Receiver

Apart from receiver circuits' design of traditional buses, the receiver for FlexRay systems must recognize the Idle State besides slicing the received bits. Therefore, we propose a 3-comparator scheme to achieve the required functions. The Comparator0 is used to determine if Data_0 or Data_1 is in the Active state. The Comparator1 and Comparator2 are used to detect whether the input signals on the bus is in the Idle State or not. Fig. 6 shows the schematic of the proposed receiver.

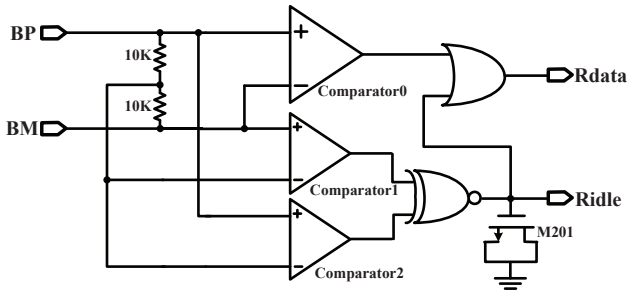

Fig. 6. The schematic of the receiver.

A fault situation which can easily occur in communication networks is the bus line short circuit (SC) [5]. A SC failure detector is included in the receiver design and illustrated in Fig. 7. The MOS string, ME1 to ME4, is used to generate the reference voltages, Vref1 and Vref2, which are close to Vdd33 ($\sim$2.7 V) and GND ($\sim$0.7 V), respectively. The comparators CMP1 and CMP4 are used to detect if the bus is short to Vdd33, while the comparators CMP2 and CMP3 are used to detect if the bus is short to GND. O1 and O3 are represented in BP and BM short to Vdd33, respectively. O2 is represented in BP and BM short to GND. The XOR gate is used to prevent the error detection in Idle_LP state.

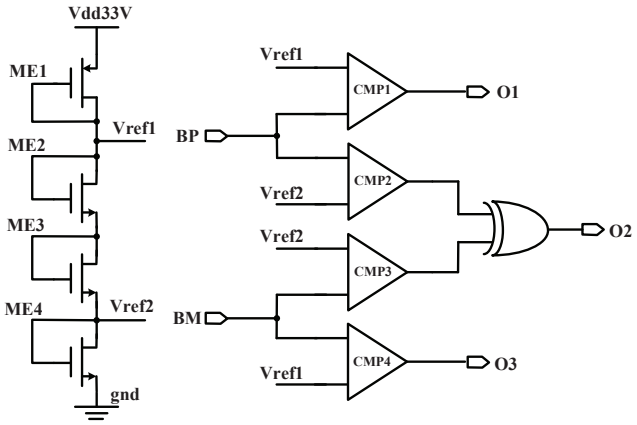

Fig. 7. The schematic of the failure detector.

III. Simulation and Implementation

The proposed design is carried out by a typical 0.18 μm single-poly six-metal CMOS technology. Verified by all-PVT-corner post-layout simulations, the throughput of the transmitter and the data rate of the receiver can reach 100 Mbps in a single channel. Fig. 8 shows the layout view of the proposed transceiver design. The worst case simulation waveform given the data rate is 100 Mbps between the output of the transmitter and the output of the receiver are shown in Fig. 9 and Fig. 10, respectively. The behavior model under short circuit failure is tested. An arbitrarily sequence of short circuits is applied to BP and BM nodes and the simulation results are shown in Fig. 11. SC to ground (GND) forces the short circuited bus voltage to ground, while SC to Vdd33 forces the short circuited bus line voltage to Vdd33. In differential buses, SC between bus lines (BP and BM) are catastrophic. Data can not be correctly represented in all short circuit cases. Table III and IV show the comparison between FlexRay specification and our design.

IV. Conclusion

In this paper, we propose a transceiver design including failure detection circuit, which can be used in a FlexRay-based automotive system. The proposed design is implemented by a typical 0.18 μm mixed-signal CMOS process such that it can easily be integrated in an ECU without using any high voltage process.

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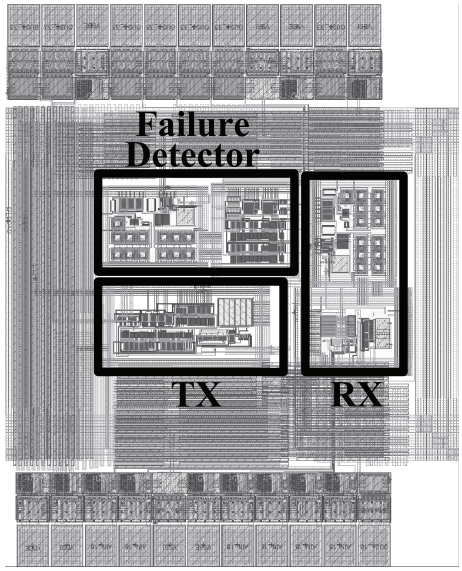

Fig. 8. Layout view of the proposed transceiver.

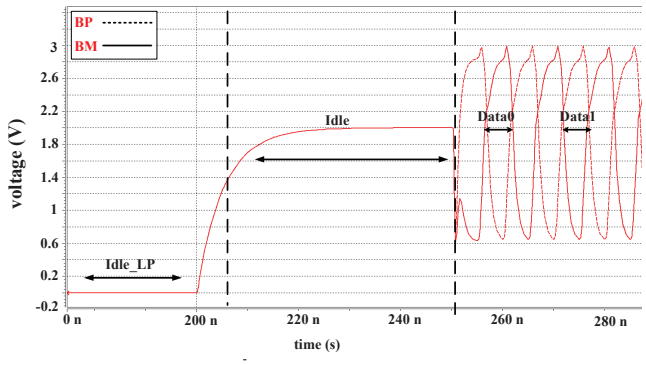

Fig. 9. Post-layout simulation of Tx.

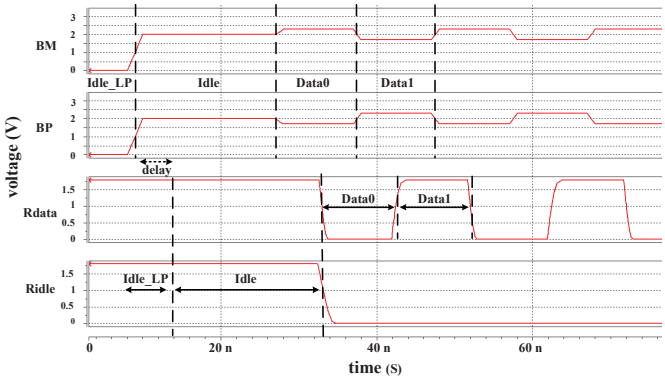

Fig. 10. Post-layout simulation of Rx.

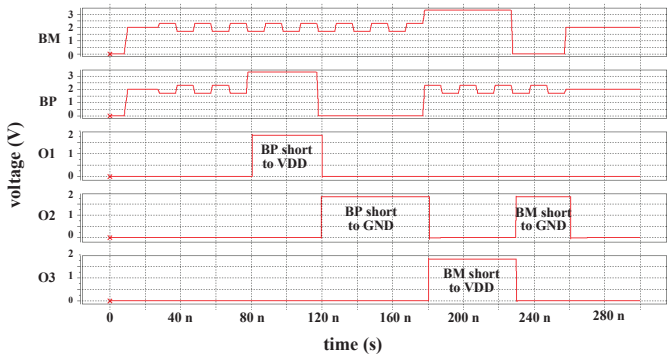

Fig. 11. Post-layout simulation of failure detector.

TABLE III
COMPARISON OF FLEXRAY STANDARDS AND THE PROPOSED TX

FlexRay Tx Specification		Simulation Result
Differential voltage	> 1.2 V	> 2.1 V
Bias of Idle_LP	0∼30 mV	~ 0 V
Slew rate	< 100 ns	< 1.2 ns
Delay time	5∼25 ns	< 6 ns
Throughput	10 Mbps	> 100 Mbps

(Note: The load of the twisted pari = $40\Omega \times 100pF$)

TABLE IV
COMPARISON OF FLEXRAY STANDARDS AND THE PROPOSED RX

FlexRay Rx Specification		Simulation Result
Receiver delay	100 ns	< 7 ns
Idle reaction time	50∼400 ns	< 6 ns
Active reaction time	100∼450 ns	< 6 ns
Data Rate	10 Mbps	> 100 Mbps

(Note: The simulation reaction time not include logic delay in BD)

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