A PCI166-compatible 3xVDD-Tolerant Mixed-Voltage I/O Buffer

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***Abstract*—A PCI166-compatible 3×VDD mixed-voltage I/O buffer with ESD protection consideration is proposed. By using a compact Dynamic gate bias generator to provide appropriate gate drive voltages for the output stage, the I/O buffer can transmit sub-3×VDD voltage level signal without gate-oxide overstress hazard. Besides, the leakage current is eliminated by adopting a Floating N-well circuit. The maximum data rate is simulated to be 166/166/166/100/80 MHz when VDDIO is 5.0/3.3/1.8/1.2/0.9 V, respectively, with an equivalent probe capacitive load of 10 pF.**

***Index Terms*—mixed-voltage-tolerant, I/O buffer, floating N-well circuit, gate-oxide reliability**

I. Introduction

With the fast development of CMOS technology, the supply voltage of integrated circuits (IC) is drastically scaled down to reduce power consumption [1]. When chips using different processes and supply voltages are integrated in a PCB-based system, such as in a PCI interface, conventional I/O buffers are not adequate to communicate due to the problems of gate-oxide reliability, hot carrier degradation, and the undesired leakage current path [2]. In past years, many mixed-voltage I/O buffers were reported to deal with the chip interface problems of different voltage levels [1]−[3]. However, most of them can only transmit and receive the signal with the voltage from VDD to 2×VDD [1]−[3]. The compatibility with more advanced processes has been ignored. Therefore, a wide range I/O buffer able to simultaneously transmit and receive signal from $\frac{1}{2}$×VDD to sub-3×VDD is deemed as a total solution for these scenarios. Although [5] can achieve the same voltage tolerance capability, the speed is too slow. Therefore, another goal of this work is focused on the speed enhancement. Comparing with the above papers, a more compact structure of the Dynamic gate bias generator is proposed to facilitate a higher data rate in this paper.

To communicate the signal at sub-3×VDD, triple stacked transistors are used in the output stage to avoid the gate-oxide overstress. Notably, traditional gate-tracking circuit and floating N-well circuit can not be used directly due to the high voltage signal which is very close to 3×VDD [2]. A protection voltage equal to VDDH−VDD (3.2 V) is required to ensure the gate-oxide reliability. The NMOS clamping technique without any power-consuming DC current path is employed to generate this protection voltage. Besides, the current drive capability with ESD protection is also proposed in this work.

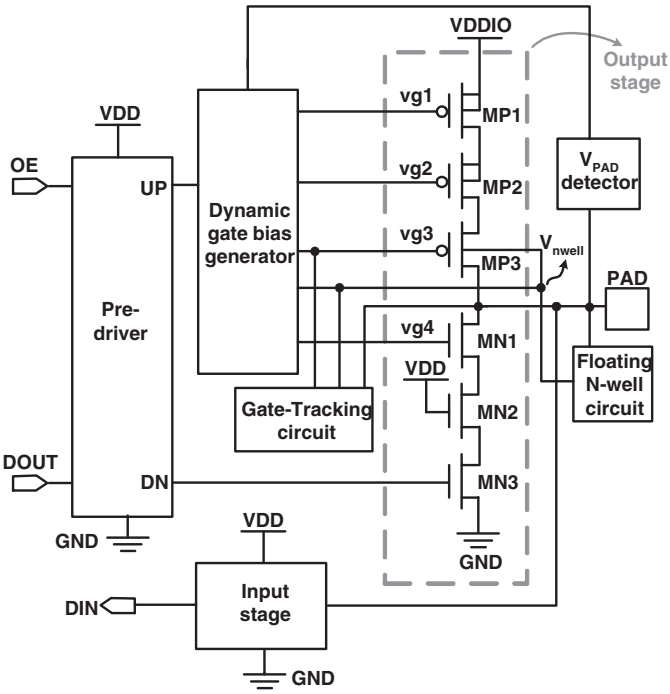


Fig. 1. Block diagram of the proposed mixed-voltage I/O buffer.

II. 0.9 V to 5 V Mixed-Voltage I/O Buffer

Fig. 1 shows the block diagram of the proposed I/O buffer consisting a Pre-driver, an Input stage, an Output stage, a Dynamic gate bias generator, a Floating N-well circuit, a Gate-Tracking circuit, and a V_{PAD} detector.

A. Output stage

Since the supply voltage (VDD) of the core circuits is 1.8 V in 0.18 μm CMOS process, the output stage must be realized with three stacked PMOS and NMOS transistors, respectively, for 2×VDD<5 V<3×VDD, as depicted in Fig. 1. Besides, appropriate gate voltages are needed for MP1∼MP3 and MN1∼MN3 to ensure the gate-oxide reliability and correct functions. Notably, in the receiving mode, when V_{PAD} is higher than VDD, the parasitic diode existing in MP3 is easily turned on to cause undesirable leakage current. Therefore, the gate tracking circuit and the floating N-well circuit are adopted to avoid this problem.

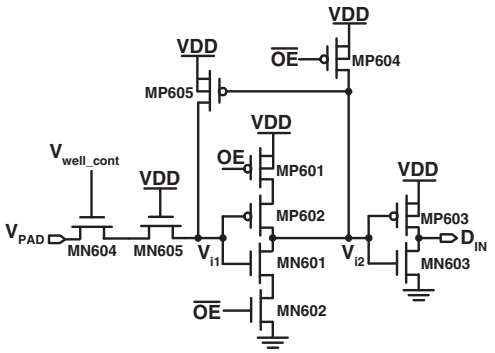


Fig. 2. Input stage circuit.

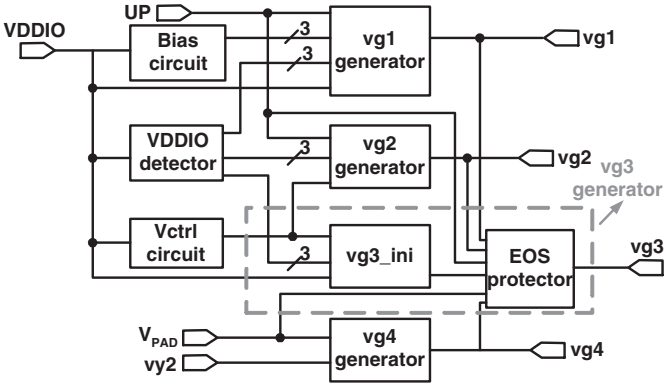


Fig. 3. Block diagram of the Dynamic gate bias generator.

B. Pre-driver

The Pre-driver is a simple logic circuit to decode and pre-drive. When the voltage of control signal OE is at 1.8 V, the I/O buffer operates in the transmitting (TX) mode. The logic state of $\mathrm{V_{PAD}}$ is determined by $\mathrm{D_{OUT}}$. On the other hand, when the I/O buffer is in the receiving (RX) mode, OE is 0 V.

C. Input stage

As shown in Fig. 2, MN604 and MN605 are added to prevent MP602 and MN601 from gate-oxide overstress. MP605 is used to clamp $\mathrm{V_{i1}}$ at 1.8 V when logic 1 is received. MP601 and MN602 are turned off as well as MP604 is turned on to reduce power dissipation in the TX mode.

D. Dynamic gate bias generator

The Dynamic gate bias generator is composed of a VDDIO detector, vg1, vg2, vg3, and vg4 generators, as shown in Fig. 3. The details of each subcircuit will be analyzed in the following text.

1) Bias circuit and V_{PAD} *detector:* Referring to Fig. 4, the Bias circuit and $\mathrm{V_{PAD}}$ detector are both realized with a string of diode-connected PMOS transistors. The summation of the threshold voltages of the PMOS must be larger than VDDIO and $\mathrm{V_{PAD}}$, respectively, such that the transistors would be operated in the sub-threshold region to reduce the static current.

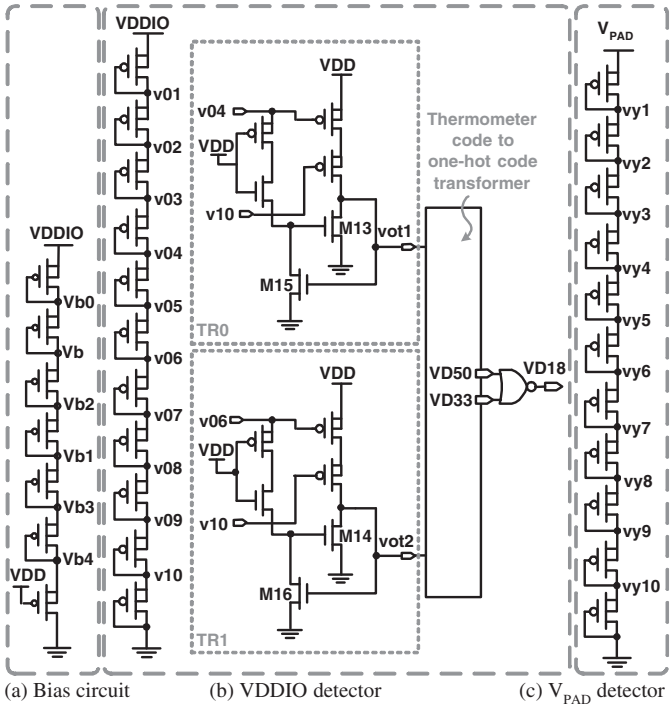


Fig. 4. Bias circuit, VDDIO detector and $\mathrm{V_{PAD}}$ detector.

2) VDDIO detector: VDDIO Detector is implemented with a string of diode-connected PMOS transistors, two detection circuits, (TR0, TR1), and a thermometer code to one-hot code decoder, as illustrated in Fig. 4. As mentioned previously, the summation of the threshold voltages are larger than VDDIO such that the DC current in the PMOS string is very small. The DC voltages V01∼V10 generated by the PMOS string devices are all proportional to VDDIO. V04, V06, and V09 are fed into TR0∼TR2 for VDDIO detection. M15 and M16 are added to discharge the gate voltage of M13 and M14 to 0 V, respectively, when vot1 and vot2 are at logic 1. Through simple glue logic gates, the thermometer code vot1 and vot2 could be easily converted into the one-hot code VD50 and VD33. Then, VD18 could be generated through a single logic gate. The thermometer code, vot1 and vot2, can be obtained according to various VDDIOs.

3) vg1 generator: In Fig. 5, vg1 generator comprises a cross-coupled latch and a voltage level converter, which outputs a pair of opposite signals, vg1 and $\overline{\mathrm{vg1}}$. It is basically composed of two cross-coupled transistors PMOS with two NMOS transistors in series as discharging paths. vg1 generator contains three pairs of discharging paths which are respectively controlled by the signals UP50, UP33, UP18, and their complementary signals. When VDDIO is fed with 5 V and MN105 is turned on, $\overline{\mathrm{vg1}}$ is discharged to 3.3 V through the first pair of discharging paths (MP103, MN101, MP105, MN103, and MN105) while vg1 is pulled up to VDDIO. When VDDIO is fed with 3.3 V, the second pair of discharging paths (MN107∼MN110, MN117, MN118, MP105, and MP106) is activated, which is controlled by UP33 and $\overline{\mathrm{UP33}}$. When VDDIO is fed with 1.8/1.2/0.9 V, the third discharging path (MN111∼MN116) is on. Referring to the logic equations in Fig. 5, any input voltage will appear in only one pair of

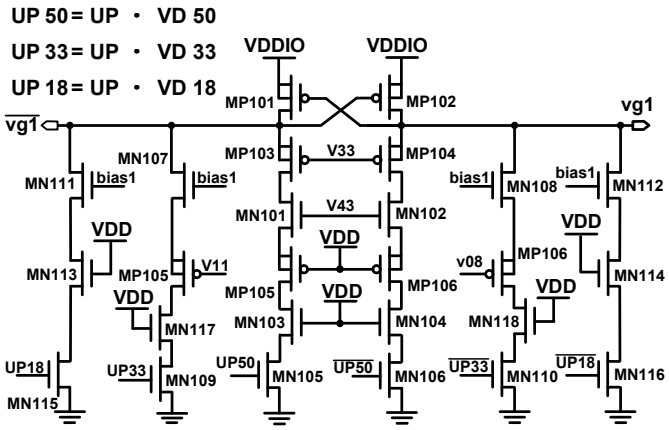
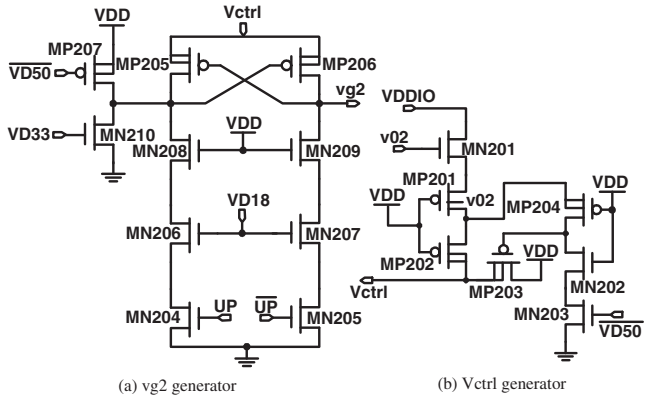


Fig. 5. vg1 generator.



(a) vg2 generator (b) Vctrl generator

Fig. 6. vg2 generator.

discharging paths.

4) vg2 generator: Fig. 6 shows the schematic of vg2 generator, while Vctrl is determined by the Vctrl generator varying with different VDDIO. vg2 generator is implemented with a level convertor to produce an appropriate voltage at the gate of MP2. When VDDIO is 5 V and Vctrl is 3.3 V, vg2 is charged to 3.3 V through MP205. On the other hand, vg2 will be charged to 1.8 V while VDDIO is 3.3/1.8/1.2/0.9 V. In Fig. 6 (b), MP204 is added to turn off MP203 avoiding the leakage current when VDDIO is 5 V.

5) vg3 generator: The proposed vg3 generator is depicted in Fig. 7, which is composed of $\mathrm{vg3\_ini}$ generator and EOS protector. In Tx mode, $\mathrm{vg3\_ini}$ is charged to 1.8-$|\mathrm{Vtn}|$ through MN318 when DOUT is at logic low. On the contrary, $\mathrm{vg3\_ini}$ is charged to 1.8 V through MP304 when DOUT is at logic high. In Fig. 7 (b), EOS protector constitutes a safeguard among devices against a permanent damage such as the electrical overstress phenomenon of the circuit operated at a high voltage signal. As VDDIO is 5 V given OE=1.8 V and $\overline{\mathrm{UD50}}$ =0 V in the Tx mode, vg3 will be biased between 3.3 V and 5.0 V and sent to Output stage depending on $\mathrm{vg3\_ini}$. In the same manner, when VDDIO is fed with 3.3/1.8/1.2/0.9 V, the output signal vg3 is properly biased from 0 V to 1.8 V.

E. ESD Protection Consideration

In traditional I/O buffers, the parasitic diode of the PMOS in the output stage can provide a discharge path for the ESD current. However, the parasitic diode connected to the I/O PAD and VDDIO does not exist due to the floating n-well circuit in the mixed-voltage-tolerant I/O buffer. Thus, the ESD capability of the mixed-voltage-tolerant I/O buffer is worse than that of traditional I/O buffers given the same size. In order to retain enough ESD capability, the penalty is the large area of NMOS and PMOS in Output stage. From the measurement results of several previous works [1]-[3], the ESD strength of the stacked output stage with their current driving ability higher than 25 mA can be equalized to 2 kV for HBM (human body model) and 200 V for MM (machine model) [3], [4]. Fig. 8 shows the simplified circuit with ESD consideration through discharging path and charging path. $\mathrm{V_{DS,NMOS}}$ and $\mathrm{V_{DS,PMOS}}$ can be derived as follows,

$$\mathrm{V_{DS,PMOS}} = \frac{\mathrm{V_{IL}} - \mathrm{V_{SS}}}{2} \tag{1}$$

$$\mathrm{V_{DS,NMOS}} = \frac{\mathrm{V_{IH}} - \mathrm{V_{SS}}}{2} \tag{2}$$

where $\mathrm{V_{IL}}$ and $\mathrm{V_{IH}}$ are set to 0.35×VDD and 0.65×VDD, respectively [4]. Moreover, Output Stage are operated in the triode region. Thus, by taking above conditions and the characteristic of transistors in triode region into consideration, the W/L ratio of PMOS and NMOS in the Output Stage can be determined.

III. Implementation and Simulation Results

The proposed design is implemented with a typical 0.18 μm CMOS process. Fig. 9 shows the layout of the proposed mixed-voltage I/O buffer. The maximum data rate given VDDIO = 5.0 V is simulated by thorough frequency scan, as shown in Fig. 10. Our circuit can be operated at 166 MHz under the most critical situation and the overstress problems are successfully overcome. The performance of the proposed mixed-voltage I/O buffer is summarized in Table I compared with prior I/O buffers. Table I shows that a wide voltage range, high speed, 3×VDD I/O buffer, is successfully achieved by this work.

IV. Conclusion

A PCI166-compatible 3×VDD mixed-voltage I/O buffer with ESD protection consideration is proposed. The signal from $\frac{1}{2}$×VDD to sub-3×VDD can be transmitted and received simultaneously. Besides, the effects of gate-oxide overstress and the leakage current are both eliminated.

V. Acknowledgment

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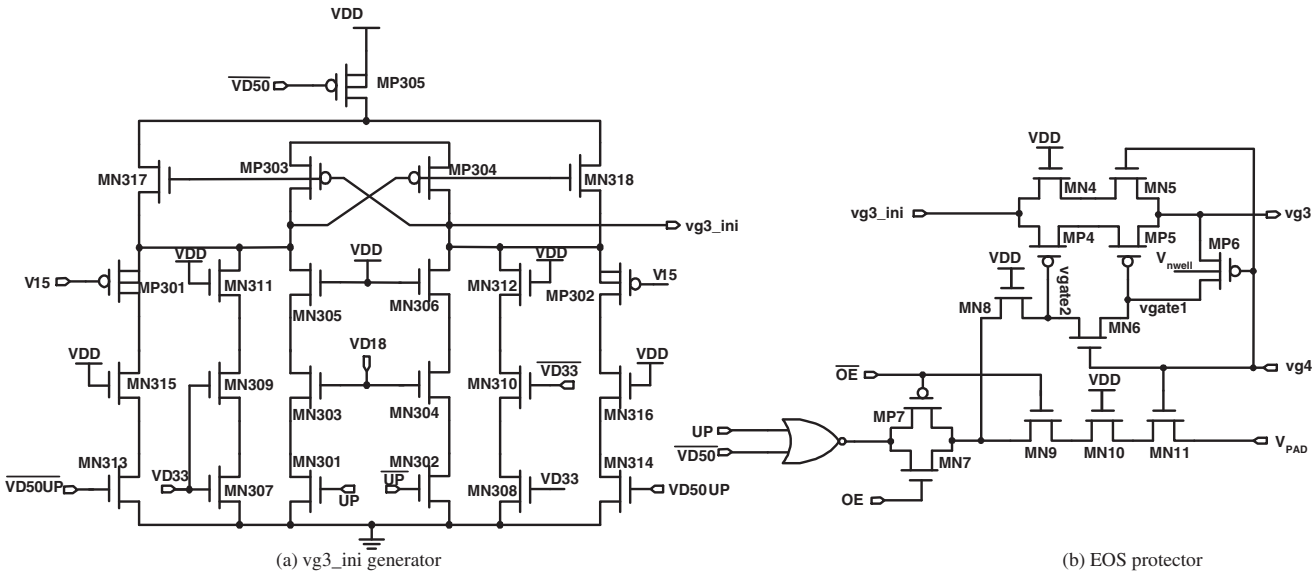
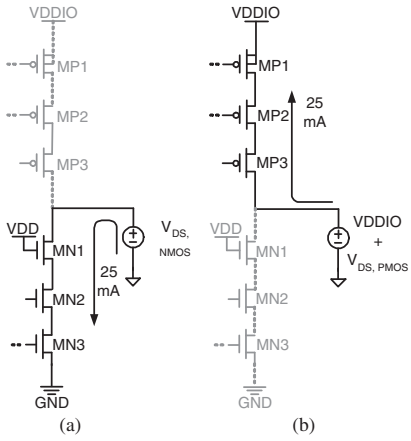
TABLE I
PERFORMANCE CAPARISON OF MIXED-VOLTAGE I/O BUFFER

	Year	Transmitting voltage mode (V)	Process (μm)	Frequency (MHz)	Area (μm$\times\mu$m)
This work	2010	0.9/1.2/1.8/3.3/5	0.18	166	65×652
[5]	2009	0.9/1.2/1.8/2.5/3.3/5	0.18	66	65×780
[6]	2009	5/3.3/1.8	0.35	60	1328×1126
[1]	2008	1.5/3.3	0.18	266	N/A
[2]	2007	1.2/2.5	0.13	133	107.73×65.38



(a) vg3_ini generator (b) EOS protector

Fig. 7. vg3 generator (a) $vg3_{\_ini}$ generator (b) EOS protector.



(a) (b)

Fig. 8. The simplified circuit of output stage with ESD protection. (a) Discharging path. (b) Charging path.

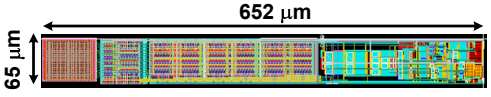


Fig. 9. Layout of the proposed mixed-voltage I/O buffer.

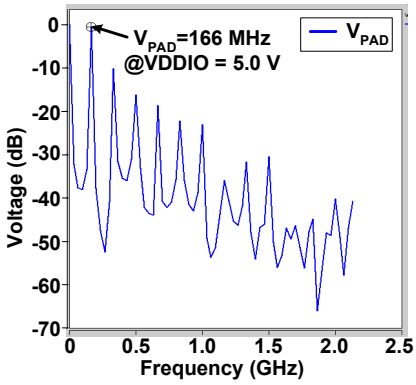


Fig. 10. The maximum date rate given VDDIO = 5.0 V.

REFERENCES

[1] M.-D. Ker, T.-M. Wang, and F.-L. Hu, "Design on mixed-voltage I/O buffers with slew-rate control in low-voltage CMOS process," in *Proc. 15th Int. Conf. on Electronics, Circuits and Systems*, pp. 1047-1050, Aug. 2008.

[2] H.-W. Tsai and M.-D. Ker, "Design of 2×VDD-tolerant I/O buffer with considerations of gate-oxide reliability and hot-carrier degradation," in *Proc. 14th Int. Conf. on Electronics, Circuits and Systems*, vol. 4, pp. 1240-1243, Dec. 2007.

[3] G. Liu, Y. Wang, and S. Jia, "A new design of mixed-voltage I/O buffers with low-voltage-thin-oxide CMOS process," in *Proc. 7th Int. Conf. on ASIC*, pp.201-204, Oct. 2007.

[4] *JEDEC Standard*, JESD82-7A, Oct. 2004.

[5] C.-C. Wang, J.-W. Liu, and R.-C. Kuo, "0.9 V to 5 V bidirectional mixed-moltage I/O buffer with an ESD protection output stage," in *Proc. IEEE Int. Conf. on IC Design and Technology,* pp. 29-32, May 2009.

[6] T.-J. Lee, T.-Y. Chang, and C.-C. Wang, "Wide-range 5.0/3.3/1.8 V I/O buffer using 0.35-um 3.3-V CMOS technology," *IEEE Trans. on Circuits and Systems-I: Regular Papers,* vol. 36, No. 4, pp. 763-772, Apr. 2009.