# A High Precision Low Dropout Regulator with Nested Feedback Loops

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***Abstract*—A high precision low dropout regulator (LDO) with nested feedback loops is proposed in this paper. By nesting a zero-tracking compensation loop inside of the negative feedback loop comprising an Error Amplifier, the independence of off-chip capacitor and ESR is ensured for different load currents and operating voltages. Therefore, in low Iddq or low voltage scenarios, the total error of the output voltage caused by line and load variations is less than ±3% according to on-silicon measurement results.**

***Index Terms*—Low dropout, low noise, and LDO**

## I. Introduction

THe LDO (low-dropout) regulator is generally utilized to translate a voltage level or provide a stable output voltage, which has been considered as one of the important components for the power management of wireless applications, e.g., cellular phones, hand-held computers, and particularly implanted wireless biomedical chips [1]. Traditional linear LDO regulators usually consist of a two-stage error amplifier, a power output stage and a negative feedback loop. However, since the stability and accuracy of the regulated output voltage is the most critical factor in many field applications such as biomedical chips, traditional designs suffer from poor efficiency as the difference between the input and output voltages is increased [2]. To attain a fast transient response and an accurate output voltage, several prior LDO regulators were proposed to use high gain amplifiers with either a cascade or cascode technology. It results in the stability problem due to the appearance of inherent three poles. Besides, the varying load current also affects the stability [3] - [5]. Thus, a frequency compensation technique to ensure the stability of the LDO regulator was proposed to resolve this problem [3] - [12]. Traditionally, the off-chip capacitor and its ESR (equivalent series resistor) are designed to move the zero around to achieve a pole-zero cancelation and keep the phase margin larger than zero degree. However, the off-chip capacitor increases the area of the printed-circuit board (PCB) and the value of the ESR might drift owing to the variation of the temperature and different materials. Therefore, the off-chip capacitor scheme is not acceptable in many applications demanding high precision. In this work, a new compensation architecture independent of the off-chip capacitor and its ESR is presented to enhance the LDO regulator's performance regarding the transient response and the noise rejection. Besides, a novel bandgap reference integrated with an error amplifier in a feedback loop is proposed to achieve the high precision of LDO.

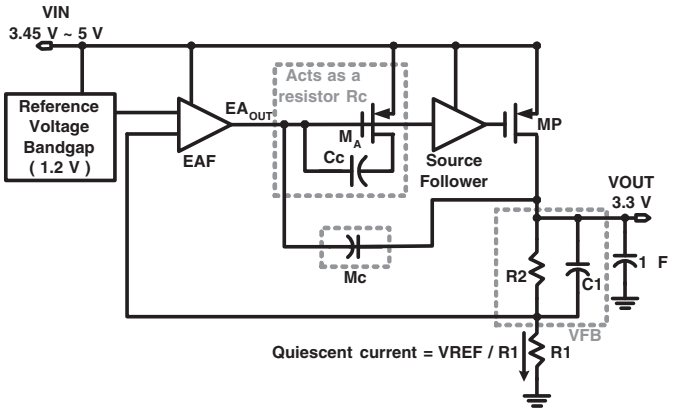


Fig. 1. Architecture of the proposed low noise low dropout regulator.

## II. Circuit Design

Fig.1 shows the block diagram of the proposed LDO which is composed of a Reference Voltage Bandgap, an Error Amplifier, a Source Follower, a Power MOS (MP), a voltage divider composed of R1 and R2, a variable resistance Rc.

### A. Bandgap Reference

To generate a stable voltage against process and temperature variations, a novel bandgap reference circuit is adopted. To enhance the capability against the supply voltage variation and the noise coupling from the substrate, a feedback loop with an error amplifier (EAB) is used as shown in Fig. 2. Assuming the gain of the EAB is very large, Vx and Vy are approximately equal, where Vy and Vx are the voltages at the inverting and noninverting input terminals of EAB, respectively. In Fig. 2, transistors M1 and M2 are both operated in saturation region. Taking channel-length modulation into consideration, the drain currents of M1 and M2, I1 and I2, can be written as

$$\mathrm{I1} = \frac{\beta_1}{2}(\mathrm{V_{GS1}} - \mathrm{V_{TH1}})^2(1 + \lambda \mathrm{V_{DS1}}) \quad (1)$$

$$\mathrm{I2} = \frac{\beta_2}{2}(\mathrm{V_{GS2}} - \mathrm{V_{TH2}})^2(1 + \lambda \mathrm{V_{DS2}}) \quad (2)$$

where $V_{GS1}$ and $V_{GS2}$ are the gate to source voltage of M1 and M2, respectively, $V_{TH1}$ and $V_{TH2}$ are the threshold voltage of M1 and M2, respectively, $\lambda$ is the channel-length modulation coefficient, $V_{DS1}$ and $V_{DS2}$ are the drain to source voltage of M1 and M2, respectively, $\beta_1$ and $\beta_2$ represent the device parameters of M1 and M2, respectively. Given that I1 = I2, $V_{GS1} = V_{GS2}$, $V_{DS1} = V_{DS2}$, we can have

$$V_{GS1} + V_{BE1} = V_{GS2} + I1 \times R3 + V_{BE2} \tag{3}$$

Eqn. (3) can be rewritten as

$$\begin{aligned} I2 &= \frac{V_{BE1} - V_{BE2} + V_{GS1} - V_{GS2}}{R3} \\ &= \frac{V_{BE1} - V_{BE2}}{R3} = I3 \end{aligned} \tag{4}$$

Since $V_{BE} = V_T \times \ln(\frac{Ic}{Is})$, and the size of Q2 and Q3 are both the $n$ times of that of Q1, I3 can be expressed as:

$$I3 = \frac{V_T \times \ln(n)}{R3} \tag{5}$$

Then, the sensitivity of I3 versus temperature can be derived as

$$\frac{\partial I3}{\partial T} = \frac{K}{q} \times \frac{\ln(n)}{R3} \tag{6}$$

Since Is=$cT^{4+m}\exp(\frac{-Eq}{KT})$, where $c$ and $m$ are constants, the sensitivity of $V_{BE}$ versus temperature can be derived as

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - \frac{Eq}{q}}{T} = -1.5\ (mV/K) \tag{7}$$

where T=300$^o$K, $V_{BE}$= 0.75 V in Eqn. (7).

In Fig. 2, VREF = I3$\times$ R4+$V_{BE3}$. Hence, the sensitivity of VREF versus temperature can be derived as

$$\frac{\partial VREF}{\partial T} = \frac{R4}{R3} \times \frac{K}{T}\ln(n) + \frac{V_{BE} - (4+m)V_T - \frac{Eq}{q}}{T} \tag{8}$$

Thus, the sensitivity of VREF can be eliminated by adjusting the value of R4 to generate a stable reference voltage.

### B. Source Follower

Source Follower is used to drive the large capacitance load and the small resistance load. The $EA_{OUT}$ is fed into the Source Follower to drive MP in the saturation region, where VB4 is a bias voltage connected to EAF, as shown in Fig. 3.

### C. Error Amplifier

Speed and gain always determine the performance of the LDO, and the speed of the LDO are mainly determined by the error amplifier, i.e., EAF, in Fig. 1. In order to reduce the the noise from VIN, EAF is implemented with a folded cascode structure, as shown in Fig. 3, where VB4 is a voltage bias connected to the following Source Follower. Moreover, the cascode structure can enlarge the gain to provide a precise output voltage of LDO.

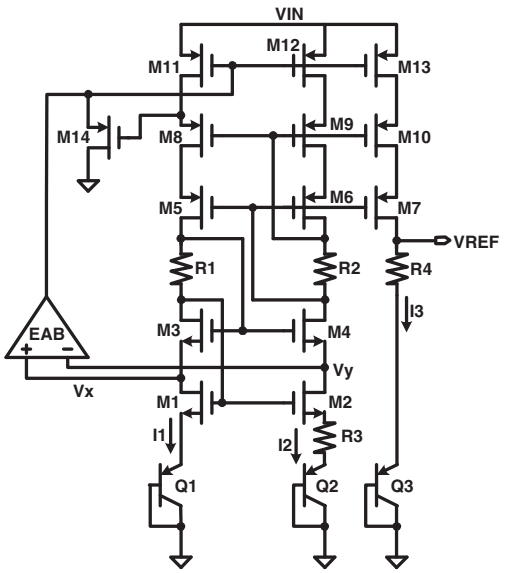


Fig. 2. The schematic of bandgap reference.

### D. Frequency Compensation

In a negative feedback system, the stability is always a critical issue. To ensure the stability of the system, the phase margin of the open loop gain should be carefully designed. In traditional LDO architectures, the phase margin is dominated by the load. Therefore, two frequency compensated methods are adopted to keep our LDO apart from load capacitor and its ESR.

*1) Zero-tracking compensation:* As shown in Fig. 1, the PMOS, $M_A$, is biased in the triode region to act as a variable resistance. Its resistance is varied with the voltage at VOUT, which is the load voltage. Therefore, the zero is varied with the dominant pole to avoid the bandwith of the LDO from decreasing. Meanwhile, the phase margin is also compensated.

*2) Nested Miller compensation:* A small Miller capacitor, Mc, is inserted on the feedback path to the gate of $M_A$, as shown in Fig. 1. Besides, the feedback voltage divider composed of R1 and R2 are connected with C1 in parallel to generate a extra zero and pole. When the pole's frequency equals (1+R2/R1)k times of the zero's frequency, the noise of the system can be eliminated, where k is the experimental constant. According to our measurement in Section III, the frequency of the pole is about 2.75 times of the zero's frequency.

## III. Simulation and Measurement

### A. Simulation of the Bandgap Reference

The low noise LDO is designed and fabricated in a 0.18 $\mu$m standard CMOS process. The bandgap reference with a compensated Error Amplifier has been simulated given the temperature from -40 $^o$C to 120 $^o$C. as shown in Fig. 4. VREF has a variation of $\pm$1 mV from the mean value 1.204 V given different process corners. A stable VREF is obtained given different VIN from 3 V to 5 V, as shown in Fig. 5.

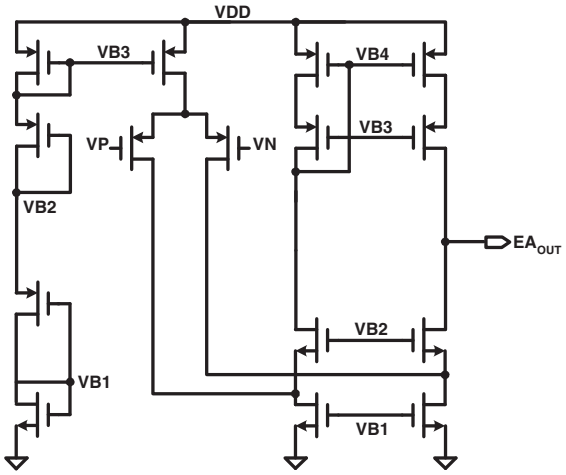


Fig. 3. Error amplifier (EAF).

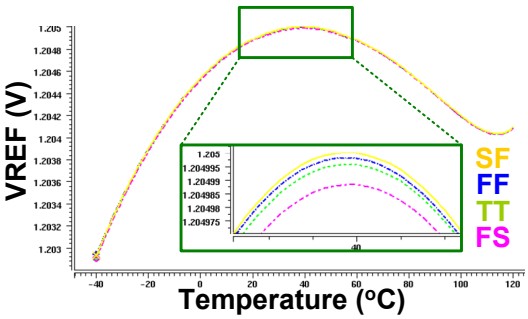


Fig. 4. Bandgap reference simulations given different process corners.

### B. Measurement Results for the Proposed LDO

Fig. 6 shows the die photo of the proposed circuit. The measured environment is composed of an digital oscilloscope, a function generator, and a power supply. The smallest dropout of the LDO is 0.018 V while the output current is 165 mA, the output load is 4.7 $\mu$F and 20 $\Omega$ in parallel. Fig. 7 shows the transient response of LDO in the line regulation measurement. When VIN is switching switching from 3.45 V to 5 V, VOUT is stable with a settling time less than 36.55 $\mu$s and a line regulation of 0.012%. When load regulation is measured, the test configuration with R5 = 1K $\Omega$ and R6 = 14 $\Omega$ in Fig. 8 is used, where R5 and R6 are load resistances. Fig. 9 shows the measured transient response of LDO at VIN = 3.3 V with the output current switching from 120 mA to 0 mA. When M0 is turned off, VOUT is stabilized with a settling time less than 42.54 $\mu$s and a load regulation of 0.005%. Fig. 10 and Fig. 11 shows the measured PSRR when VIN is at 30.08 kHz and 3.08 kHz, respectively. The quiescent current, Iddq, is 50 $\mu$A with a load current = 240 mA. The performance comparison of LDOs is shown in Table I. Our design has the edge of minimal line regulation, load regulation and dropout voltage.

## IV. Conclusion

In this paper, a novel bandgap reference with a compensated error amplifier for high precision LDO is proposed. This

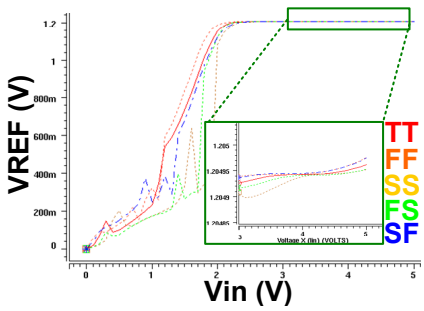


Fig. 5. VREF is stable given different VIN from 3 V to 5 V.

design is independent of the off-chip capacitor and its ESR. The measurement results justify its high precision with line regulation=0.012% and load regulation=0.005%. Moreover, the PSRR stays over 50 dB even if the operating frequency is up to 3.08 kHz.

## V. Acknowledgment

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TABLE I
PERFORMANCE CAPARISON OF LDO

| | [8] | [4] | [5] | [6] | Ours |
|---|---|---|---|---|---|
| process ($\mu$m) | 0.18 | 0.18 | 0.35 | 0.18 | 0.18 |
| year | 2009 | 2008 | 2007 | 2009 | 2010 |
| Line regulation (%) | 0.024 | N/A | N/A | 0.231 | 0.012 |
| Load regulation (%) | 0.7 | N/A | N/A | 0.101 | 0.005 |
| Dropout (V) | 0.3 | N/A | 0.2 | 0.541 | 0.018 |
| ESR zero required | Yes | No | No | Yes | No |
| Iddq (mA) | 0.028 | 0.027 | 0.02 | 0.035 | 0.05 |
| ILmax (mA) | N/A | 150 | 200 | 150 | 240 |


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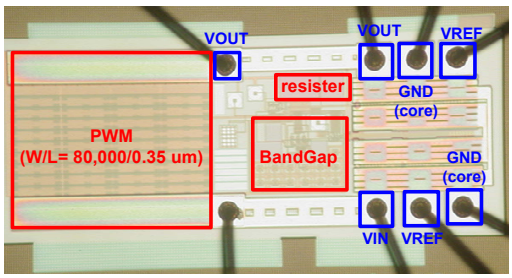


Fig. 6. Die photo of the proposed LDO.

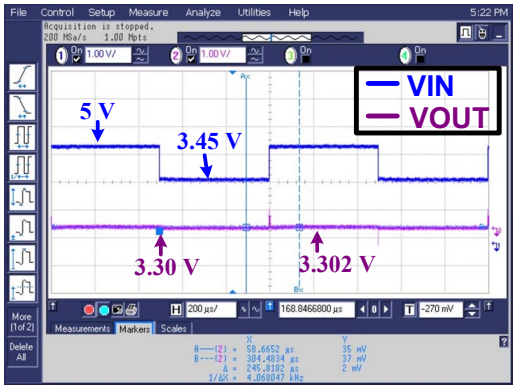


Fig. 7. Measured line regulation of proposed LDO.

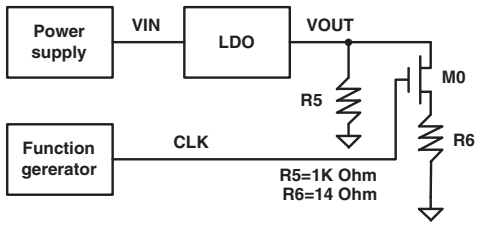


Fig. 8. Measured architecture for LDO Load regulation.

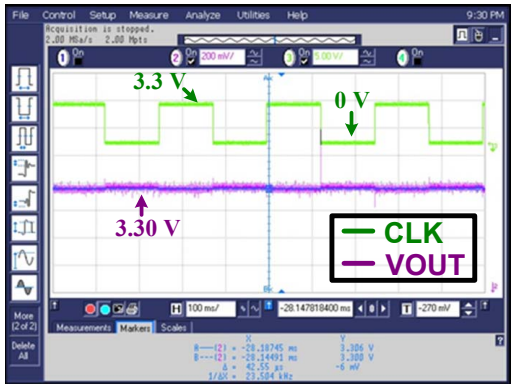


Fig. 9. Measured Load regulation of proposed LDO.

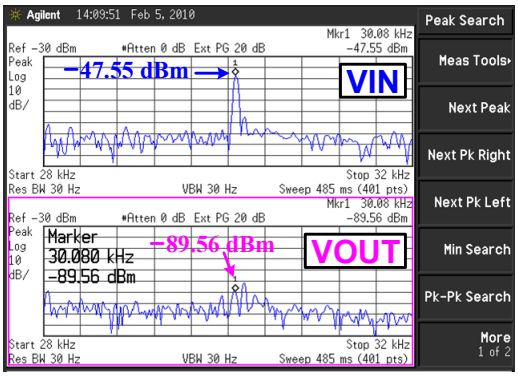


Fig. 10. Measured PSRR at VIN = 30.08 kHz.

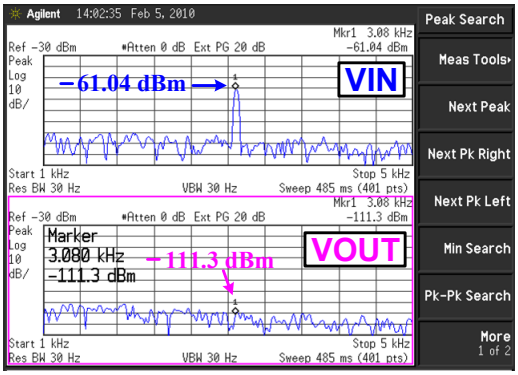


Fig. 11. Measured PSRR at VIN = 3.08 kHz.