450 MHz 1.0 V to 1.8 V Bidirectional Mixed-Voltage I/O Buffer Using 90-nm Process

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***Abstract*—A 1.0 V to 1.8 V mixed-voltage I/O buffer implemented with 90-nm 1-V standard CMOS devices is proposed. By using a dynamic gate bias generator to provide appropriate gate drive voltages for the output stage, the I/O buffer can transmit 2×VDD voltage level signal without any gate-oxide overstress hazard. Besides, the leakage current is eliminated by adopting a floating N-well circuit. The maximum data rate is simulated to be 340 MHz and 450 MHz for 1.8 V and 1.0 V, respectively, with a given capacitive load of 20 pF.**

***Index Terms*—mixed-voltage-tolerant, I/O buffer, floating N-well circuit, gate-oxide reliability**

I. Introduction

With the development of CMOS technology, the supply voltage of the integrated circuit (IC) is shrunk to nanometer scale to reduce power consumption [1]. When these chips using different processes and supply voltages are integrated in a PCB-based system, such as in PCI-X and PCI-express interface, conventional I/O buffers are not adequate to communicate due to the problems of gate-oxide reliability, hot carrier degradation, and the undesired leakage current path [2]. In past several years, many mixed-voltage I/O buffers were reported to deal with the chip interface problems of different voltage levels [1]−[4], [6]. However, the transmitting and receiving frequency of most previous works are not high enough to meet the specification of PCI-express, which is up to 266 MHz. Therefore, a wide range I/O buffer able to simultaneously transmit and receive signal from VDD to 2×VDD is deemed as a total solution for these scenarios. To communicate the signal with 2×VDD swing, double stacked transistors are used in the output stage to avoid the gate-oxide overstress. Notably, a simplified floating N-well circuit with low power consumption is adopted to avoid leakage current path produced by parasitic diodes. Besides, the current drive capability with ESD protection is also justified in this paper.

II. 1.0 V to 1.8 V Bidirectional Mixed-Voltage I/O Buffer

Fig. 1 (a) shows the block diagram of the proposed I/O buffer which is composed of a Pre-driver, an Input stage, an Output stage, a VDDIO detector, a Vg1 generator, a Vg2 generator, and a Floating N-well circuit.

A. Output stage

Since the supply voltage of the core circuits is 1.0 V in 90 nm CMOS process, the output stage must be realized with two stacked PMOS and NMOS for VDD<1.8 V<2×VDD, as depicted in Fig. 1. Besides, the appropriate gate voltages are needed for P_{o1}, P_{o2} and N_{o1}, N_{o2} to ensure the gate-oxide reliability and correct functions. The detailed operation of the Output stage is tabulated in Table I.

B. Pre-driver

The proposed Pre-driver is a simple logic circuit to decode and pre-drive. When the voltage of control signal OE is at 1 V, the I/O buffer operates at the transmitting mode (Tx mode). The logic state of VPAD is determined by D_{OUT}. Besides, the current drive capability of the signal D_{OUT} will be amplified by the Pre-driver to push other transistors with large scale. On the other hand, when the I/O buffer is at the receiving mode (Rx mode), the voltage of control signal is given at 0 V. The receiving signal D_{IN} would be determined by VPAD.

C. VDDIO detector

VDDIO detector is mainly implemented with a string of diode-connected PMOS to produce different voltage biases, V1∼V6, as illustrated in Fig. 1 (b). When VDDIO is at 1.8 V, MP003 is turned on and V1 is large enough to turn off MP001. In order to keep the voltage drop between V1 and the voltage of node neta less than 1 V, MP002 is added. The gate voltage of MP002, V3, is then maintained around 0.8 V to avoid reliability problems. At this time, MN001 is turned on to discharge the voltage of node neta to 0 V. The state of VD18 is then determined at logic 1. On the other hand, when VDDIO is at 1 V, MP003 is turned off and MP001 and MP002 are both turned on to pull up the voltage of node neta to 1 V. The state of VD18 is then determined at logic 0. As soon as

TABLE I
Gate Voltages of the Output Stage

	VDDIO (V)	V_{g1} (V)	V_{g2} (V)	V_{g4} (V)	V_{nwell} (V)
RX	1.8	1.8	1.0/Vpad[a]	0	1.0/Vpad[a]
	1.0	1.0	1.0	0	1.0
TX	1.8	>0.8/0	>0.8	1.0/0	1.8/1.0
	1.0	0/1.0	0	1.0/0	1.0

[a] When 1.8 V is received.
[b] Vg3 is operated at 1.0 V in all cases.

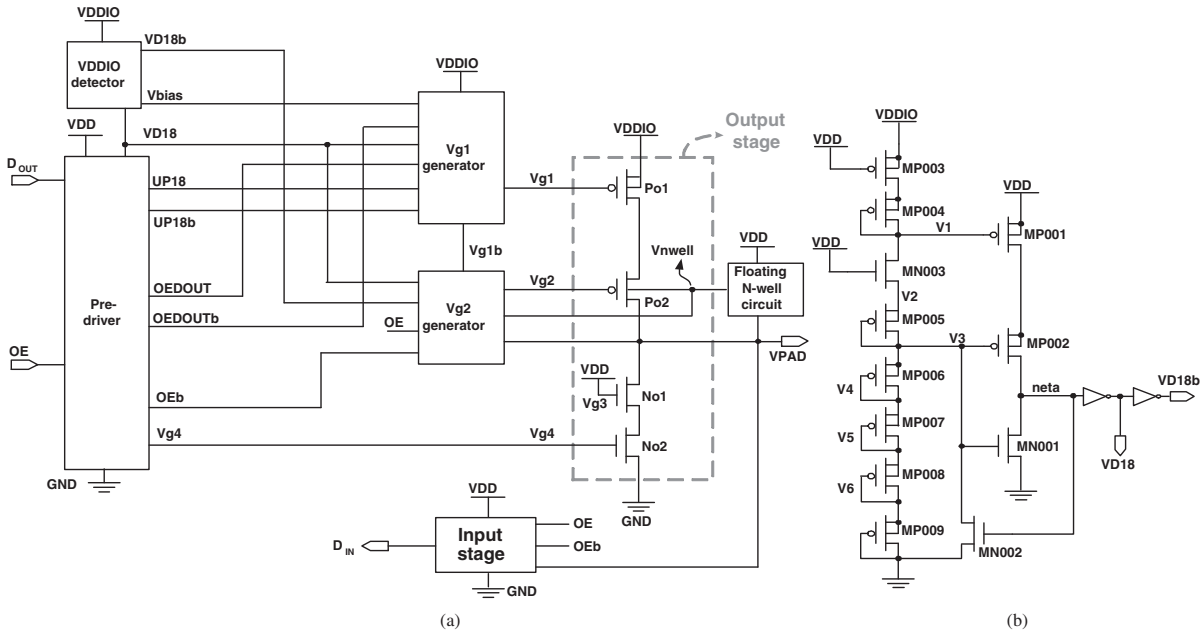

Fig. 1. The proposed mixed-voltage I/O buffer. (a) Block diagram. (b) VDDIO detector.

the voltage of node neta is up to 1 V, MN002 is turned on to turn off MN001 to eliminate the leakage current.

D. V_{g1} generator

In Fig. 4, V_{g1} generator comprises a voltage level converter, which outputs a pair of opposite signals, Vg1 and Vg1b. It is composed of two cross-coupled PMOS transistors with stacked transistors in series as discharging paths. In the Rx mode, the voltage of OEDOUT is biased at 0 V to make Vg1 equal to VDDIO. In this way, Po1 of Output stage can be turned off to eliminate the risk of leakage current. In the Tx mode, when VDDIO is at 1.8 V and the signal Dout is at logic 1, the voltage of OEDOUT is biased at 1.0 V to turn on the MN101. Then, Vg1 can be discharged down to V3+Vthp through MP103, MN103, and MN101, where Vthp is the threshold voltage of MP103. When the voltage of OEDOUT is biased at 0 V, MN102 is turned off to pull up Vg1b to VDDIO, which can also turn off the MP101 to prevent any static leakage current path.

E. V_{g2} generator

Fig. 4 shows the schematic of V_{g2} generator, including two basic floating N-well circuit cells, Cell A and Cell B, which are utilized to compare two voltages and output the higher one. In the Tx mode, when VDDIO is at 1.8 V and Dout is at logic 1, Vg1b biased at 1.8 V is fed into Cell A through MP203, while the voltage of node OEb is at 0 V to turn on MP204 to pass the voltage value of VDD into Cell A. After comparing two voltages, VDD and Vg1b, the higher one is presented at node netx to turn off MP202. At the same time, MN207 and MN208 are turned on to output 0 V at the node nety. Then, MP201 is turned on to pull up Vg2 to 1.0 V. When VDDIO is at 1.8 V and Dout is at logic 0, Vg1b is biased at 1.0 V to turn off MP203. Besides, VPAD is at logic 0 and the voltage of node netx is biased at 1.0 V to turn off MP202, which can keep VPAD and Vg2 from cross coupling.

In the Rx mode, Vg1b is always lower than 1.0 V to turn off MP203. When VPAD equals to 1.8 V, the gate voltage of MP207 is clamped by MN203 decreasing to 1.0 V. Then, MN204 is turned on and the voltage of node netx is charged to 1.0 V to turn on MP202. When Vg2 is pulled up to 1.8 V, the PMOS of Output stage in Fig. 1, Po2, is turned off to reduce leakage current risk.

F. Floating N-well circuit and Input stage

A traditional floating N-well circuit is adopted in this study. When VPAD is higher than VDD, Vnwell can be charged up to VPAD to avoid the undesired leakage current path through the parasitic diode of Po2 in Output stage.

As shown in Fig. 5, VPAD is clamped at 0.8 V by MN301 to prevent MP301 and MN302 from gate-oxide overstress in the Rx mode, while MP303 is used to charge the gate voltages of MP301 and MN302 to VDD. In the transmitting mode, MP305 is turned on and MP304 is turned off to reduce static power dissipation.

G. ESD Protection Consideration

From the measurement results of previous works [1]-[4], the ESD strength of the stacked output stage with their current driving ability higher than 25 mA can be equalized up to 2 kV

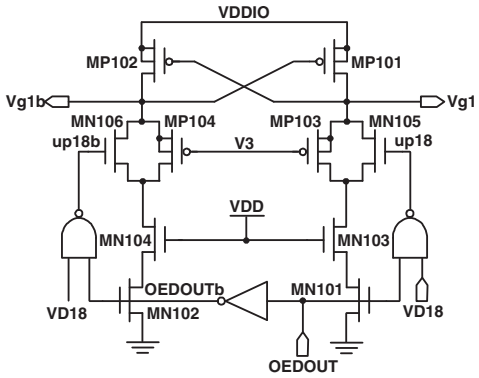

Fig. 2. V_{g1} generator.

for HBM (human body model) and 200 V for MM (machine model) [5]. Fig. 7 shows the simplified circuit with ESD consideration through discharging path and charging path. $V_{DS,NMOS}$ and $V_{DS,PMOS}$ can be derived as

$$V_{DS,PMOS} = \frac{V_{IL} - V_{SS}}{2} \quad (1)$$

$$V_{DS,NMOS} = \frac{V_{IH} - V_{SS}}{2} \quad (2)$$

where V_{IL} and V_{IH} are set to 0.3×VDD and 0.7×VDD, respectively [5]. Moreover, the Output stage are operated in triode region. Thus, by taking above conditions and the characteristic of transistors in triode region into consideration, the size of output stage can be estimated.

III. Simulation and Implementation Results

The proposed design is implemented using a typical 90 nm CMOS process. Fig. 6 shows the layout of the proposed mixed-voltage I/O buffer. The maximum data rate with different VDDIO are simulated in the Tx mode, as shown in Fig. 7. The waveform of V_{g1}∼V_{g2} and V_{well_out} with different VDDIO are illustrated in Fig. 8 and Fig. 9. Fig. 10 depicts the waveform of VPAD and DIN with different VDDIOs in the Rx mode. The performance of the proposed mixed-voltage tolerant I/O buffer is summarized in Table II which is compared with previous I/O buffers. Table II shows that a high frequency, wide voltage range I/O buffer for nanometer process, is successfully achieved by this work.

IV. Conclusion

A 1.0 V to 1.8 V mixed-voltage tolerant I/O buffer is proposed in this paper. The signal from VDD to 2×VDD can be transmitted and received simultaneously. Besides, the effects of gate-oxide overstress and the leakage current are both eliminated. All of the functions are verified through detailed all-PVT-corner simulation results.

V. Acknowledgment

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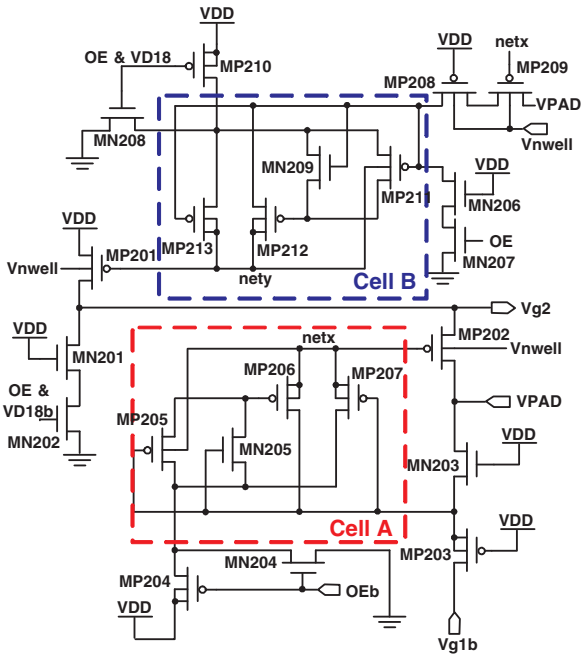

Fig. 3. V_{g2} generator.

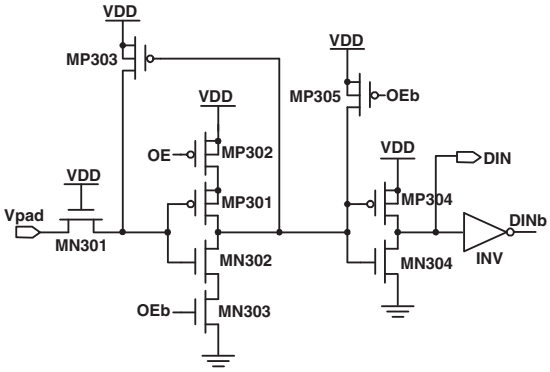

Fig. 4. Input stage circuit.

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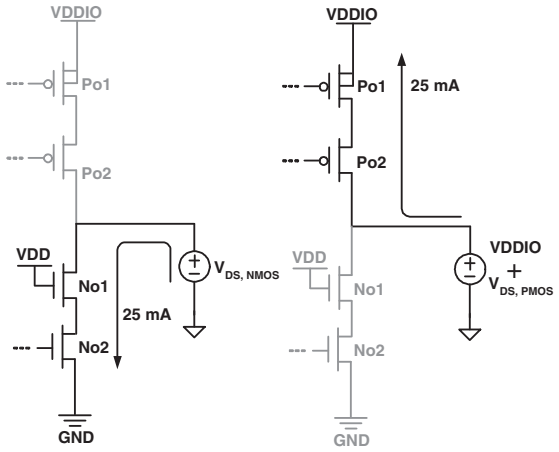

Fig. 5. The simplified circuit of output stage with ESD protection. (a) Discharging path. (b) Charging path.

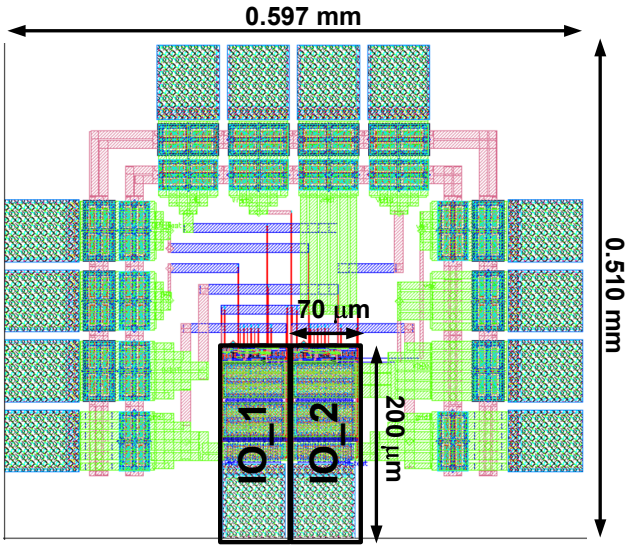

Fig. 6. Layout of the proposed mixed-voltage I/O buffer.

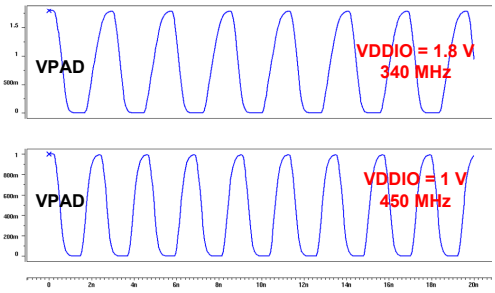

Fig. 7. The maximum data rate with different VDDIO in TX mode.

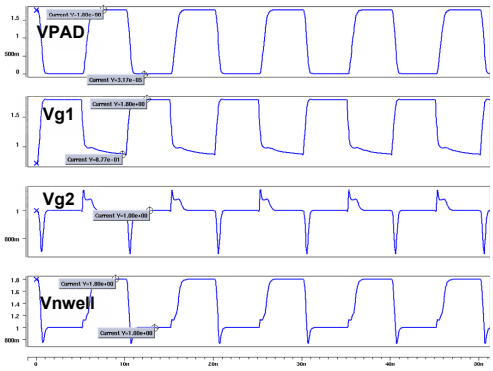

Fig. 8. V_{g1}~V_{g2} and V_{well_out} given VDDIO = 1.8 V in Tx mode.

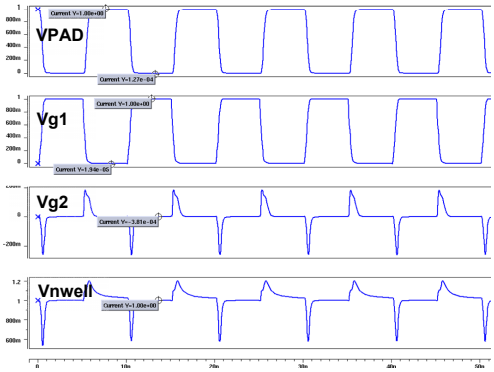

Fig. 9. V_{g1}~V_{g2} and V_{well_out} given VDDIO = 1.0 V in Tx mode.

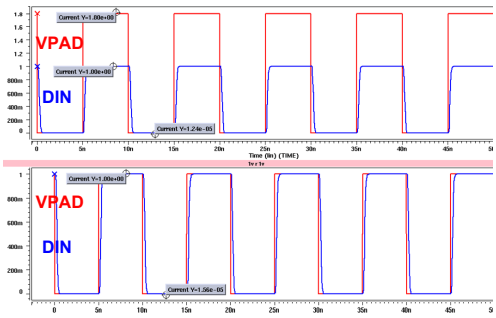

Fig. 10. VPAD and DIN with different VDDIO in Rx mode.

TABLE II
PERFORMANCE CAPARISON OF MIXED-VOLTAGE I/O BUFFER

	Year	Voltage modes (V)	Maximum frequency (MHz)	Process (μm)
This work	2009	1/1.8	450	0.09
[1]	2008	1.5/3.3	266	0.18
[2]	2009	1.5/3.3	133	0.13
[3]	2007	1.8/3.3	200	0.18
[4]	2006	2.5/5	200	0.25