A 125-MHz Wide-Range Mixed-Voltage I/O Buffer Using Gated Floating N-well Circuit

Chua-Chin Wang†, *Senior Member, IEEE,* Szu-Chia Liao, and Yi-Cheng Liu

***Abstract*—A fully bidirectional mixed-voltage I/O buffer using a gated Floating N-well circuit is presented. In addition, to provide appropriate gate voltages for Output stage, a Dynamic gate bias generator without gate-oxide overstress effect is implemented. The proposed I/O also takes advantage of a novel Gate-tracking circuit and a PAD voltage detector by means of eliminating the leakage current such that the compatibility among all subcircuits is ensured. Our design is proved on silicon that when VDDIO is 5.0/3.3/1.8/1.2/0.9 V, the maximum data rate is found to be 80/80/125/100/80 MHz, respectively, with a given capacitive load of 10 pF.**

***Index Terms*—wide-range I/O buffer, floating N-well, dynamic gate bias, mixed-voltage**

I. Introduction

Though the semiconductor process and core voltage are kept scaling down, the supply voltage on board is still remained as high as 3.3 V (or even 5.0 V), e.g., a PCI-X interface [1], [2]. Therefore, an I/O cell capable of receiving/transmitting different signal voltages is very much needed. Prior I/O buffer schemes have been proved to be prone to potential problems of hot-carrier degradation, gate-oxide overstress, and undesirable leakage current paths in advanced processes and applications nowadays [3], [4]. For instance, I/O buffers proposed in [3] - [7] were meant to improve these effects where many efforts have been thrown thereon except that the best performance among these designs can be applied only to three different voltage modes.

By contrast, our proposed design can provide the bidirectional communication interface with different voltages from $\frac{1}{2}\times$VDD to $3\times$VDD, i.e, from 0.9 V to 5.0 V given VDD = 1.8 V. Furthermore, the most attractive advantage in our design is a gated Floating N-well circuit such that a high data rate, e.g., 125 MHz is achieved. In addition, our design given the supply voltage VDD operating in 1.8 V is implemented by a standard CMOS 0.18 μm process using only thin-oxide devices for the fabrication cost reduction.

II. High-Speed Wide-Range Mixed-Voltage I/O Buffer

In this study, we adopt a gated Floating N-well circuit as well as a Gate-tracking circuit to eliminate the problems of body effect and the gate-oxide overstress caused by lower and higher voltage signals, respectively. Particularly, in the former, the operating speed can be enhanced. A PAD voltage detector is used to ensure the gate-oxide reliability for the transistors in Output stage. A Dynamic gate bias generator is employed to generate required bias voltages for other subcircuits.

The proposed high speed fully wide-range I/O buffer is shown in Fig. 1. In addition to the mentioned features, it comprises a Pre-driver, a High voltage detector, an Input stage, and an Output stage. Notably, the signal voltage level, i.e., VDDIO, can be transmitted or received at 0.9/1.2/1.8/3.3/5.0 V, while the supply voltage of the core circuitry is VDD = 1.8 V.

†Prof. C.-C. Wang is the contact author. He is with Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan 80424. (e-mail: ccwang@ee.nsysu.edu.tw)

A. Pre-driver

Pre-driver implemented by a digital CMOS logic circuit is used to pre-drive and decode digital signals delivered from the core circuitry. OE decides which one of the transmitting mode (OE = 1.8 V) or receiving mode (OE = 0 V) is selected. When the proposed system operates in the Tx mode, the logic state of V_{PAD} is determined by that of D_{OUT}, while the logic state of the receiving signal D_{IN} always follows that of V_{PAD}.

B. Input stage

MN12 and MN13 act as current-limiting resistors to prevent MN14 from the gate-oxide overstress when the voltage at PAD is high, i.e., V_{PAD} = 3.3/5.0 V, in Fig. 1. The detailed operation of Input stage is explained as follows.

In the Rx mode, when V_{PAD} = 5.0/3.3 V, Vi1 is near 1.4 V via MN12 and MN13 to ensure the gate-oxide reliability. Meanwhile, the gate voltage of the transistor MP12 is pulled up to 1.8 V as the logic state 1, i.e., V_{PAD} = 0.9/1.2/1.8/3.3/5.0 V. At the same time, Vi2 is pulled down to 0 V to turn on MP12 through the invertor composed of MP10 and MN14. Then, Vi1 is pulled up to 1.8 V.

If OE = 1.8 V in the Tx mode, both MP9 and MN15 will be off. MP11 is turned on to charge Vi2 to 1.8 V, whereas MP12 is turned off for the elimination of current leakage.

C. Output stage

There are three stacked PMOS and NMOS transistors in Output stage of Fig. 1 to alleviate the effect of gate-oxide overstress. The main functionality of Output stage is to safely transmit and receive the signal voltages from 0.9 V to 5.0 V. Their individual gate drives are mainly generated by Dynamic gate bias generator, which will be described later in the following text.

D. Gate-tracking circuit

Gate-tracking circuit which serves as switch controller of the gate voltage, i.e., Vmp3, at the Output stage, depending on the PAD voltage, is exhibited in Fig. 1. The major benefit of such a circuit design is to prevent from the potential problem of the leakage current path through the transistor MP3 in the Rx mode.

In the Tx mode, when VDDIO is fed with 5.0/3.3 V and the logic state is "1", Vmp1_b = 5.0/3.3 V as well as Vmp2 = 3.3/1.8 V. At the same time, Vmn1 can be biased at 3.3/1.8 V, and then MP8 can be charged to 5.0/3.3V via MP4, MP5, and MP6 to make Vmp3 independent of the PAD voltage so as to avoid the Gate-tracking circuit activating. In the Rx mode, if V_{PAD} is fed with 5.0/3.3 V and Vmn1 is equal to 3.3/1.8 V, MP7 will not only be turned on, but the gate drive of the transistor MP3 will follow the PAD voltage as well. However, if V_{PAD} is provided with the lower voltage such as 1.8/1.2/0.9/0 V, both Vmn1 and the gate drive of the transistor MP8 will be biased at 1.8 V. Thus, the transistor MP7 will be on, while the transistor MP8 will be off.

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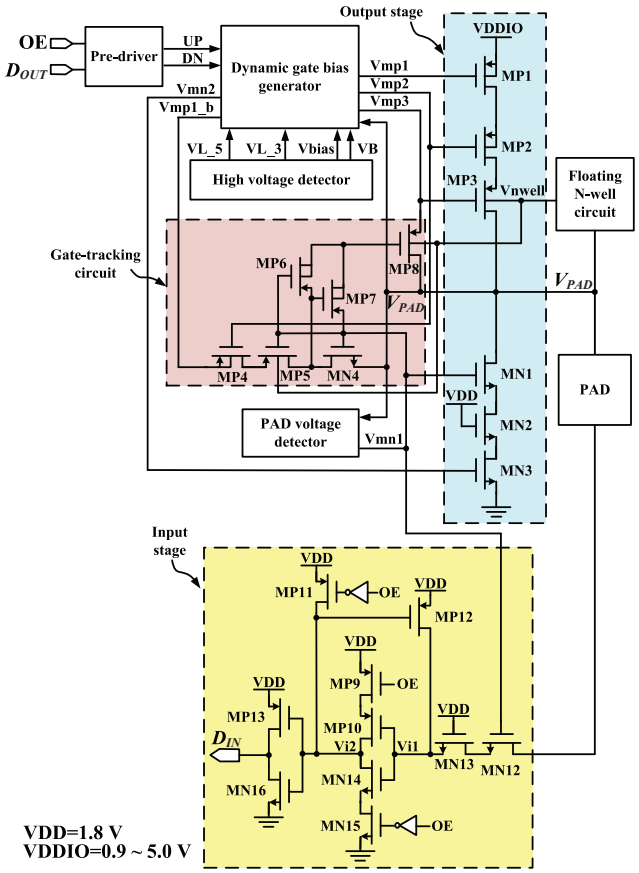


Fig. 1. Schematic diagram of the proposed wide-range bidirectional I/O buffer

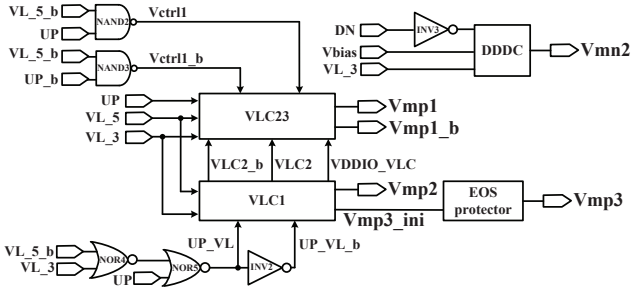


Fig. 2. Schematic diagram of Dynamic gate bias generator

E. Dynamic gate bias generator

Dynamic gate bias generator, including two level converters (VLC1 and VLC23), a dynamic detection driven circuit (DDDC), an electrical overstress (EOS) protector, and some digital logic gates, that is depicted in Fig. 2, plays an important part in compatibility among the subcircuits of the entire I/O, or rather it makes a great impact on the entire system performance especially in its tolerance of the mixed-voltage range. In view of this, the design provides the appropriate gate drives for the transistors MP1, MP2, MP3, and MN3 in Output stage by means of ensuring the gate-oxide reliability in different scenarios such that the design can achieve the fully wide-range bidirectional performance. The detailed summary of the circuit analyzed in the Tx mode (OE = 1.8 V) is displayed in Table I.

However, the voltage levels of Vmp1, Vmp2, and Vmp3 in the receiving state are the same as those when the logic 0 is transmitted in the Tx mode. Besides, the particular case is that when the signal is received with 5.0/3.3 V voltage at PAD, Vmp3 is charged toward 5.0/3.3 V through Gate-tracking circuit. This can avoid the leakage current caused by the transistor MP3.

1) VLC1: The proposed VLC1 depicted in Fig. 3 (a) is used to provide Output stage with two biases, Vmp2 and Vmp3, while Vmp3 is generated by EOS protector and Vmp3_ini. Also, this design generates two control signals as well as a voltage level, i.e., VLC2, VLC2_b, and VDDIO_VLC to VLC23. Besides, the circuit functionality in the part of the dotted line of Fig. 3 (a) is to generate a voltage, i.e., VDDIO_VLC, varied with VDDIO. Obviously, a 2×VDD voltage level convertor is implemented through the detailed circuit analysis, whose results are summarized in Table II.

2) DDDC and EOS protector: Both DDDC and EOS protector are shown in Fig. 3 (b) and (c), respectively. The function of DDDC is to offer proper biases to Output stage based on VDDIO such that it alleviates the problem of duty cycle distortion, especially in the scenario that when VDDIO is lower than 1.8 V, the voltage difference between gate and source of PMOS drops seriously in Output stage. In addition, EOS protector constitutes a safeguard among devices against a permanent damage such as the electrical overstress phenomenon of the circuit operated at a high voltage signal. As VDDIO is applied with 5.0 V given OE = 1.8 V and VL_5 = 0 V in the Tx mode, Vmp3 will be biased between 3.3 V and 5.0 V and sent to Output stage depending on Vmp3_ini. In the same manner, when VDDIO is fed with 3.3/1.8/1.2/0.9 V, the output signal Vmp3 is properly biased from 0 V to 1.8 V.

On the contrary, if V_{PAD} = 5.0/3.3 V in the Rx mode, Vgate1 and Vgate2 determined by PAD voltage will be pulled up to 5.0/3.3 V and down to 3.3/2 V, respectively, due to the corresponding signals passing through the Gate-tracking circuit. Similarly, if V_{PAD} = 1.8/1.2/0.9/0 V, both Vgate1 and Vgate2 will be charged (discharged) to 1.4/1.2/0.9/0 V.

3) VLC23: As shown in Fig. 4, VLC23 generates two critical biases, Vmp1 and Vmp1_b, to Output stage and Gate-tracking circuit, whose functionality is to effectively generate a higher voltage such as 3×VDD level, namely 3×VDD voltage level convertor. After completely analyzing the operation mechanism of the above items depending on VDDIO, we attain the same results as the first, third, and sixth columns in Table I.

F. High voltage detector

High voltage detector composed of a bias circuit and two detector circuits, i.e., Detector 1 and Detector 2, to pass the four output signals on, i.e., VB, Vbias, VL_5, and VL_3, of Fig. 5 (a) with a closed-loop structure such that not only do all transistors enter the subthreshold region, but attain very low static current as well. The scheme has the capability of detecting if VDDIO is higher than 1.8 V or 3.3 V as well as of generating two corresponding signals, VL_5 and VL_3, to Dynamic gate bias generator. The results of the circuit analysis are briefly summarized in Table III.

G. PAD voltage detector

Consider a simplified structure of the PAD voltage detector and refer to Fig. 5 (b). Such a major role does this circuit play that it will effectively control the gate drive of MN1, i.e., Vmn1, from Output stage, depending on the PAD voltage. Thus, after analyzing this circuit, we give a brief summary that Vmn1 is operated at 3.3/1.8/1.8/1.8/1.8/1.8 V for the PAD voltages with 5.0/3.3/1.8/1.2/0.9/0 V, respectively.

TABLE I
FUNCTIONAL TABLE OF DYNAMIC GATE BIAS GENERATOR

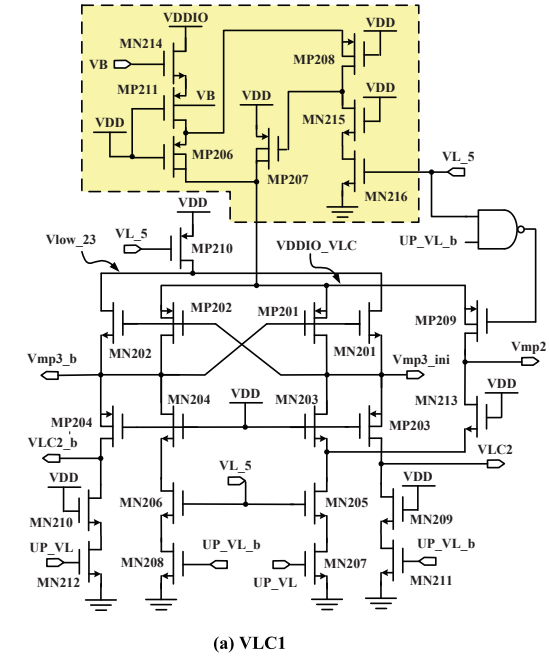
VDDIO	UP	Vmp1	Vmp2	Vmp3	Vmp1_b	Vmn2
5.0 V	0 V	3.3 V	3.3 V	3.3 V	5.0 V	0 V
	1.8 V	5.0 V	3.3 V	1.8 V	3.3 V	1.8 V
3.3 V	0 V	1.8 V	1.8 V	1.8 V	3.3 V	0 V
	1.8 V	3.3 V	1.8 V	1.8 V	1.8 V	1.8 V
1.8 V	0 V	0 V	0 V	0 V	1.8 V	0 V
	1.8 V	1.8 V	1.8 V	1.8 V	0 V	1.8 V
1.2 V	0 V	0 V	0 V	0 V	1.2 V	0 V
	1.8 V	1.2 V	1.8 V	1.8 V	0 V	1.2 V
0.9 V	0 V	0 V	0 V	0 V	0.9 V	0 V
	1.8 V	0.9 V	1.8 V	1.8 V	0 V	0.9 V

TABLE II
FUNCTIONAL TABLE OF VLC1

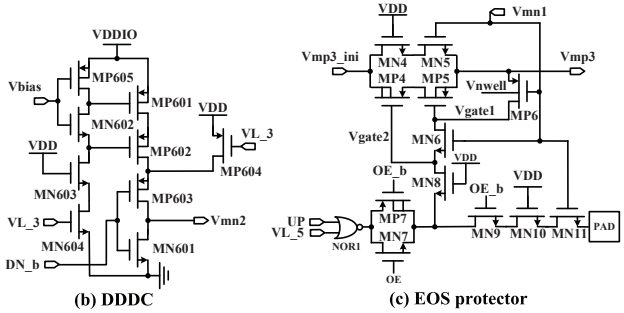
	VDDIO	Logic 0 is at PAD	Logic 1 is at PAD
Vmp2	5.0 V	3.3 V	3.3 V
	3.3 V	1.8 V	1.8 V
	1.8/1.2/0.9 V	1.8 V	0 V
Vmp3_ini	5.0 V	1.8 V	3.3 V
	3.3 V	1.8 V	1.8 V
	1.8/1.2/0.9 V	1.8 V	0 V
VLC2	5.0 V	0 V	3.3 V
VLC2_b	5.0 V	3.3 V	0 V
VDDIO_VLC	5.0 V	3.3 V	3.3 V
	3.3 V	1.8 V	1.8 V
	1.8/1.2/0.9 V	1.8 V	1.8 V

TABLE III
FUNCTIONAL TABLE OF
HIGH VOLTAGE DETECTOR

VDDIO	VB	Vbias	VL_5	VL_3
5.0 V	4.3 V	3.3 V	0 V	0 V
3.3 V	2.6 V	1.8 V	1.8 V	0 V
1.8 V	1.1 V	1.8 V	1.8 V	1.8 V
1.2 V	0.5 V	1.8 V	1.8 V	1.8 V
0.9 V	0.2 V	1.8 V	1.8 V	1.8 V



(a) VLC1



(b) DDDC (c) EOS protector

Fig. 3. Schematic diagrams of VLC1, DDDC, and EOS protector

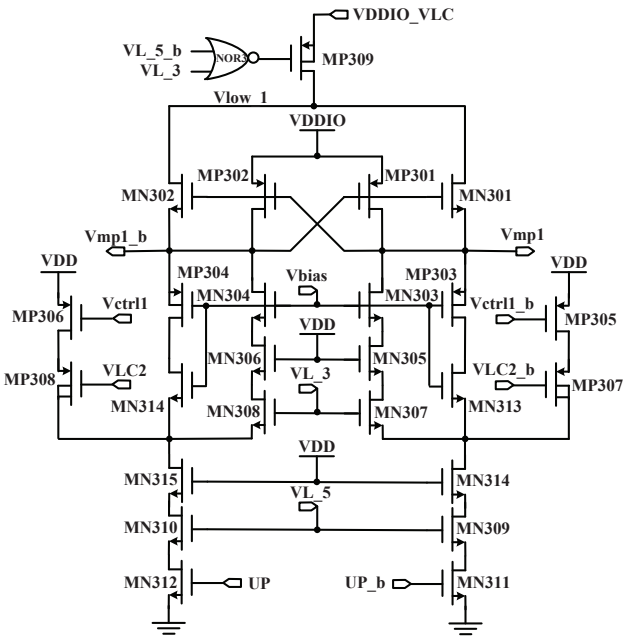


Fig. 4. Schematic diagram of VLC23

H. Floating N-well circuit

Last but not least, the gated Floating N-well circuit depicted in Fig. 6 is used to achieve high speed performance. Specifically, this circuit functions as a bulk bias generator for MP3 in Fig. 1 and Vnwell to Output stage such that it may not merely avoid the undesired leakage current through the parasitic P+/N-well diode, but also prevent the occurrence of the body effect generated when Output stage is operating in the Tx mode.

Next, the analysis proceeds in detail as follows. The lower voltage signals, i.e., 0.9/1.2/1.8 V, can be applied in the Tx mode. Furthermore, Vmp3 is equal to 0 V as well as the gate voltage of the transistor MP506 is applied at 1.8 V to turn off for the leakage current averted. However, when the logic 0 is transmitted, both Vmn1 and Vmp3 are biased at 1.8 V to shut MP501 and MP502 off. Then, Vnwell will be charged toward 1.8 V via MP506, MP505, and MP504. On the contrary, if the PAD voltage V_{PAD} is applied at a higher level such as 5.0/3.3 V, Vmn1 will be biased at 3.3/1.8 V, respectively. Meanwhile, both MP502 and MP503 will be on such that Vnwell will be pulled up to 5.0/3.3 V, whereas the transistor MP504 is off to prevent the phenomenon as already mentioned earlier.

As the PAD voltage is driven by 0/0.9/1.2/1.8 V in the Rx mode, Vmn1 and Vmp3 both equal to 1.8 V to turn MP501 and MP503 off. Moreover, Vnwell is charged to 1.8 V via MP506, MP505, and MP504.

III. Implementation and Measurement

To demonstrate the performance, we utilize only thin-oxide devices in 0.18 μm CMOS technology to implement the proposed design. The die photo of our I/O buffer is shown in Fig. 7. The maximum data rates with different VDDIO are shown in Fig. 8 (a) in the Tx mode. Next, given different V_{PAD} in the Rx mode, the waveforms of both V_{PAD} and D_{IN} in Fig. 8 (b) show that all of D_{IN} voltage levels are switched to 1.8 V. Finally, the performance of our scheme compared with that of prior I/O buffers is depicted in Table IV and our static power consumption is estimated to 17 μW in the worst case.

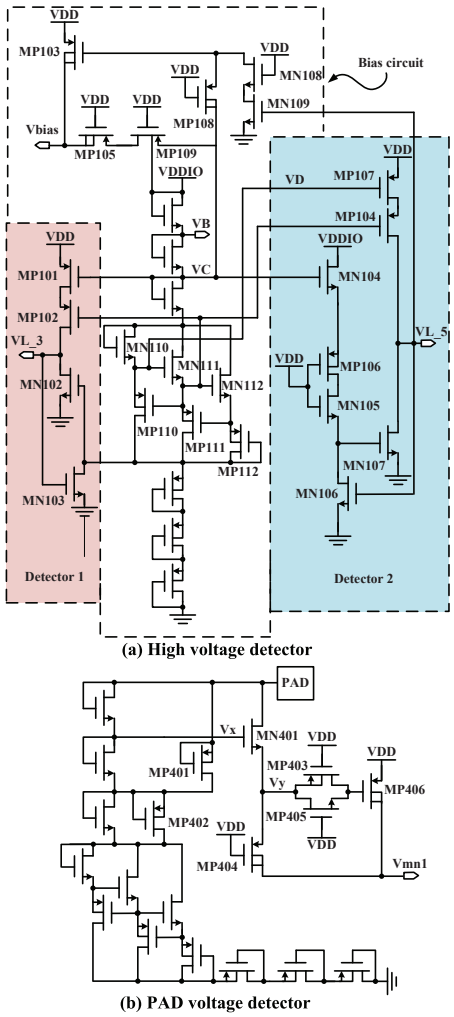


Fig. 5. Schematic diagrams of High voltage detector and PAD voltage detector.

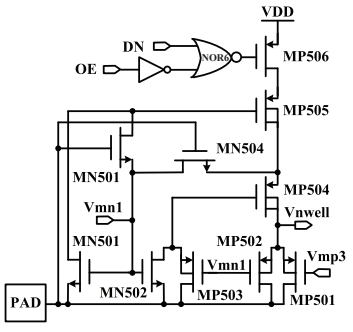


Fig. 6. Schematic diagram of Floating N-well circuit.

TABLE IV
COMPARISON WITH SEVERAL PRIOR WORKS

	[5]	[6]	[2]	[7]	Ours
# of voltage modes	1	2	1	3	5
Max. operating voltage	2.2VDD	3VDD	3.3VDD	1.5VDD	3VDD
Min. operating voltage	2.2VDD	VDD	3.3VDD	0.54VDD	0.5VDD
Normal voltage (VDD)	2.5 V	1.0 V	1.0 V	3.3 V	1.8 V
Process (μm)	0.25	0.13	0.13	0.35	0.18
Speed (MHz)	50	133	133	80	125
Year	2005	2006	2007	2009	2009

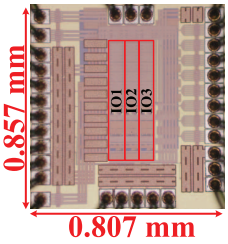


Fig. 7. Die photo of the proposed high-speed I/O buffer

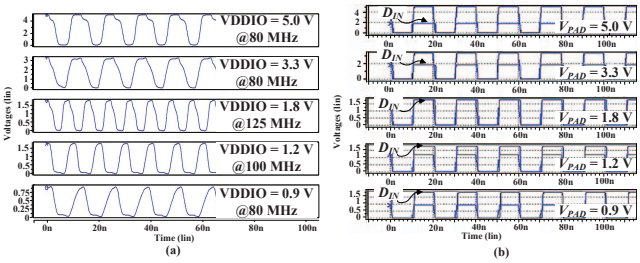


Fig. 8. (a) The maximum data rate with different VDDIO in the Tx mode and (b) V_{PAD} and D_{IN} with different V_{PAD} in the Rx mode.

IV. Conclusion

Implementation results indicate that our scheme without utilizing thick-oxide technology not only can transmit and receive the signals which are tolerant of different voltages from $\frac{1}{2}\times$VDD to $3\times$VDD, but also can attain the highest data rate, 125 MHz, by using an innovative Floating N-well circuit with a 1.8 V power supply. What is more, the intrinsic drawbacks of body effect, gate-oxide overstress, and leakage current are all obviated.

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