A Power-Aware Signed 2-Dimensional Bypassing Multiplier for Video/Image Processing

Gang-Neng Sung, *Student Member, IEEE*, Yu-Cheng Lu, Chua-Chin Wang, *Senior Member, IEEE*

***Abstract* – This paper presents a power-aware signed digital multiplier design by taking advantage of a 2-dimensional bypassing method dedicated for local multiplications widely used in FFT/IFFT operations of video/image processing. The proposed low power multiplier is carried out by Baugh-Wooley algorithm using novel 2-dimensional bypassing cells. The proposed bypassing cells constituting the multiplier skip redundant signal transitions when the horizontally (row) partial product or the vertically (column) operand is zero.**

Key word: low power multiplier, bypassing, Baugh-Wooley, partial product, FFT/IFFT computations.

I. INTRODUCTION

Booming of battery-operated multimedia devices requires energy-efficient circuits, particularly digital multipliers which are building blocks of digital signal processors (DSP). Besides adders, digital multipliers are the most critical arithmetic functional unit in many DSP applications, e.g., FFT/IFFT, Digital Cosine Transform, digital filtering, etc [1]. For instance, Fig. 1 shows a local FFT operation, where the multiplication operations are highly demanded in local computations. Array and parallel multipliers are very welcomed due to their high execution speed and throughput besides its high regularity for the local computations. However, the increasing capacitive wire load and operands' bit length result in very large power dissipation. In this work, we manage to reduce the power dissipation by an observation that the energy consumption of CMOS logic is proportional to the number of transitions. [2] proposed a "bypassing" multiplier which skips the addition when the partial product of a row is zero. We, thus, propose a signed 2-dimensional bypassing approach detecting the nullity of the partial products as well as the multiplicand at the same time to determine whether the additions on the corresponding row and those on the corresponding column are skipped or not, respectively.

II. SIGNED 2-DIMENSIONAL BYPASSING MULTIPLIER

A basic guideline to reduce the power dissipation of a digital multiplier is to reduce its unnecessary switching activities. Hence, we propose to detect the bitwise nullity of the multiplicand in the vertical direction and the partial product in the horizontal direction in an array multiplier to remove the unnecessary operations taken place in the corresp-ponding adding cells.

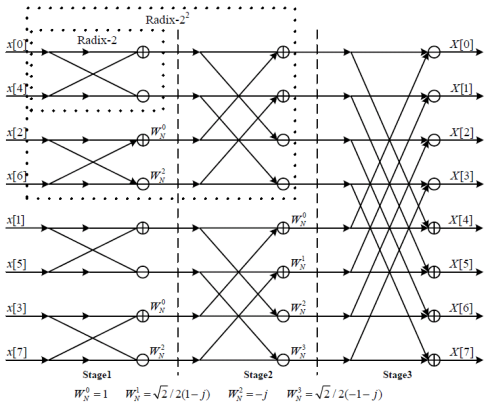


Fig. 1. Signal flow graph of an 8-point FFT.

A. Baugh-Wooley algorithm

A typical signed multiplication is based upon the following equations.

$$X = X_{n-1} \ldots . X_0 = -X_{n-1}2^{n-1} + \sum_{i=0}^{n-2} X_i 2^i$$

$$Y = Y_{n-1} \ldots . Y_0 = -Y_{n-1}2^{n-1} + \sum_{j=0}^{n-2} Y_j 2^j$$

$$P = XY = X_{n-1}Y_{n-1}2^{2n-2} + \sum_{i=0}^{n-2}\sum_{j=0}^{n-2} X_i Y_j 2^{i+j} - X_{n-1}\sum_{j=0}^{n-2} Y_j 2^{n+j-1} - Y_{n-1}\sum_{i=0}^{n-2} X_i 2^{n+i-1}$$

where P is the product, X is the multiplier, and Y is the multiplicand. X_i, i = n-1, …, 0 and Y_j, j = n-1, …, 0, are respectively the bit representations of the multiplier and the multiplicand, and n is the bit length of the operands. A typical implementation of such a signed multiplier is the Baugh-Wooley design shown in Fig. 2.

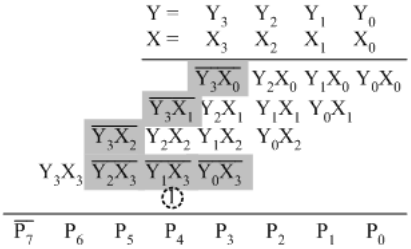


Fig. 2. A typical 4×4 Baugh-Wooley multiplier architecture.

Differences between signed and unsigned multiplier designs are that the partial products in the gray area of Fig. 2 of the Baugh-Wooley multiplier architecture should be inversed and added a "1" in the dotted circle.

* This research was partially supported by the National Science Council under grant NSC96-2628-E-110-018-MY3 and NSC97-2220-E-110-009.

[1] G.-N. Sung, Y.-C. Lu, and C.-C. Wang are with Department of Electrical Engineering, National Sun Yat-Sen University, 80424, Taiwan. (email: ccwang@ee.nsysu.edu.tw)

978-1-4244-4316-1/10/$25.00 ©2010 IEEE

B. 2-dimensional bypassing design

Besides the power saving by row-based bypassing [2], we utilize a signed 2-dimensional bypassing which detects the bitwise nullity of the multiplicand bits, Y_j's, in addition to the state of the multiplier, X_i's. In other words, as soon as the Y_j is found to be zero, the results from the adding cells residing in the previous column are automatically passed to the corresponding adding cells in the next column.

The proposed signed 2-dimensional bypassing multiplier architecture is shown in Fig. 3. The two "1"s in the dotted circles of Fig. 3 are used to realize the "1" in the dotted circle in Fig. 2. However, a conflict appears when one adding cell, AC_{ij}, encounters a scenario when $Y_j = X_{i+1} = 0$. In such a scenario, the $AC_{i+1,j}$ perhaps will lose the carry in.

For instance, assume i = 2, j = 1 and $X_2 = Y_1 = 0$ in Fig. 3 which shows a signed 2-dimentional bypassing 4 × 4 multiplier design. We expect the row 2 and the column 1 are bypassed. If the carry out of the adder upon the adding cell AC_{22} is "1", it should be propagated to the carry in of AC_{22}.

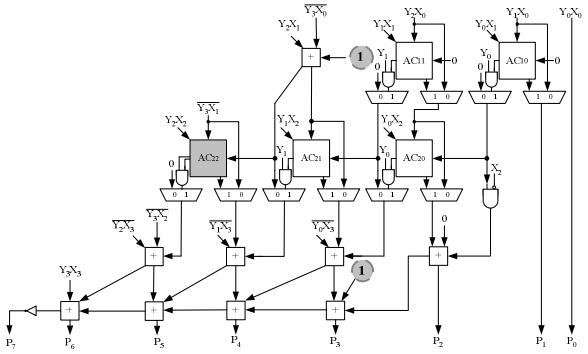
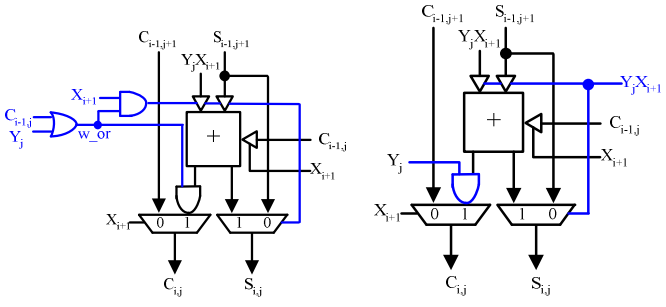


Fig. 3. Proposed signed 2-dimensional bypassing multiplier (4×4).

C. Adding cell with bypass logic

According to the above illustrative example, a simple rule is introduced: **If and only if X_i is not equal to "0" and the carry in is "1", then the adding cell, AC_{ij}, can not be bypassed.** Hence, an adding cell with the bypass logic is revealed in Fig. 4(a). It is also represented by a gray box in Fig. 3. Others AC_{ij}'s are shown as the one in Fig. 4(b).



(a) **(b)**

Fig. 4. (a) Adding cell with bypass logic. (b) Adding cell without bypass logic.

D. Domino effect in large multipliers

It is obvious that not every adding cell needs the bypass logic. It will be very area-efficient if we can identify which adding cells require the bypass logic to produce a correct multiplication result. Given n = 4, it can be easily concluded that AC_{22} is the only unit with the necessity of a bypass logic. If n = 5 and the identical array structure is used, then AC_{31}, AC_{32}, AC_{33}, AC_{23} need the bypass logic to attain correct results. By a similar induction, for any n × n multipliers, where n □ 5, all of the adding cells, AC_{ij} (n – 2 □ i □ 3, n – 2 □ j □ 1 and AC_{ij} (i = 2, j = n – 2), must contain the bypass logic to execute the correct multiplication. In other words, if n = 8, a totel of (8 – 4) × (8 – 2) + 1 = 25 adding cells with bypass logic are required, as show in Fig. 4. Therefore, the following rule is concluded.

Theorem 1: A total of (n – 4) × (n – 2) + 1 adding cells with bypass logic are required to constitute a signed 2-dimensional bypassing multiplier, ∀n > 3.

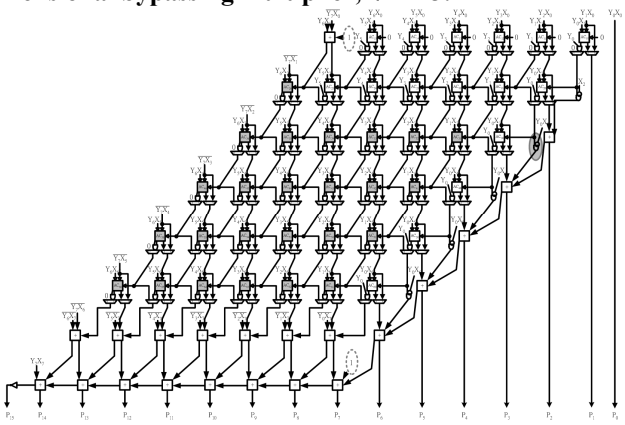


Fig. 4. An 8 × 8 signed multiplier using 2-dimentional bypassing.

III. Implementation and Measurement Result

A typical 0.18 um 1P6M CMOS cell-based design flow process was adopted to carry out the prototype of our design. Table I shows the comparison with other prior works. The proposed design shows a 20% of improvement of power-delay product (PDP).

TABLE I
COMPARISON IN CATE COUNT AND CLOCK RATE

	Process	Clk	Delay	Power	PDP
[3]	0.35 um	1 GHz	1 ns	60.18 mW	60.18 pJ
Baugh-Wooley	0.18 um	166 MHz	6 ns	6.66 mW	39.96 pJ
ours	0.18 um	166 MHz	6 ns	5.27 mW	31.74 pJ

References

[1] C.-C. Wang, J.-M. Huang, and H.-C. Cheng, "A 2K/8K mode small-area FFT processor for OFDM demodulation of DVB-T receivers," *2005 Inter. Conf. on Consumer Electronics (ICCE 2005)*, CD-ROM version, 4.1-2, Jan. 2005.

[2] J. Ohban, V. G. Moshnyaga, and K. Inoue, "Multiplier energy reduction through bypassing of partial products," in *Asia-Pacific Conference on Circuits and Systems,* vol. 2, pp. 13-17, Oct. 2002.

[3] H.-C. Chow, and I.-C. Wey, "A 3.3 V 1 GHz low-latency pipelined Booth multiplier with new Manchester carry-pass adder," *IEEE Inter. Symp. on Circuits and Systems,* vol. 5, pp. 121-124, May 2003.