A 1.8 V to 3.3 V Level-Converting Flip-Flop Design for Multiple Power Supply Systems

Chua-Chin Wang*, *Senior Member, IEEE*, Jen-Wei Liu*, Ron-Chi Kuo*,
Katherine Shu-Min Li†, and Sying-Jyan Wang‡
*Department of Electrical Engineering
National Sun Yat-Sen University, Kaohsiung, Taiwan
Email: ccwang@ee.nsysu.edu.tw
†Department of Computer Science and Engineering
National Sun Yat-Sen University, Kaohsiung, Taiwan
Email: smli@cse.nsysu.edu.tw
‡Department of Computer Science and Engineering
National Chung-Hsing University, Taichung, Taiwan
Email: sjwang@cs.nchu.edu.tw

***Abstract*—The voltage islands scheme using multiple supply voltages (MSV) has been widely used in system-on-chip (SOC) designs to reduce the unnecessary power dissipation in non-critical function blocks. In these SOC designs, the circuit blocks with the same voltage level are clustered into a single voltage island to reduce the cost of voltage supply network and the power consumption. However, a voltage level converter is required to stitch different voltage islands when the normal scan mode is activated. Besides carrying out the scan testing function, the level converter should be able to overcome the gate-oxide overstress problem given more than two supply voltages and backward compatibility. In this study, a 1.8 V to 3.3 V level-converting flip-flop (LCFF) implemented using 0.18 μm CMOS technology is proposed. By utilizing the voltage keeper technique, the power consumption and the power delay product (PDP) can be successfully reduced without any leakage current path.**

***Index Terms*—Dual-supply voltage, flip-flop, level conversion**

I. Introduction

The power consumption becomes an essential issue in modern VLSI circuits [1]. Since the power consumption is dominantly attributed to supply voltages, lowering supply voltage has been recognized as an effective way to reduce both dynamic and leakage power consumption [6]. Therefore, the technique of multiple supply voltages (MSV) has been proposed for low power application. Besides, clustering the circuit blocks with the same voltage level, called voltage islands scheme, has been widely realized for MSV in SOC designs to reduce the cost of voltage supply networks [2]- [5].

However, a level converter is required to stitch different voltage islands when the normal scan mode is activated. Several prior works has been proposed to deal with this issue especially for scan paths from lower voltage island to higher voltage island [6]- [9]. Nevertheless, level converters in [9] used to converting 2×VDD from VDDL to VDDH did not take gate-oxide overstress and leakage current problems into consideration. Therefore, in this paper, a novel 1.8 V to 3.3 V level-converting flip-flop implemented using 0.18 μm CMOS technology is proposed to resolve these problems.

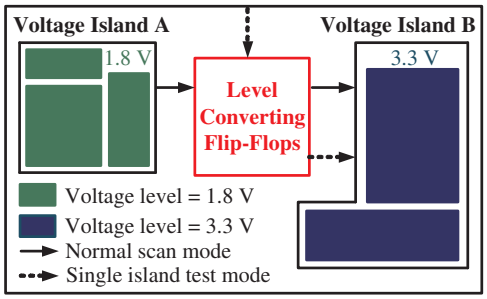

Fig. 1. Different voltage islands on a single chip.

II. Proposed Level Converter Flip-Flop

Fig. 2 shows the block diagram of the proposed 1.8 V to 3.3 V Level-Converting Flip-Flop which is constructed with a D Flip-Flop and a Voltage-Level Converter.

A. D Flip-Flop

The D flip-flop is composed of an inverter, a NAND3 and a delay element, as shown in Fig. 3. The inverse clock signal (CLKB) is generated by the delay element. When the clock signal(CLK) and the inverse clock signal(CLKB) are both high, the state of node q_18 will be changed by the input signal D. Otherwise, the state are remained the same. Therefore, this design is more power-saving than prior works.

When the signal CLK changed from logic 0 to logic 1, the signal CLKB is changed from logic 1 to logic 0. During such a short period defined by the delay element, signals CLK and CLKB can be both operated at logic 1, to turn on MN3 and MN4. Thus, if the input signal D is logic 0, the voltage of the node NAND3_OUT is biased at 1.8 V. Then, the voltage of node q_18 is pulled down through MN2, MN3, and MN4, while the voltage of the node netx is pulled up by the inverter INV.

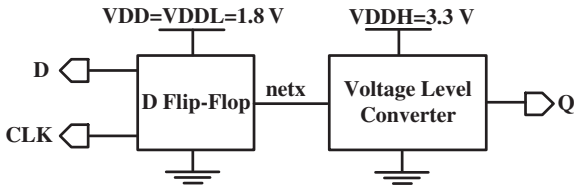

Fig. 2. Block diagram of the proposed level-converting flip-flop.

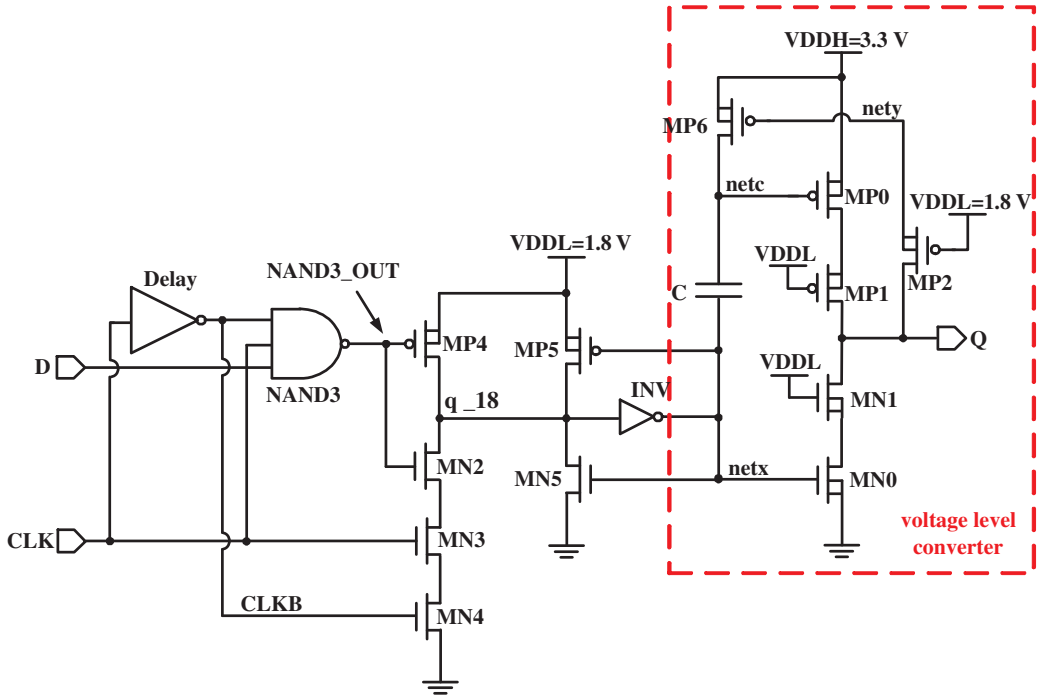

Fig. 3. Proposed level-Converting flip-flop without any leakage current path.

On the other hand, if the input signal is at logic 1 during this short delay time, the voltage of the node NAND3_OUT is biased at 0 V. Then, the voltage of node q_18 is aroused by MP4 such that the voltage of the node netx is pulled down by the inverter INV1.

B. Voltage Level Converter

The proposed voltage level converter is depicted in the right side of Fig. 3, where a small capacitor C (∼0.4 pF) is adopted. The stack transistors MP0, MP1, MN0, and MN1 are utilized to prevent output signal Q from overstress when VDDH equals to 3.3 V. When the voltage of signal Q equals to 3.3 V, transistor MP2 is turned on to charge the voltage of nety to 3.3 V. Then, transistor MP6 is turned off. On the other hand, When the voltage of signal Q changes to 0 V, MP2 is turned off to discharge the voltage of nety to 1.8 V+V_{thp}. Then, transistor MP6 is turned on to pull up the voltage of netc to 3.3 V such that transistor MP0 is turned off. At the same time, the voltage of netx is 1.8 V, the voltage of signal Q is discharged to 0 V through transistors MN0 and MN1. As soon as the voltage of netx is pulled down to 0 V, transistor MN0 is turned off to cause that the voltage of netc is pulled down to 1.5 V. Hence, MP0 is turned on and the output signal is charged to 3.3 V to avoid any overstress.

III. Simulation Results

To verify the proposed level converting flip-flop, the simulation environment is setup as shown in Fig. 4. I1∼I4 are realized with the proposed flip-flops, which are driven by a 2-to-4 decoder_1.8 V and four multiplexors M1, M2, M3, and M4. A 2-to-4 encoder_3.3 V is driven by the outputs of the proposed LCFFs. Notably, the 2-to-4 decoder_1.8 V with a 1.8 V power supply and the 2-to-4 encoder_3.3 V with a 3.3 V power supply are employed as different voltage islands. The proposed level-converting flip-flop is implemented in 0.18 μm CMOS technology without any thick oxide device. Fig. 5 shows the layout of the proposed design. The post-layout simulation results comparing with prior works are listed in Table I. Two functions, the normal scan mode and the single island test mode, are depicted as follows.

A. Normal Scan Mode

In the normal scan mode, the proposed flip-flops stitch the voltage islands. When the signal test2 is at logic 0, the

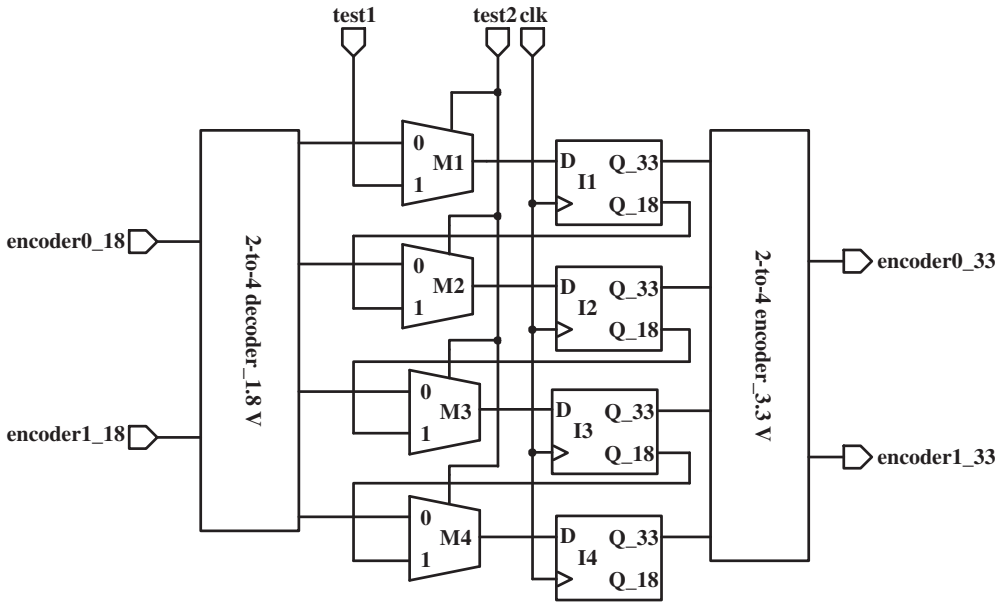

Fig. 4. Test circuit.

outputs of the 2-to-4 decoder_1.8 V are fed toward the flip-flops I1∼I4 through M1∼M4. Then, the signal which is stored and level converted by the I1∼I4 will be finally input to the 2-to-4 encoder_3.3 V. After encoded by the 2-to-4 encoder_3.3 V, the logic values of encoder0_33 are the same as those of encoder0_18. It is the same for encoder1_33 and encoder1_18. Fig. 6∼8 show the simulation results at different PVT (process, voltage, temperature) corners in the normal scan mode.

B. Single Island Test Mode

Due to the process drifting or the design uncertainty, the error of SOC may occur within a voltage island. To ensure the individual island's function correctness, an extra mode, called single island test mode, is added. When the signal test2 is at logic 1, the value of the signal test1 is read and stored in I1∼I4 on every rising edge of four consecutive clock cycles. After encoding the four values of the signal test1, the outputs, encoder0_33 and encoder1_33, are generated on the fourth rising edge of the clock clk. By scrutinizing the results, the function of the voltage island with 3.3 V power supply can be checked easily. Fig. 9∼11 show the simulation results at different PVT corners in the single island test mode.

IV. Conclusion

A 1.8 V to 3.3 V level-converting flip-flop using 0,18 μm CMOS technology is proposed in this paper. Two modes, normal scan mode and single island test mode, are provided in the flip-flop. The flip-flop can stitch different voltage islands in the normal scan mode. It can also justify the individual island's function when the single island test mode is activated. Besides, we overcome the gate-oxide overstress problem caused by more than two supply voltages and backward compatibility. By utilizing the voltage keeper technique, the power consumption and the power delay product (PDP) can be drastically reduced without any leakage current path.

TABLE I
Comparison with prior works

	Delay time (ps)	Average power (μW)	PDP
[9] LCMSSFF-I	286.77	59.83	171.57
[9] LCMSSFF-II	294.60	64.58	190.25
[9] LCHLSFF	277.50	124.68	345.98
This work	300	88.7	266.1

Acknowledgment

This investigation is partially supported by Ministry of Economic Affairs, Taiwan, under grant 97-EC-17-A-01-S1-104 and by National Health Research Institutes under grant NHRI-EX98-9732EI.

References

[1] K. Usami, "Overview on low power SoC design technology," in *Proc. Asia and South Pacific Design Automation Conf.*, pp. 634-636, Jan. 2007.
[2] D. Sengupta and R. Saleh "Supply voltage selection in voltage island based SoC design," in *Proc. 2008 IEEE Int. SOC Conf.*, pp. 219-222, Sept. 2008.
[3] X. Qiu, Y. Ma, X. He, and X. Hong, "Voltage island aware incremental floorplanning algorithm based on MILP formulation," in *Proc. 9th Int. Conf. on Solid-State and Integrated-Circuit Technology*, pp. 2264-2267, Oct. 2008.
[4] S. Lin, H. Yang, and R. Luo, "A novel low power interface circuit design technique for multiple voltage islands scheme," in *Proc. IEEE Int. Symp. on Circuits and Systems*, pp. 1401-1404, May 2007.
[5] R. Puri, D. Kung, and L. Stok, "Minimizing power with flexible voltage islands," in *Proc. IEEE Int. Symp. on Circuits and Systems*, pp. 21-24, May 2005.
[6] L.-Y. Chiou and S.-C. Lou, "An energy-efficient dual-edge triggered level-converting flip-flop," in *Proc. IEEE Int. Symp. on Circuits and Systems*, pp. 1157-1160, May 2007.

[7] P. Zhao, J. B. McNeely, P. K. Golconda, S. Venigalla, N. Wang, M. A. Bayoumi *et al.*, "Low-power clocked-pseudo-NMOS flip-flop for level conversion in dual supply systems," *IEEE Trans. Very Large Scale Integration Systems*, 2009, to be appeared.

[8] S. Lin, H. Yang, and R. Luo, "High speed soft-error-tolerant latch and flip-flop design for multiple VDD circuit," in *Proc. IEEE Computer Society Annual Symp. on VLSI*, pp. 273-278, Mar. 2007.

[9] K. S.-M. Li, M.-H. Hsieh, and S.-J. Wang, "Level converting scan flip-flops," in *Proc. IEEE Int. Symp. on Circuits and Systems*, May 2009, to be appeared.

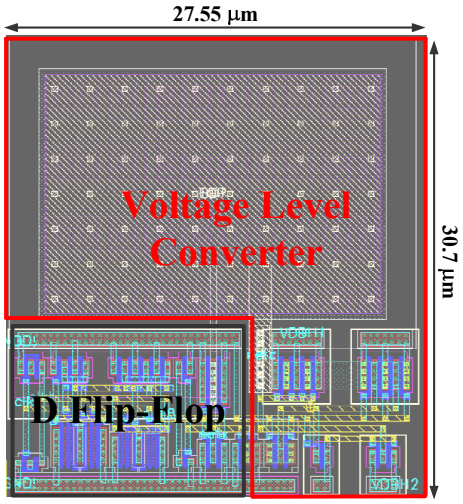

Fig. 5. Layout of the proposed level-converting flip-flop.

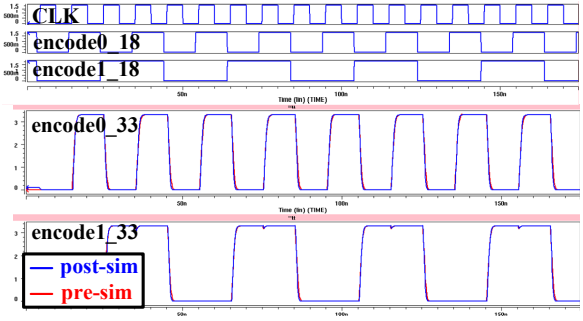

Fig. 6. Normal scan mode at corner TT, 25°C.

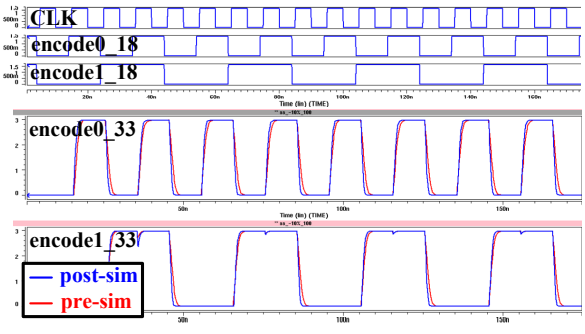

Fig. 7. Normal scan mode at corner SS, 100°C.

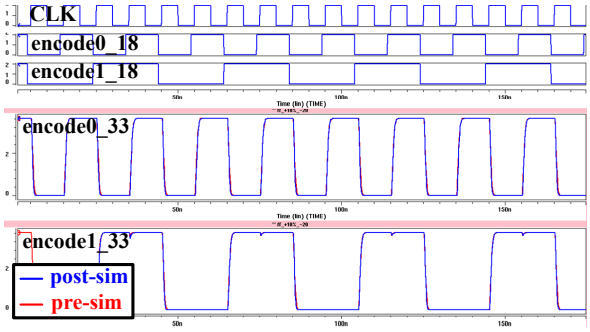

Fig. 8. Normal scan mode at corner FF, -20°C.

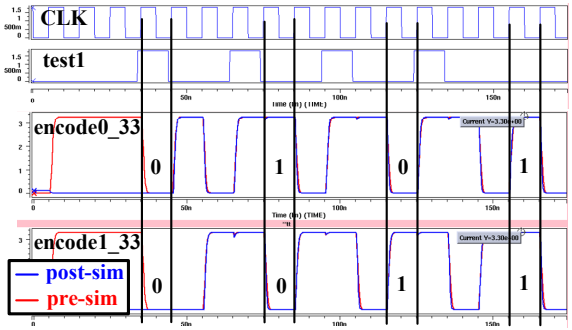

Fig. 9. Single island test mode at corner TT, 25°C.

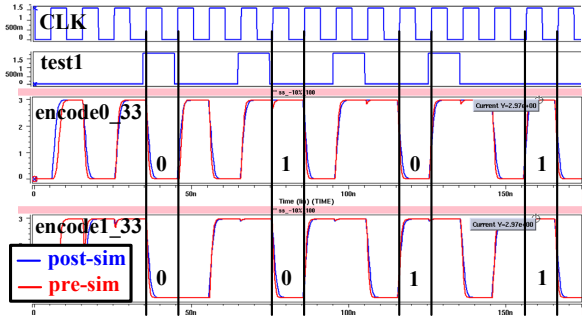

Fig. 10. Single island test mode at corner SS, 100°C.

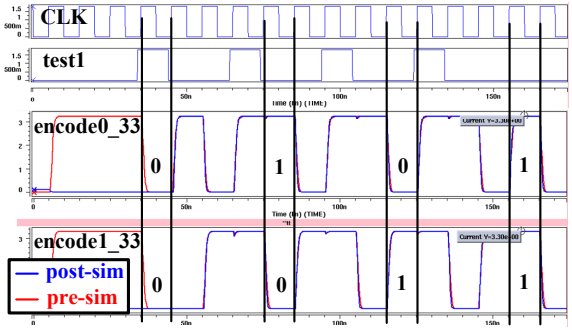

Fig. 11. Single island test mode at corner FF, -20°C.