A High Performance Current-Balancing Instrumentation Amplifier for ECG Monitoring Systems

Chia-Hao Hsu, *Student Member, IEEE,* Chi-Chun Huang, *Student Member, IEEE,*
Kian Siong Lim, Wei-Chih Hsiao, and Chua-Chin Wang†, *Senior Member, IEEE*

***Abstract*—A high command-mode rejection ratio (CMRR) and low input referred noise instrumentation amplifier (IA) is presented for ECG applications. A high pass filter (HPF) with a small-G_m OTA using a current division technique is employed to attain small transconductance, which needs only a small capacitor in the HPF such that the integration on silicon is highly feasible. The proposed design is carried out by TSMC (Taiwan Semiconductor Manufacturing Company) standard 0.18 μm CMOS technology. CMRR is found to be 127 dB and input referred noise is merely 0.278 according to the simulation results.**

***Index Terms*—CMRR, instrumentation amplifier, ECG, high pass filter**

I. Introduction

Signal sampling is one of the critical challenges in biomedical systems. Biomedical signals usually have small amplitude and low frequency, e.g., only a few μ volts and $\leq$ 1 KHz. Moreover, common-mode signal might be larger than that of the biomedical signals. Therefore, high common-mode rejection ratio (CMRR) is required in any instrumentation amplifier (IA) to faithfully sense the weak biomedical signals. Thus, a biomedical signal processing system usually consists of a sensor, an IA, a low-pass filter, a sample and hold (S/H), and an analog-to-digital convertor (ADC), as shown in Fig. 1 [1]. [2] was the first integrated IA without any additional trimmed component to provide a high CMRR. The IA in [2] is based on a current balancing technique using two input pairs to balance the differential currents. The gain of the IA is defined by the ratio of two resistors namely R_{gain} and R_{scale} in [2]. By using the current balancing technique, several later IA investigations, e.g., [3], [4], were further proposed to add a high pass filter to remove the DC offset of the sensor such that the CMRR was improved.

Lately, portable Electrocardiogram (ECG) monitoring devices are welcomed by many patients and their family for the purpose of home care. In an ECG system, IA is an important element to read the ECG signals. Several prior IAs used an HPF with an off-chip capacitor to meet the demands of an ECG system [3], [4], but they caused the increase of area cost. By contrast, this paper proposes a high performance IA with a higher CMRR and a lower input referred noise without any off-chip capacitor. The capacitor in the HPF is reduced drastically by a current division voltage-to-current converter technique such that it can be integrated on silicon.

†Prof. C.-C. Wang is with the Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan 80424. (e-mail: ccwang@ee.nsysu.edu.tw). He is the contact author.

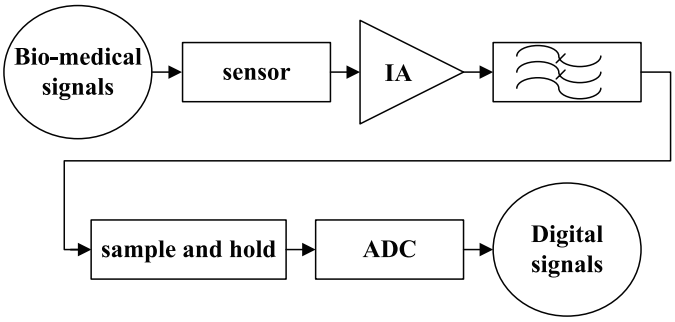

Fig. 1. Block of a biomedical signal processing system

II. Current-Balancing Instrumentation Amplifier

Prior IAs typically consist of three operational amplifiers and several matching resistors to achieve high CMRR, as shown in Fig. 2. There are two major drawbacks in this type of IAs: high power consumption and too many resistors, which reduce the battery operating time and increase the area cost, respectively.

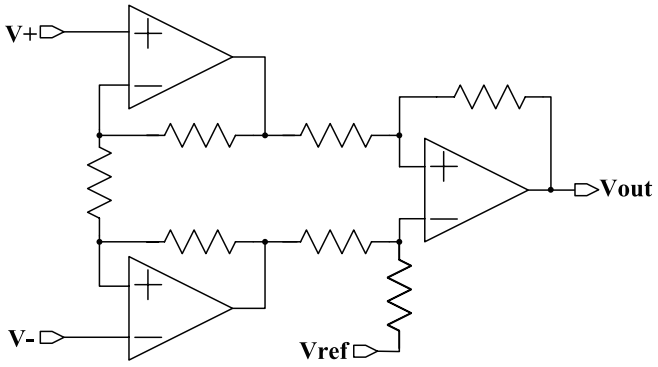

Fig. 2. Structure of a convention IA

In this paper, the proposed IA is based on a current-balancing technique [4] and an operation transconductance amplify (OTA) with small G_m to achieve high CMRR and small transconductance of HPF. Fig. 3 shows the schematic

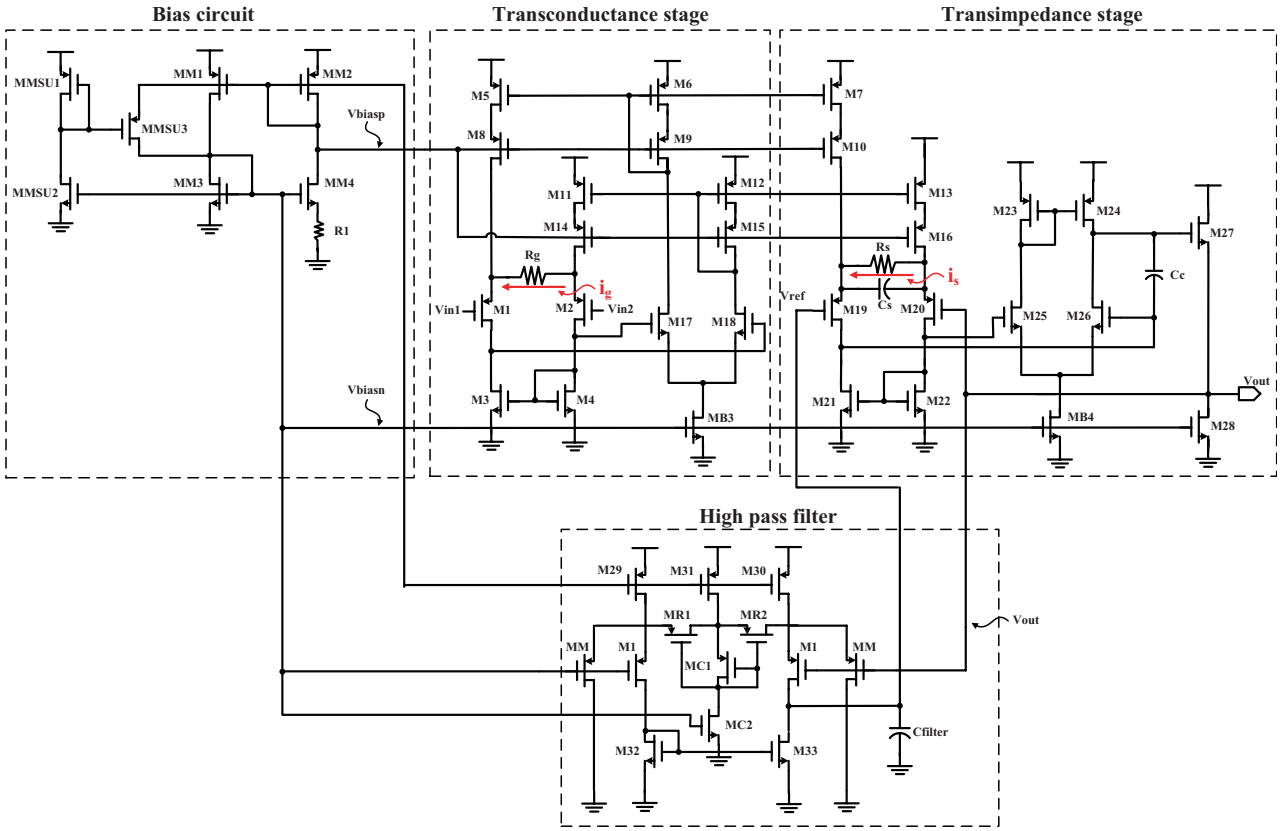

Fig. 3. Schematic diagram of the proposed IA

of the proposed IA, comprising a Bias circuit, a Transconductance stage, a Transimpedance stage, and a High pass filter. The differential input voltage, Vin1 and Vin2, are converted into a differential current, i_g, flowing across resistor R_g in Transconductance stage. By the current mirror composed of M5 - M16, i_g is mirrored to be i_s in Transimpedance stage. Then, the mirror current, i_s, is converted into a voltage by flowing across resistor R_s. The relation of i_g and i_s is expressed as Eqn. (1). Therefore, the differential gain of the current-balancing IA is determined by the ratio of Rs to Rg.

$$A_d = \frac{Vout - Vref}{Vin2 - Vin1} = \frac{i_s \cdot Rs}{i_g \cdot Rg} = \frac{Rs}{Rg} \quad (1)$$

A. Transconductance stage and Transimpedance stage

A typical current-balancing IA is composed of a Transconductance stage circuit and a Transimpedance stage circuit [4]. However, if the reliability and the area cost are taken into consideration, the resistors, Rg and Rs, and capacitors, Cs and Cc, must be all integrated on silicon.

By the specification of ECG in [3], the CMRR must be larger than 90 dB, and the input referred noise voltage must be lower than 10 μV RMS. Besides CMRR and integration requirements, power supply rejection ratio (PSRR) is also highly needed in IA designs. A cascade current mirror was then used to resolve this problem in [4].

The ECG frequency band is located between 0.2 Hz and 200 Hz. Then, we can derive the -3 dB pole by Eqn. (2).

$$f_{3dB} = \frac{1}{2\pi RsCs} \quad (2)$$

Therefore, if Rs and f_{3dB} are, respectively, given 500 kΩ and 200 Hz, Cs is estimated to be 1.6 nF. Regarding -3 dB zero at 0.2 Hz, it will be derived in the following text.

B. High pass filter

High pass filter is designed to reject the low frequency noise from human body. An approach, namely G_m-C filter, was presented in [5], [6], as shown in Fig. 4. The G_m-C filter can attain a sufficiently large impedance without resistance to reduce the area cost.

Therefore, the HPF in Fig. 3 is replaced with the G_m-C filter, where V_{ref} is coupled to the gate of M19. However, though the G_m-C filter can achieve the low -3 dB cut-off frequency at 0.2 Hz in the feedback path from Vout to HPF, Cfilter is too large to be integrated on chip. A zero is expressed in Eqn. (3), which is used to implement a -3 dB zero at 0.2 Hz. According to Eqn. (3), the transconductance, G_m, is directly proportional to Cfilter. We then are able to reduce Cfilter by tuning G_m smaller.

$$f_{low} = \frac{G_m}{2\pi Cfilter} \quad (3)$$

An OTA usually has very smaller G_m. For instance, an OTA in [7] is called small-G_m OTA. This small-G_m OTA is based

on a current division voltage-to-current converter technique, as shown in Fig. 5. The source-drain voltage of MC1 is adjusted by tuning MC1's size such that MR1 and MR2 are biased in linear region. The differential voltage, $(V_1 - V_2)$, is converted to currents, respectively flowing across MR1 and MR2. Notably, the sizes of MM_1 and MM_2 must be much larger than M1_1 and M1_2 (more than 10 times) such that the divided currents of M1_1 and M1_2 are smaller than the currents of MM_1 and MM_2. The current path from M1_2 to M33 is biased at Vo, which is coupled to the gate of M19. The small-signal transconductance is expressed in Eqn. (4), where M is the gate width ratio of MM_2 to M1_2 as well as the gate width ratio of MM_1 to M1_1, and g_oMR is the conductance of MR1 and MR2, μ_n is the mobility of carrier in channel, C_{ox} is the gate-channel capacitance, and V_T is the threshold voltage, V_G is the gate voltage, and V_{CM} is the the common-mode voltage. W and L are, respectively, the width and length of the gate of MR1 and MR2.

$$G_m = \frac{g_o MR}{M+1} = \frac{1}{M+1}(\mu_n C_{ox}\frac{W}{L}(V_G - V_{CM} - V_T)) \quad (4)$$

According to Eqn. (4), G_m can be reduced by the increasing M and the reducing $(V_G - V_{CM} - V_T)$. In Fig. 3, High pass filter comprises the small-G_m OTA and Cfilter. Thus, given that the size of MM_1 and MM_2 is far larger than that of M1_1 and M1_2, the transconductance of the small-G_m OTA will be very much reduced. Therefore, Cfilter is also reduced.

C. Bias circuit

Bias circuit is composed of a beta-multiplier and a start-up circuit, which is used to generate two bias voltages, Vbiasp and Vbiasn, to bias the proposed IA. The start-up circuit is composed of MMSU1, MMSU2, and MMSU3 in Fig. 3 to set the Bias circuit in the normal operation region, where it will not affect the beta-multiplier operation. By carefully tuning of the sizes of MM1-MM4 and R1, the bias voltages, Vbiasp and Vbiasp, are 1.2 V and 0.5 V, respectively.

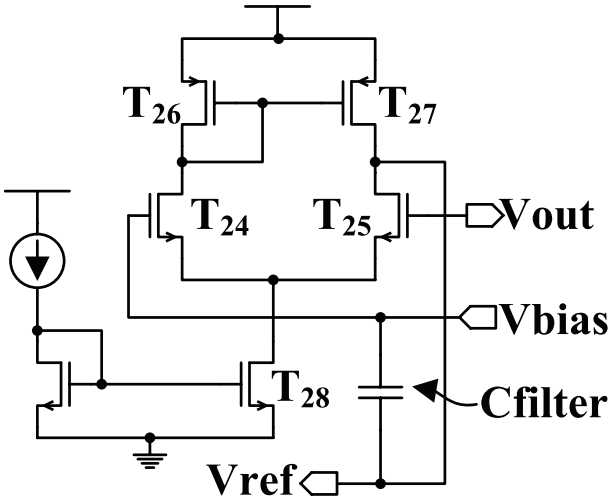

Fig. 4. Schematic diagram of G_m-C filter

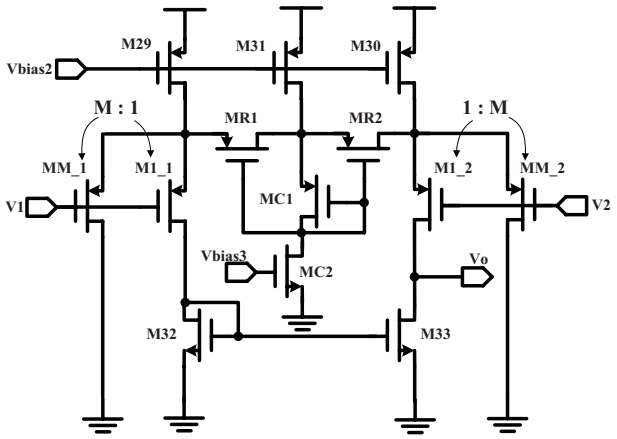

Fig. 5. Schematic of small-G_m OTA

III. Implementation and Simulation

TSMC (Taiwan Semiconductor Manufacturing Company) standard 0.18 μm CMOS technology is adopted to carry out the proposed IA. Fig. 6 shows the layout of the proposed IA design. The chip area of the proposed IA is 758 $\times$ 377 μm^2. By using HSPICE, the worst-cast result of the all-PVT post-layout simulations is shown in Fig. 7. The gain response, which is located between 0.2 Hz $\sim$ 200 Hz and the -3 dB pole and -3 dB zero, is found around 45 dB. The CMRR response is around 127 dB in Fig. 8. The input referred noise response is 0.278 μV in Fig. 9. The PSRR is 65 dB. The input common-mode range (ICMR) is 0.45 V $\sim$ 1 V. The specification of the proposed IA is tabulated in Table I.

Table. II shows the comparison with several prior works. The proposed IA has the highest CMRR and the lowest input referred noise. Moreover, the proposed IA does not require any off-chip capacitor. Therefore, the proposed instrumentation amplifier is considered as a better solution for ECG systems.

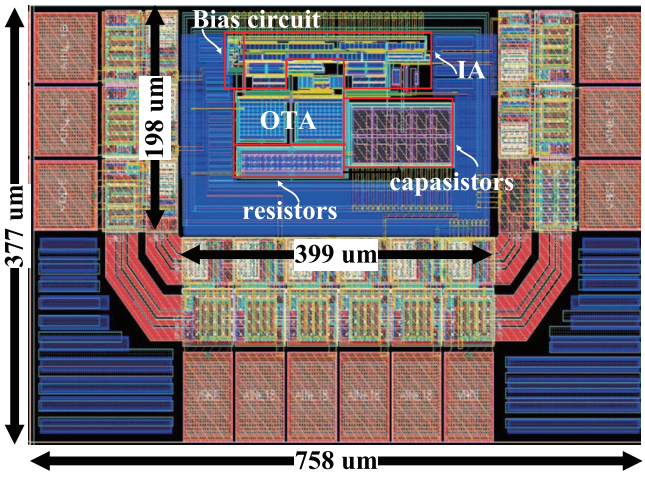

Fig. 6. The layout diagram of the proposed IA

IV. Conclusion

A high performance current-balancing instrumentation amplifier for ECG monitoring systems is presented in this paper.

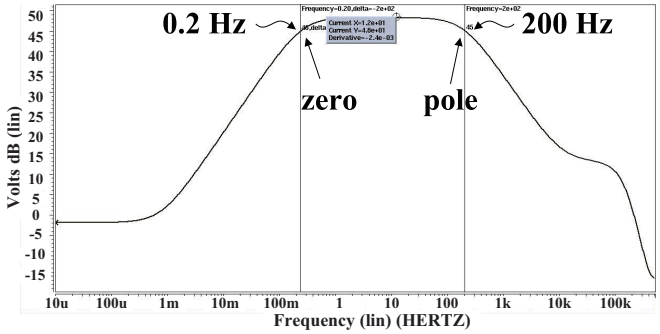

Fig. 7. Gain response of the proposed IA

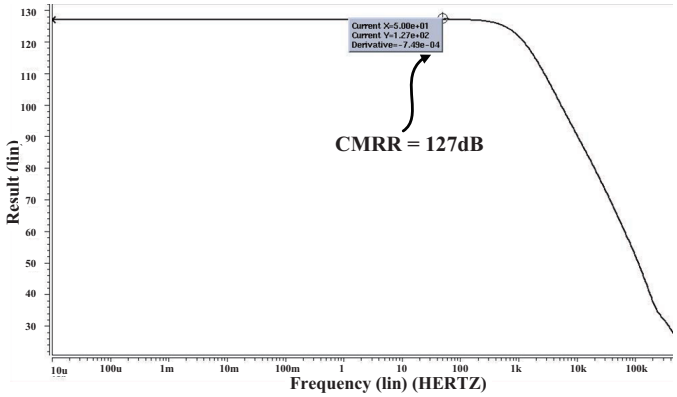

Fig. 8. CMRR response of the proposed IA

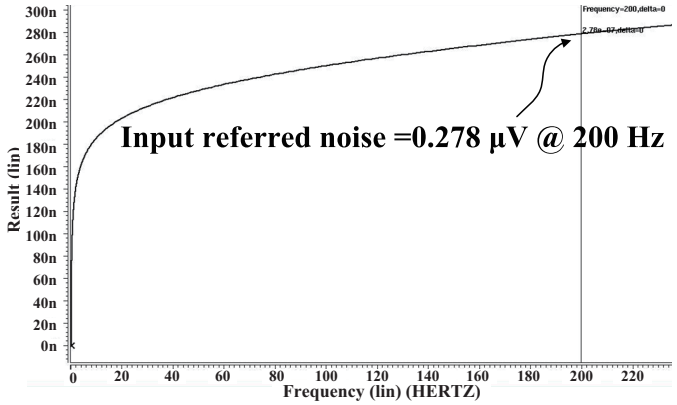

Fig. 9. Input referred noise response of the proposed IA

TABLE I
SPECIFICATION OF THE PROPOSED IA

DC offset	0.3mV
PSRR	65 dB
ICMR(V)	0.45 $\sim$ 1
Bandwidth	0.2 $\sim$ 200 Hz
Area	758 $\times$ 377 μm^2

TABLE II
COMPARISON WITH SEVERAL PRIOR WORKS

	[3]	[8]	[9]	[10]	Ours
Technology (μm)	0.35	0.18	0.18	0.35	0.18
Power supply (V)	3.3	1.8	1	3	1.8
CMRR (dB)	100	80	124	110	127
Gain (dB)	55	40	46	50	45
Power (μW)	72.6	3.3	165	4.9	138
Input referred noise (RMS)(μV)	6	1.5	2.8769	n/a	0.278
Year	2005	2007	2008	2008	2009

The proposed instrumentation amplifier circuit uses a small-G_m OTA in a high pass filter. The capacitor is greatly reduced and feasibly intergraded on chip. Compared with several prior works, the proposed design attains highest CMRR and lowest input referred noise.

ACKNOWLEDGEMENT

This investigation is partially supported by National Science Council under grant NSC 96-2628-E-110-19-MY3 and National Health Research Institutes under grant NHRI-EX98-9732EI. The authors would like to express their deepest gratefulness to CIC of NSC for their thoughtful chip fabrication service.

REFERENCES

[1] H.-C. Chow and J.-Y. Wang, "High CMRR instrumentation amplifier for biomedical applications," *9th Int. Symp. on Signal Processing and Its Applications*, pp. 1-4, Feb. 2007.

[2] H. Krabbe, "A high-performance monolithic instrumentation amplifier," *IEEE Int. Solid-State Circuits Conf.*, vol. 14, pp. 186-187, Feb. 1971.

[3] M. Shojaei-Baghini, R. K. Lal, and D. K. Sharma, "A low-power and compact analog CMOS processing chip for portable ECG recorders," *Asian Solid-State Circuits Conf.*, pp. 473-476, Nov. 2005.

[4] R. Martins, S. Selberherr, and F. A. Vaz, "A CMOS IC for portable EEG acquisition systems," *IEEE Tran. on Instrumentation and Measurement*, vol. 47, no. 5, pp. 1191-1196, Oct. 1998.

[5] H. Wu, and Y.-P. Xu, "A low-voltage low-noise CMOS instrumentation amplifier for portable medical monitoring systems," *The 3rd Int. IEEE-NEWCAS Conf.*, pp. 295-298, June. 2005.

[6] C. Nanda, J. Mukhopadhyay, D. Mandal, and S. Chakrabarti, "A CMOS instrumentation amplifier with low voltage and low noise for portable ECG monitoring systems," *IEEE Int. Conf. on Semiconductor Electronics*, pp. 54-58, Nov. 2008.

[7] J. Silva-Martinez and S. Solis-Bustos, "Design considerations for high performance very low frequency filters," in *Proc. of IEEE Inte. Symp. on Circuits and Systems*, vol. 2, pp. 648-651, June 1999.

[8] T. Denison, K. Consoer, W. Santa, A.-T. Avestruz, J. Cooley, and A. Kelly, "A 2 μW 100 nV/rtHz chopper-stabilized instrumentation amplifier for chronic measurement of neural field potentials," *IEEE J. of Solid-State Circuits*, vol. 42, no. 12, pp. 2934-2945, Dec. 2007.

[9] C. Nanda, J. Mukhopadhyay, D. Mandal, and S. Chakrabarti, "A CMOS instrumentation amplifier with low voltage and low noise for portable ECG monitoring systems," *IEEE Int. Conf. on Semiconductor Electronics*, pp. 54-58, Nov. 2008.

[10] J. T. Li, S. H. Pun, P. U. Mak, and M. I. Vai, "Analysis of op-amp power-supply current sensing current-mode instrumentation amplifier for biosignal acquisition system," *30th Annual Int. Conf. of the IEEE Engineering in Medicine and Biology Society*, pp. 2295-2298, Aug. 2008.