A $\frac{1}{2}\times$VDD to $3\times$VDD Bidirectional I/O Buffer Using 0.18-μm 1.8-V CMOS Technology

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***Abstract*—This paper presents a wide-range I/O buffer able to transmit and receive signals of 0.9/1.2/1.8/3.3/5.0 V by using a typical 0.18 μm CMOS process. Dynamic gate bias circuit of the proposed I/O buffer is composed of two voltage converters, an EOS protector and glue logics. A High voltage detector detects voltage level of VDDIO different supply voltage and then generates several bias voltages to Dynamic gate bias circuit, which then provides appropriate bias voltages to transistors of Output stage. The Output stage consists of triple stacked MOS transistors to avoid the gate-oxide overstress and hot-carrier degradation. A Floating N-well circuit in the proposed I/O buffer is used to remove undesirable leakage current paths. The maximum output speed of the proposed design is measured on silicon to be 50 MHz given VDDIO = 1.8 V.**

***Index Terms*—wide-range, I/O buffer, Floating N-well, Dynamic gate bias, mixed-voltage tolerant**

I. Introduction

With the rapid evolution of CMOS technology, supply voltage and feature size of chips are scaled down to reduce power consumption and area cost. However, the compatibility among chips is an interest problem when chips with different logic voltage levels are integrated in a system on a PCB. Conventional I/O buffers are no longer suitable in such a scenario. The Output stage of the traditional I/O buffer is typically composed of a PMOS and an NMOS. These I/O buffers suffer from hazards of gate-oxide overstress, hot-carrier degradation, and the undesirable leakage current paths when V_{PAD} is at high level (VDDH) [1], [5]. The gate-oxide overstress would cause the gate-oxide breakdown.

This paper proposes a fully wide-range I/O buffer which is implemented using a typical CMOS 0.18 μm process. To achieve Rx and Tx of mixed-voltage signals, a Dynamic gate bias generator is proposed, which is different from conventional voltage dividers [7]. The proposed Dynamic gate bias generator with low power dissipation provides five bias voltages to the Output stage. The proposed I/O buffer is proved on silicon to transmit and receive the signals with voltage levels of 0.9/1.2/1.8/3.3/5.0 V, i.e., $\frac{1}{2}\times$VDD $\sim$ $3\times$VDD. Dynamic gate bias generator circuit also provides appropriate gate biases to the gate drives of output PMOSs. Moreover, the proposed I/O buffer does not need thick-oxide devices such that the fabrication cost is reduced.

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II. $\frac{1}{2}\times$VDD $\sim$ $3\times$VDD Bidirectional I/O Buffer

The block diagram of the proposed wide-range I/O buffer is shown in Fig. 1. It is composed of a Pre-driver, a Dynamic gate bias generator, a High voltage detector, a PAD voltage detector, an Output stage, a Floating N-well circuit, a Gate-tracking circuit, and an Input stage. Notably, VDDIO stands for the signal voltage level to be transmitted or received. The details of these sub-circuits are revealed in the following text.

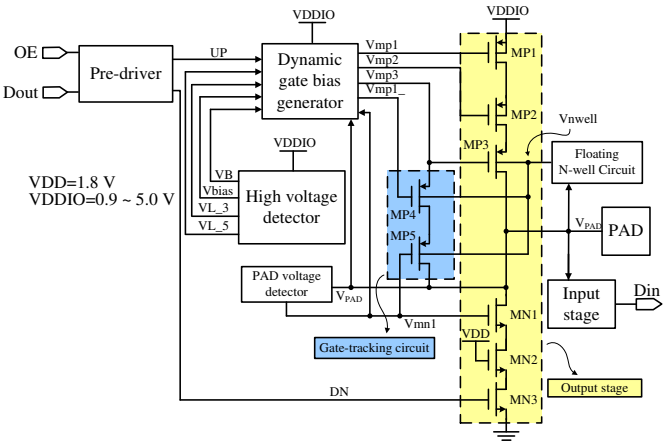


Fig. 1. Schematic of the proposed wide-range I/O buffer

A. Pre-driver

Pre-driver is a digital CMOS logic circuit. OE determines which of the transmitting mode (OE = 1.8 V) or receiving mode (OE = 0 V) is selected. In Tx mode, when Dout = 0 is transmitted, UP = 1 to enable Dynamic gate bias generator circuit to generate bias voltage, Vmp1, which turns off the Output stage's MP1. Simultaneously, MN3 is turned on by DN = logic 1. On the contrary, when Dout = 1 to be transmitted, Dynamic gate bias generator circuit generates corresponding bias voltages to turn on the PMOS transistors of Output stage. MN3 is turned off simultaneously. In Rx mode, the signal Dout is irrelevant. The Output stage is shut off.

B. Dynamic gate bias generator

The gate drives of MP1, MP2, and MP3 shown in Fig. 1 must be biased at certain appropriate voltage levels to ensure the gate-oxide reliability in different scenarios depending on the combination of Tx/Rx modes and VDDIO. We propose a Dynamic gate bias generator is composed of two level converters (VLC1 and VLC23), an electrical overstress

protector (EOS), and digital logic gates, as shown in Fig. 2. The details of VLC1, VLC23, and EOS protector therein are given as follows.

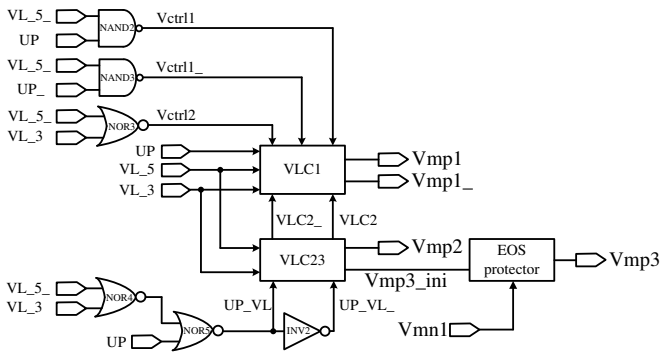


Fig. 2. Schematic of Dynamic gate bias generator

1) VLC23: Referring to Fig. 3 (a), VDDIO_VLC voltage depends on VDDIO. When VDDIO = 5 V, MP206 is turned on and then VDDIO_VLC will be biased to 3.3 V (= VB - V_{TH_MN214}), where VB is a bias generated by High voltage detector which will be described later, and V_{TH_MN214} is the threshold voltage of MN214. Therefore, VDDIO turns off MP207 via MN214 and MP208. When VDDIO = 0.9/1.2/1.8/3.3 V and VL_5 = 1.8 V, MN216 is turned on. The gate drive of MP207 will be biased to 0 V, and then VDDIO_VLC = 1.8 V.

When VDDIO = 5 V, UP = 0 V and if UP_VL = 1.8 V, MN205 is turned off because VL_5 = 0 V. Vmp3_ is discharged through MP204, MN210 and MPMN212, which causes MP201 to be turned on, and Vmp3_ini = VLC2 = 3.3 V. When Vmp3_ini = 3.3 V, MN202 will be turned on, and Vmp3_ is pulled up to 1.8 V. Simultaneously, Vmp2 will be pulled to 3.3 V by MN217 and MP209. VLC2_ is pulled to 0 V by MN212 and MN210.

On the other hand, when UP = 1.8 V and UP_VL = 0 V, Vmp3_ini will be drawn to 1.8 V. Vmp3_ will be pulled to 3.3 V. So is VLC2_. Vmp2 will be pulled to 3.3 V, and VLC2 will be pulled to 0 V. Because the gate drive of MP205 is 3.3 V, which is larger than its drain to source voltage drop, MP205 is turned off to isolate Vmp1 and Vmp2.

When VDDIO = 3.3 V, VL_5 = 1.8 V, and UP_VL = 0 V. Vmp3_ is pulled down to 0 through MN204, MN206 and MN208 such that VDDIO_VLC = 1.8 V. Vmp3_ini is pulled up to 1.8 V through MP201. Vmp2 is also 1.8 V. MP201 is turned off.

When VDDIO = 1.8/1.2/0.9 V and UP = 0 V, UP_VL = 1.8 V, Vmp3_ini is pulled down to 0 through MN203, MN205 and MN207. Therefore, MP202 is turned on, and VDDIO_VLC will be 1.8 V. Vmp3_ becomes 1.8 V and Vmp2 is 0 V. When UP = 1.8 V, UP_VL is biased at 0 V, Vmp3_ = 0 V, Vmp3_ini will be pulled to 1.8 V through MP201 and Vmp2 will be pulled to 1.8 V via MP205. Because VL_5 is equal to 1.8 V, MP210 is turned off.

2) EOS: EOS circuit is shown in Fig. 3 (b). In Tx mode, when VDDIO = 5 V, OE =1.8 V, VL_5 = 0 V, the gate drive of MP5 (Vgate1) and MP4 (Vgate2) are equal to UP_. MP5 and MP4 are turned on, Vmp3 = Vmp3_ini. It is the bias to MP3 in Fig. 1 without gate-oxide overstress. When VDDIO = 3.3/1.8/1.2/0.9 V, OE =1.8, and VL_5 = 1.8 V, Vgate1 and Vgate2 are biased at 0 V. MP4 and MP5 will be turned on, and then Vmp3 = Vmp3_ini. In Rx mode, OE = 0 V, MN7 and MP7 are turned off, Vgate1 and Vgate2 are biased at V_{PAD}. Notably, Vmn1 provided by PAD voltage detector will be biased at 3.3/2 V for V_{PAD} = 5.0/3.3 V, respectively. Vmp3 will be pulled up to 5.0/3.3 V. Therefore, MP6 is turned on, Vgate1 is charged to 5.0/3.3 V to turn off MP5. At the same time, Vgate2 is pulled at 3.3/2 V through MN6 such that MP4 will be turned off to avoid gate-oxide overstress. When V_{PAD} = 0/0.9/1.2/1.8 V, Vgate1 and Vgate2 are biased at 0/0.9/1.2/1.4, respectively, such that MP4 and MP5 are turned on to pass the bias voltage, 1.8 V, to Vmp3.

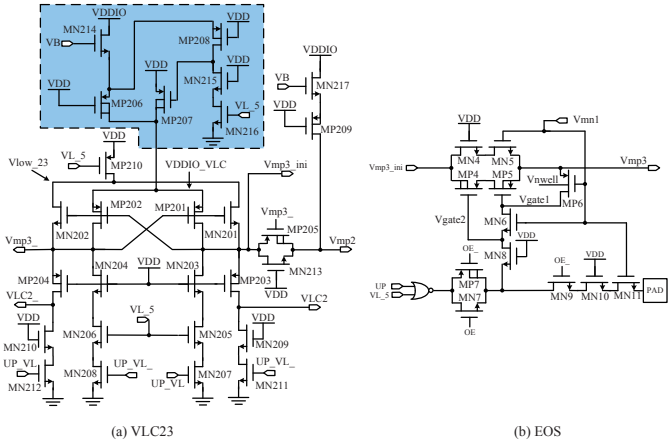


Fig. 3. Schematics of VLC23 and EOS

3) VLC1: Fig. 4 (a) shows the schematic of VLC1. When VDDIO = 5.0 V and UP = 0 V, Vctrl1_ and VLC2_ are biased at 0 V due to VL_5 = VL_3 = 0 V. MN310 and MN308 are turned off. Vmp1 must be discharged to VDD to avoid overstress on MP303 and MN313. MP305 and MP307 are both on due to Vctrl_ = VLC2_ = 0 V such that the source of MN313 is biased at VDD. MN313 and MP303 are also on by Vbias. Therefore, Vmp1 is biased at VDD. Then, MP302 will be turned on, and Vmp1_ will be pulled at 5.0 V. Therefore, Vmp1 is pulled up to 3.3 V. When UP = 1.8 V, Vctrl1 and VLC2_ are both equal to 0, Vmp1 will be pulled to 5.0 V and Vmp1_ = 3.3 V.

When VDDIO is 3.3 V and UP is 0 V, Vctrl1, Vctrl2 and Vctrl1_ are all biased at 1.8 V. VL_3 becomes 0 V such that MN308 is turned off. Vmp1 is discharged through MN311, MN309, MN313 and MN303. MP302 is turned on. Vmp1_ will be pulled up to 3.3 V. Vmp1 will be pulled down to 1.8 V though MP312, MP310, and MN301. If UP = 3.3, then Vmp1 will be pulled up to 3.3 V, and Vmp1_ will be pulled down to 1.8 V.

When VDDIO = 1.8/1.2/0.9 V and UP = 0 V, Vctrl1 and Vctrl1_ are biased at 1.8 V. Vmp1 will be discharged to 0 V through MN311, MN309, MN307, MN305 and MN303 such that MP302 is turned on. Vmp1_ will be pulled to 1.8/1.2/0.9 V, respectively. When UP = 1.8, Vmp1_ will be discharged

to 0 V, and Vmp1 is pulled up to 1.8/1.2/0.9 V, respectively. VL_3 is equal to 1.8 V in such a scenario such that MP312 will be turned off.

C. High voltage detector

The schematic of the High voltage detector is shown in Fig. 4 (b). It detects the voltage level of VDDIO to see if it is larger than 1.8 V or 3.3 V. Two corresponding signals, VL_5 and VL_3, are generated to Dynamic gate bias generator. A close loop structure without any start-up circuit is utilized in this circuit. In short, when VDDIO = 5.0/3.3/1.8/1.2/0.9 V, VL_5 is 0/1.8/1.8/1.8/1.8 V, and VL_3 is 0/0/1.8/1.8/1.8 V, respectively.

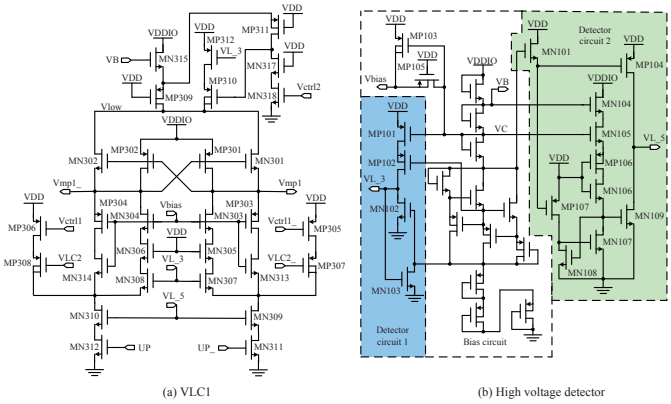


Fig. 4. Schematics of VLC1 and High voltage detector

D. PAD voltage detector

Fig. 5 (a) shows the proposed PAD voltage detector. When V_{PAD} = 5.0 V, Vx $\cong$ 4.2 V. Vmn1 is then pulled up to 3.3 V through MN401 and MP404. Vy is equal to 3.3 V such that MP405 is turned off to avoid the gate-oxide overstress of MN1 of the Output stage shown in Fig. 1.

If V_{PAD} = 3.3 V, Vx is 2.7 V. Vmn1 is biased at 2.2 V through MN401 and MP404. Vy is approximately 2.0 V and MP405 is turned off.

When V_{PAD} is 1.8/1.2/0.9 V, Vy is smaller than 1.8 V. Vmn1 is biased at 1.8 V through MP405. When V_{PAD} is 0 V, Vx and Vy are discharged through MP401 and MP402, to avoid gate-oxide overstress. Vmn1 is pulled to 1.8 V through MNP405.

E. Output stage

Stack PMOS and stack NMOS are adopted to prevent gate-oxide overstress. The gates of MP1, MP2, MP3, MN1, and MN3 in the Output stage circuit, as shown in Fig. 1, are biased at appropriate voltages by the Pre-driver circuit, Dynamic gate bias generator, and PAD voltage detector.

F. Floating N-well circuit

The Floating N-well circuit is composed of MP503, MN501, MP502 and MP501, as shown in Fig. 5 (b). It provides the N-well voltage of MP3 to prevent the leakage current path formed by the parasitic P+/N-well diode. As stated, V_{PAD} = 5.0/3.3 V, Vmn1 =3.3/2 V. Thus, MP501 and MP503 are turned on. MP502 and MN501 are turned off. Vnwell is equal to 5.0/3.3 V, respectively, such that the parasitic diode of MP3 no longer exists. Besides, since Vmn1 = 3.3/2 V, all transistors of the Output stage have no gate-oxide overstress. When V_{PAD} = 0/0.9/1.2/1.8 V, MP502 and MN501 will be turned on. MP503 and MP501 will be turned off. Therefore, Vnwell is pulled to 1.8 V through MP502, and Vmn =1.8 V.

G. Gate-tracking circuit

Gate-tracking circuit consists of MP4 and MP5, as shown in Fig. 1. It prevents the leakage current path through MP3 in Rx mode. In the Rx mode, if VDDIO = 5.0/3.3 V and logic 1 is received, Vmp1_ = 5.0/3.3 V to turn off MP4. Vmp3 is then not affected by V_{PAD}. In the Tx mode, if VDDIO = 5.0/3.3 V and Vmp1_ = 3.3/1.8 V, MP4 will be turned on to equalize the gate voltage of MP3 and V_{PAD}. Thus, the leakage current through MP3 will not exist. The gate-oxide overstress of MN4 and MP5 is also eliminated.

H. Input stage

Input stages have been reported to be able to receive the input signal with a voltage level higher than the supply voltage VDD. It can accept the voltage from 0.9 V to 5.0 V by tuning transistor aspects. MN12 and MN13 in the Input stage of the proposed I/O as shown in Fig. 5 (c) isolate any unexpected high voltage at PAD. When V_{PAD} is 5.0/3.3 V, Vi1 would be close to 1.4 V, the gate-oxide overstress hazard of MN14 is eliminated. When V_{PAD} is logic 1, Vi2 becomes 0 V to turn on MP11. MP11 pulls Vi1 up to 1.8 V to ensure MP9 is turned off. If in Tx mode, OE = 1.8 V. MP8 and MN15 are turned off. MP10 is then turned on such that Vi2 is pulled up to 1.8 V to turn off MP11. The leakage is avoided.

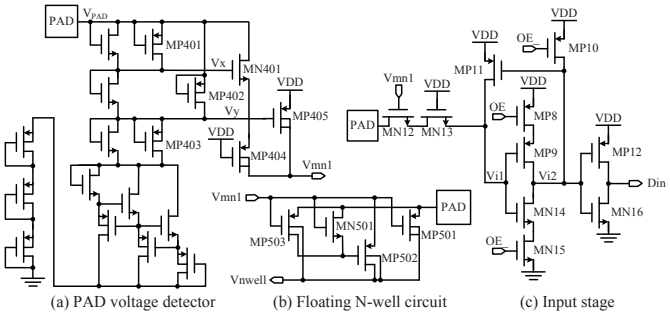


Fig. 5. Schematics of PAD voltage detector, Floating N-well circuit, and Input stage

III. Implementation and Measurement

TSMC (Taiwan Semiconductor Manufacturing Company) standard 0.18 μm CMOS technology is adopted to carry out the proposed I/O buffer. Fig. 6 is the die photo of the proposed design. Three proposed I/O buffers are included in the same die for testing consideration. Vmp1, Vmp2, Vmp3 and Vnwell are respectively output for measurement and observation. Guard rings are drawn to avoid latch up problems. The area of the proposed I/O buffer is 65 $\times$ 628 μm^2.

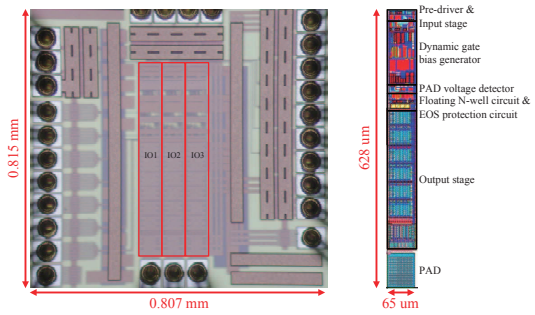
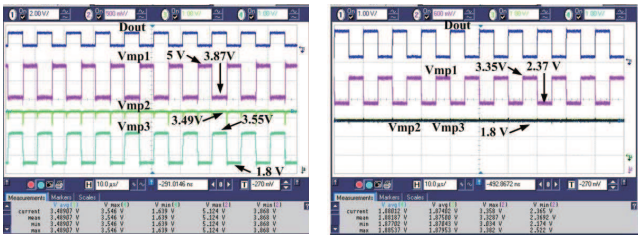


Fig. 6. The die photo of the proposed I/O buffer

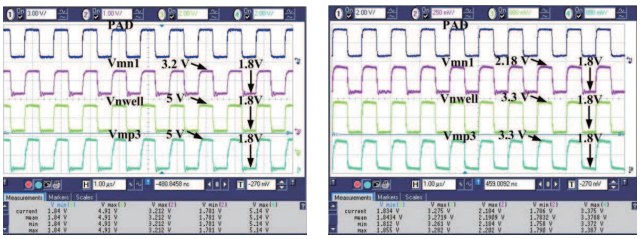
Fig. 7 (a) and (b) illustrate the measurement results of Vmp1, Vmp2, Vmp3 and Dout on silicon in the Tx mode for VDDIO = 5.0/3.3 V, respectively. For VDDIO = 5.0 V, Vmp1 is biased at 3.87/5.0 V for transmitting logic 1/0, respectively, as shown in Fig. 7 (a). Moreover, Vmp2 and Vmp3 are biased at 3.49 V and 1.8/3.55 V, respectively. Therefore, the gate-oxide reliability for MP2 and MP3 is ensured. For VDDIO = 3.3 V, Vmp1, Vmp2 and Vmp3 are biased at the expected voltages, respectively, as shown in Fig. 7 (b). On the other hand, when VDDIO = 1.8/1.2/0.9 V, Vmp1, Vmp2 and Vmp3 are biased at the expected voltages, respectively.

Fig. 8 (a) and (b) show V_{PAD}, Vmp1, Vnwell, and Vmp3 in Rx mode for VDDIO = 5.0/3.3 V given 5.0 V and 3.3 V signals at the PAD, respectively. Referring to Fig. 8 (a), Vmn1 is biased at 1.8/3.2 V, Vmp3 is biased at 1.8/5.0 V to turn off MP3. Vnwell is pulled high when the input signal at the PAD is at 5.0 V to eliminate the leakage current path through the parasitic diode. Similarly, for VDDIO = 3.3 V, N-well is biased at 1.8/3.3 V to turn off the leakage current path as well. Vmn1 is biased at 1.8/2.18 V, Vmp3 is biased at 1.8/3.3 V to turn off MP3.



(a) VDDIO = 5.0 V (b) VDDIO = 3.3 V

Fig. 7. Measured Vmp1, Vmp2, Vmp3 and Dout in Tx mode



(a) VDDIO = 5.0 V (b) VDDIO = 3.3 V

Fig. 8. Measured V_{PAD}, Vmp1, Vnwell, and Vmp3 in Rx mode

The maximum speed of the proposed I/O buffer is 50 MHz with a 19 pF load (the wire load + input capacitance of the OSC probe). Table. I shows the comparison with several prior works. The proposed I/O buffer provides the wide operating voltage (0.5×VDD ∼ 3×VDV).

TABLE I
COMPARISON WITH SEVERAL PRIOR WORKS

	[2]	[3]	[4]	Ours
# of voltage modes	2	1	3	5
Tx VDDH	No	Yes	Yes	Yes
Tx VDDL	No	No	Yes	Yes
Rx VDDH	Yes	No	Yes	Yes
Rx VDDL	No	No	Yes	Yes
Max. operating voltage	3 × VDD	3.3 × VDD	1.5 × VDD	3 × VDD
Min. operating voltage	VDD	3.3 × VDD	0.54 × VDD	0.5 × VDD
Output stage	1P1N	2P2N	2P2N	3P3N
Thick-oxide	No	Yes	No	No
Normal voltage (VDD)	1.0 V	1.0 V	3.3 V	1.8 V
Process (μm)	0.13	0.13	0.35	0.18
Area (mm^2)	0.0105	0.0316	0.0336	0.04082
Year	2006	2007	2008	2009

IV. Conclusion

A wide-range bidirectional I/O buffer with 0.9/1.2/1.8/3.3/5.0 V tolerant is proposed in this study. The proposed I/O buffer can transmit and receive the signals with voltage levels over $\frac{1}{2}$VDD ∼ 3VDD by using an extra supply voltage VDDIO. No thick-oxide devices are needed in this work. Dynamic gate bias provides appropriate control voltages for the gate drives of the stacked PMOS to ensure gate-oxide reliability. The static power consumption is merely 36 μW. Compared with several prior works, the proposed design attain the widest range.

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