A 0.9 V to 5 V Mixed-Voltage I/O Buffer Using NMOS Clamping Technique

Chua-Chin Wang†, *Senior Member, IEEE*, Jen-Wei Liu, and Ron-Chi Kuo

***Abstract*—A 0.9 V to 5 V (0.9/1.2/1.8/2.5/3.5/5 V) mixed-voltage I/O buffer with NMOS clamping technique is proposed. By using a dynamic gate bias generator to provide appropriate gate drive voltages for the output stage, the I/O buffer can transmit 3×VDD voltage level signal without gate-oxide overstress hazard. Besides, the leakage current effect is eliminated by adopting a floating N-well circuit. The maximum data rate is simulated to 140/120/120/120/80/40 Mbps for 5/3.3/2.5/1.8/1.2/0.9 V, respectively, with a given capacitive load of 10 pF.**

***Index Terms*—mixed-voltage-tolerant, I/O buffer, gate-traking circuit, gate-oxide reliability**

I. Introduction

In past several years, many mixed-voltage I/O buffers were reported to deal with the chip interface problems of different voltage levels [1]−[4]. However, most of them can only transmit and receive the signal with the voltage from VDD to 2×VDD. The compatibility with more advanced processes has been ignored. Therefore, a wide range I/O buffer able to simultaneously transmit and receive signal from $\frac{1}{2}$×VDD to 3×VDD is deemed as a total solution for these scenarios. To communicate the signal at 3×VDD, triple stacked transistors are used in the output stage to avoid the gate-oxide overstress. Notably, traditional gate-tracking circuit and floating N-well circuit can not be used directly due to the high voltage signal which is very close to 3×VDD. A protection voltage equal to VDDH−VDD (3.2 V) is required to ensure the gate-oxide reliability. The NMOS clamping technique without any power-consuming DC current path is employed to generate this protection voltage.

II. 0.9 V to 5 V Mixed-Voltage I/O Buffer

Fig.1 shows the block diagram of the proposed I/O buffer which is composed of a pre-driver, an input stage, an output stage, a dynamic gate bias generator, a floating N-well circuit, a V_{PAD} detector.

A. Output Stage

Since the supply voltage of the core circuits is 1.8 V in 0.18 μm CMOS process, the output stage must be realized with three stacked PMOS and NMOS for

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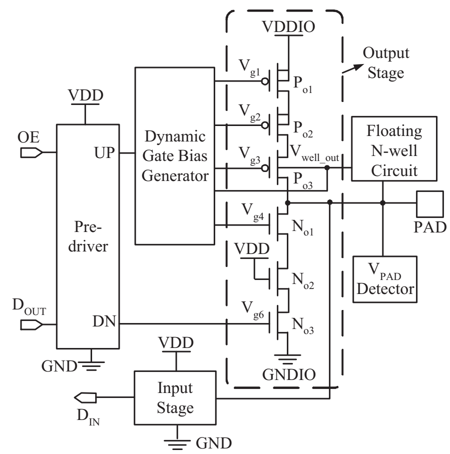

Fig. 1. Block diagram of the proposed mixed-voltage I/O buffer.

2×VDD<5 V<3×VDD, as depicted in Fig. 1. Besides, the appropriate gate voltages are needed for P_{o1}∼P_{o3} and N_{o1}∼N_{o3} to ensure the gate-oxide reliability and correct functions. The detailed operation of output stage is tabulated in Table I.

B. Pre-driver

The Pre-driver is a simple logic circuit to decode and pre-drive. When the voltage of control signal OE is at 1.8 V, the I/O buffer operates at the transmitting mode. The logic state of V_{PAD} is determined by D_{OUT}. On the other hand, when the I/O buffer is at the receiving mode, the voltage of control signal is given at 0 V. The receiving signal D_{IN} would be determined by V_{PAD}.

C. Input Stage

As shown in Fig. 2, MN604 and MN605 are added to prevent MP602 and MN601 from gate-oxide overstress, while MP605 is used to clamp V_{i1} at 1.8 V when logic 1 is received. MP601 and MN602 are turned off as well as MP604 is turned on to reduce power dissipation at the transmitting mode.

D. Dynamic Gate Bias Generator

The dynamic gate bias generator is composed of a VDDIO detector, V_{g1}, V_{g2}, V_{g3}, and V_{g4} generators. The details of each subcircuit will be analyzed in the following text.

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TABLE I
GATE VOLTAGES OF THE OUTPUT STAGE

	VDDIO (V)	V_{g1} (V)	V_{g2} (V)	V_{g3} (V)	V_{g4} (V)
RX	5	5	>3.2	$1.8/V_{PAD}$[a]	$1.8/V_{PAD}$[b]
	3.3	3.3	3.3	$1.8/V_{PAD}$[a]	$1.8/V_{PAD}$[b]
	2.5	2.5	2.5	$1.8/V_{PAD}$[a]	$1.8/V_{PAD}$[b]
	1.8	1.8	1.8	$1.8/V_{PAD}$[a]	$1.8/V_{PAD}$[b]
	1.2	1.2	1.8	$1.8/V_{PAD}$[a]	$1.8/V_{PAD}$[b]
	0.9	0.9	1.8	$1.8/V_{PAD}$[a]	$1.8/V_{PAD}$[b]
TX	5	>3.2/5	>3.2	>3.2/1.8	>3.2/1.8
	3.3	>1.5/3.3	>1.5	>1.5	1.8
	2.5	>0.7/2.5	>0.7	>0.7	1.8
	1.8	0/1.8	0	0	1.8
	1.2	0/1.2	0	0	1.8
	0.9	0/0.9	0	0	1.8

[a] Only when $V_{PAD} = 5$ V, $V_{g3} = V_{PAD}$.
[b] Only when $V_{PAD} = 5$ V, $V_{g4} > 3.2$ V.
[c] In RX or TX, $V_{well\_out} = 1.8/V_{PAD}$, and $V_{g5} = 1.8$ V
[d] In RX, $V_{g6} = 0$ V While in TX, $V_{g6} = 0/1.8$ V.

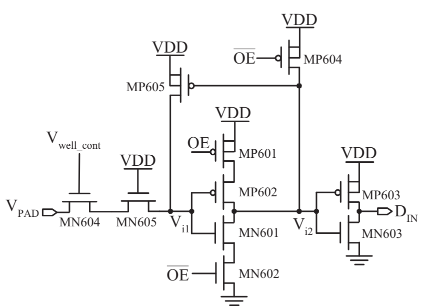

Fig. 2. Input stage circuit.

1) Bias Circuit and V_{PAD} Detector: Referring to Fig. 3, the bias circuit and V_{PAD} detector are both realized with a string of diode-connected PMOS transistors. The summation of the threshold voltages of the PMOS must be larger than VDDIO and V_{PAD} such that the transistors would be operated in the sub-threshold region and the static current can be decreased.

2) VDDIO Detector: VDDIO detector is implemented with a string of diode-connected PMOS, four detection circuits, (DT0, DT1, DT2, and DT3), and a thermometer code to one-hot code decoder, as illustrated in Fig. 3. As mentioned previously, the total threshold voltages are larger than VDDIO such that the DC current in the PMOS string is very small. The DC voltages VX1$\sim$VX11 generated by the PMOS string devices are all proportional to VDDIO. VX4, VX5, VX7, VX8, VX10 are fed into DT0$\sim$DT3 for VDDIO detection. Since VX4 and VX5 would be larger than 1.8 V for VDDIO at VDDH, a protection transistor NMOS should be inserted at the gate of the transistors PM701 and PM702. Through simple glue logic gates, the thermometer code VD0$\sim$VD3 could be easily converted into the one-hot code VD50, VD33, VD25, and VD18. The thermometer code VD0$\sim$VD3 can be obtained according to various

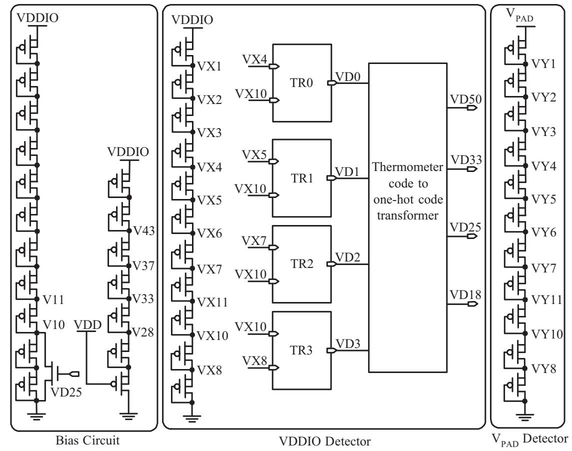

Fig. 3. Bias circuit, VDDIO detector and V_{PAD} detector.

VDDIO.

3) V_{g1} Generator: In Fig. 4, V_{g1} generator comprises a cross-coupled latch and a voltage level converter, which outputs a pair of opposite signals, Q and QB. It is composed of two cross-coupled transistors PMOS with two NMOS transistors in series as discharging paths. V_{g1} generator contains three pairs of discharging paths which are respectively controlled by the signals UP50, UPL, UP18, and their complementary signals. When VDDIO is fed with 5 V and MN105 is turned on, QB is discharged to 3.3 V through the first pair of discharging paths (MP103 , MN101, MP105, MN103, and MN105) while Q is pulled up to VDDIO. When VDDIO is fed with 3.3/2.5 V, the second pair of discharging paths (MN107$\sim$MN110, MP107, and MP108) is activated, which is controlled by UPL and $\overline{\text{UPL}}$. When VDDIO is fed with 1.8/1.2/0.9 V, the third discharging path (MN111$\sim$MN116) is on. Referring to the logic equations in Fig. 4, any input voltage will appear only in one pair of discharging paths.

4) V_{g2} and V_{g4} Generator: Fig. 5 (a) shows the schematic of V_{g2} generator. MN201 is a clamping NMOS, which can only pass the signal smaller than VX2$-V_{thn}$, where V_{thn} is the threshold voltage of NMOS. When VDDIO is fed with 5 V, OE18 and OE50 are both biased at 1.8 V such that V_{g2} can be biased at 3.2 V (VX2-V_{thn}) through MN202 and MP201 without gate-oxide overstress. MP202 is turned off under the condition that VX2 is higher than 3.2 V . If VDDIO is lower than 1.8 V in the receiving mode, OE18 and OE50 are all biased at 1.8 V such that MN202 and MP201 are turned off. V_{g2} can be operated at 1.8 V through MP203 and MP203, when VX2 is lower than 1.8 V. Besides, the undesired leakage current caused by the parasitic diodes of MP202 and MP203 can be eliminated by connecting their N-well to a floating N-well circuit comprising MN203, MP204, and MP206.

V_{g4} generator is shown in Fig. 5 (b). It pulls V_{g4} to 3.2 V when V_{PAD} is at 5 V and keeps V_{g4} at 1.8 V

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for V_{PAD} equal to 3.3 V. When V_{PAD} is at 5 V, V_{g4} is biased at 3.2 V (VY4 $-V_{thn}$) by the clamping NMOS MN401. When V_{PAD} is biased at 3.3/2.5/1.8/1.2/0.9/0 V, VY4 -V_{thn} is smaller than 1.8 V and blocked by MP401. V_{g4} is then biased at 1.8 V by MP402, because VY3 is lower than 1.8 V.

5) V_{g3} Generator: The proposed V_{g3} generator is depicted in Fig. 6 (a). In the receiving mode, when VDDIO is fed with 1.8/1.2/0.9 V and V_{PAD} is biased at 5 V, the voltage of V_{neta} and V_{netb} are clamped at 3.2V for passing V_{PAD} to V_{g3} in order to avoid the leakage current problem. Besides, MN301 is turned off by floating N-well circuit F_2 when the voltage of V_{net_bias} is lower than 1.8V. When V_{PAD} is at 0 V, an edge detector is adopt to prevent transistor P_{o3} from gate-oxide overstress. When V_{PAD} is at 2.5/3.3 V, V_{netb} is generated at 1.8 V by floating N-well circuit F1. Then, V_{PAD} is passed to MP318 to turn off the output stage P_{o3}. In the transmitting mode, when VDDIO is operated at 5 V, a negative pulse, which is triggered at the negative edge of D_{OUT}, would pulled V_{g3} down to 1.8 V. Thus, the gate-oxide overstress can be avoided. When VDDIO is operated at 1.8/1.2/0.9 V, V_{g2} is biased at 1.8/1.2/0.9 V and MN304 is turned off to protect V_{g3} from any leakage current.

E. Floating N-well Circuit

To avoid the undesired leakage current path through the parasitic diode of P_{o3}, V_{well_out} is varied with different V_{PAD} by the floating N-well circuit. The proposed floating N-well circuit is composed of two traditional floating N-well cells, FN51 and FN52, as shown in Fig. 6 (b). With the clamping NMOS MN503, FN52 can output the signal V_{well_cont} at Max(VY2$-V_{thn}$, 1.8 V).When V_{PAD} is operated at 3.3 V, V_{well_cont} is biased at 1.8 V. When V_{PAD} is at 5 V, V_{well_cont} at 3.2 V ($=$ VY2 $-$ V_{thn}) is used as the protection voltage for MP503. On the other hand, FN51 can generate the output signal V_{well_out} = Max(V_{PAD}, V_{well_cont}).

III. Implementation and Simulation Results

The proposed design is implemented with a typical 0.18 μm CMOS process. Fig. 7 shows the layout of the proposed mixed-voltage I/O buffer. The maximum data rate with different VDDIO are simulated in the TX mode, as shown in Fig. 8. The waveform of $V_{g1}\sim V_{g4}$ and V_{well_out} with different VDDIO are illustrated in Fig. 9. Fig. 10 depicts the waveforms of V_{PAD} and D_{IN} with different V_{PAD} in TX mode, whereas D_{IN} are all obtained at 1.8 V. Fig. 11 presents the waveform of $V_{g1}\sim V_{g4}$ and V_{well_out}, when VDDIO and V_{PAD} are received at 0.9 V and 5 V, respectively. The performance of the proposed mixed-voltage I/O buffer is summarized in Table II compared with previous I/O buffers. Table II shows that a wide voltage range, 3$\times$VDD, is successfully achieved by this work.

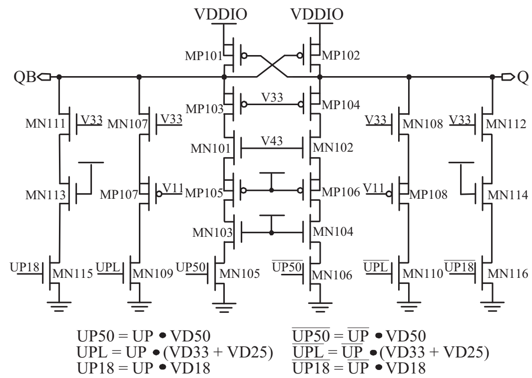

Fig. 4. V_{g1} generator.

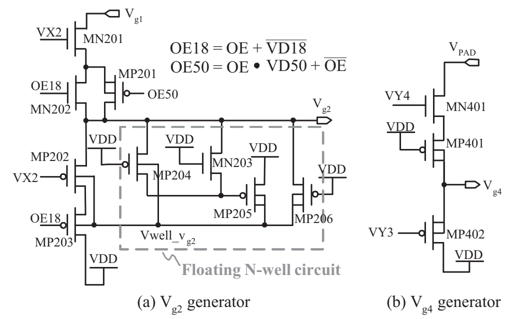

Fig. 5. V_{g2} generator and V_{g4} generator.

IV. Conclusion

A 0.9 V to 5 V mixed-voltage tolerant I/O buffer is proposed in this paper. The signal from $\frac{1}{2}\times$VDD to 3$\times$VDD can be transmitted and received simultaneously. Besides, the effects of gate-oxide overstress and the leakage current are both eliminated. All functions are verified through simulation results.

V. Acknowledgment

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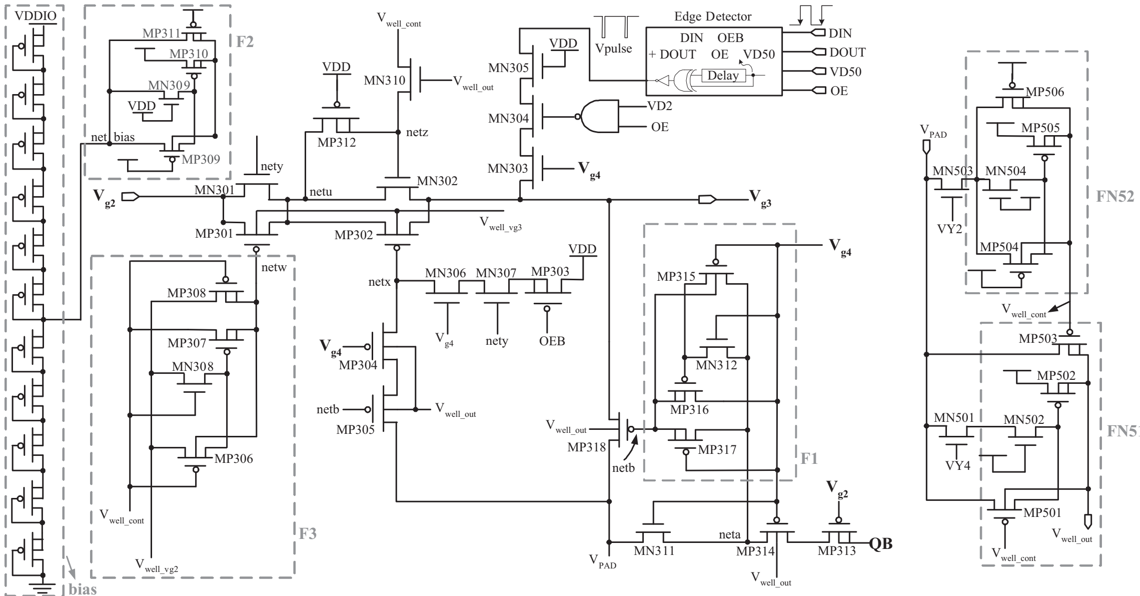

(a) V_{g3} generator

(b) Floating N-well circuit

Fig. 6. V_{g3} generator circuit and the floating N-well circuit.

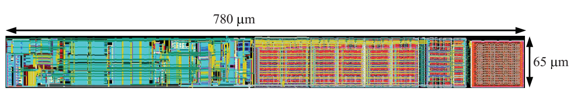

Fig. 7. Layout of the proposed mixed-voltage I/O buffer.

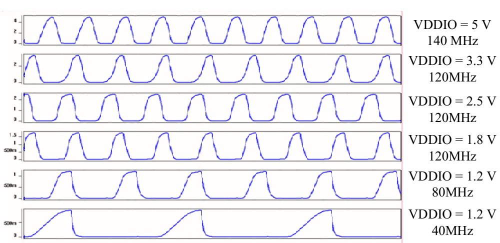

Fig. 8. The maximum data rate with different VDDIO in TX mode.

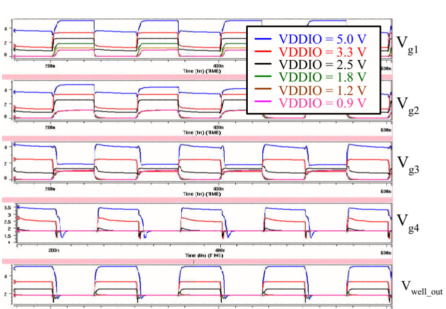

Fig. 9. V_{g1}~V_{g4} and V_{well_out} given different VDDIO.

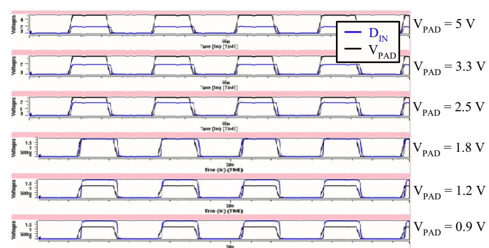

Fig. 10. V_{PAD} and D_{IN} given different V_{PAD} in TX mode.

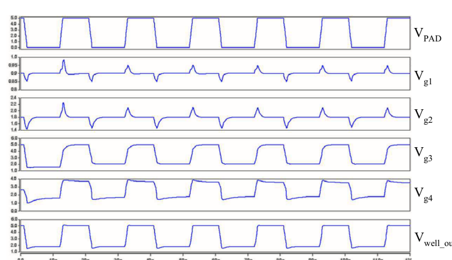

Fig. 11. V_{g1}~V_{g4} and V_{well_out}. (VDDIO=0.9 V, V_{PAD}=5 V)

TABLE II
PERFORMANCE CAPARISON OF MIXED-VOLTAGE I/O BUFFER

	Year	Transmitting voltage mode (V)	Process μm
This work	2009	0.9/1.2/1.8/2.5/3.5/5	0.18
[1]	2008	1.5/3.3	0.18
[2]	2007	1.2/2.5	0.13
[3]	2007	1.8/3.3	0.18
[4]	2006	2.5/5	0.25