A ROM-less DDFS Using A Nonlinear DAC With An Error Compensation Current Array

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***Abstract*— This paper presents the architecture and the circuit implementation of a direct digital frequency synthesizer (DDFS) with error compensation. The straight line approximation method with a 10-bit amplitude resolution is adopted in this work. The proposed technique replaces conventual ROM-based methods with a nonlinear digital-to-analog converter (DAC) to generate the sinusoid. The overall power dissipation as well as hardware complexity can be significantly reduced. This proposed DDFS is implemented using a standard 0.35μm CMOS technology. The maximum power dissipation is 3.37mW at the clock rate of 250 MHz. The chip area is 2.04 mm^2. The spurious free dynamic range (SFDR) is 63.22 dBc at a 3 MHz output.**

Keywords : DDFS, nonlinear DAC, line approximation, error compensatio, SFDR.

I. INTRODUCTION

Frequency synthesizer is an essential element in many communication systems. Phase-lock loops (PLLs) are usually employed to synthesize sinusoidal waves. However, PLL-based frequency synthesizers can not simultaneously provide both fast frequency switching and high spectral purity [1]. By contrast, direct digital frequency synthesizers (DDFS) have been considered as an alternative other than PLL-based frequency synthesizers. Because DDFS can provide faster frequency switching, excellent spectral purity, higher resolution, lower phase noise [2], and continuous phase frequency switching. Moreover, DDFS is capable of operating direct phase and frequency modulation in digital domain.

The conventional DDFS architecture is shown in Fig. 1 [3]. The phase values are converted by the phase accumulator, and samples of the sinusoid amplitude generated by a ROM look-up table are passed to DAC. The sinusoid function is smoothed by low pass filter (LPS) at last. The ROM-based DDFS architecture demands a large ROM to store the sinusoidal amplitude data, which results in more power dissipation, slower speed, and poor spectral purity. Therefore, many different researches of ROM-less DDFS architectures have been reported, e.g., [4]-[6].

Prior ROM-less DDFS works mainly developed complex polynomials to carry out the phase-to-sine mapper. If high-order polynomials are used, it will be difficult to meet the speed requirement of modern wireless communication applications due to the complexity algorithms. In order to reduce the hardware realization cost, any polynomial with more than three order will not be appreciated. Hence, lately proposed DDFSs adopted 2nd-order polynomials or less. However, these DDFSs are still difficult to provide a high performance since digital multipliers are needed in the implementation. A high performance DDFS is proposed using straight line approximation in this paper to resolve the mentioned problems.

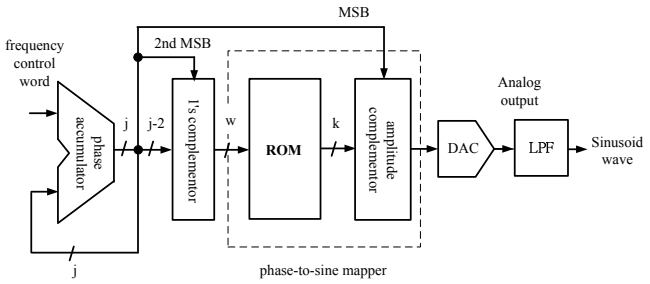

Fig. 1. Block diagram of the conventional DDFS

II. THE PROPOSED DDFS DESIGN

A. Straight Line Approximation

A perfect sinusoidal wave could be reconstructed with a quadrant waveform. The straight line approximation is considered the easiest algorithm to realize on digital circuitry. Providing that the straight line approximation is adopted to implement the DDFS with a *j*-bit phase accumulator, the formula of a quadrant of a synthesized sinusoid can be expressed as

$$y(x) = \begin{cases} (m_0 x + b_0) + e_0, & x_0 \le x < x_1 \\ (m_1 x + b_1) + e_1, & x_1 \le x < x_2 \\ \vdots & \\ (m_{j-1} x + b_{j-1}) + e_{j-1}, & x_{j-1} \le x < x_j \end{cases} \quad (1)$$

where the variable, *x*, is the output of the selected complementor, and the range of *x* is [0, $\frac{2^{j-2}-1}{2^{j-2}}$]. A complete sinusoid using quadrant symmetry can be determined by *n* sets of slope m_i, intercept b_i, and error compensation e_k. Since the error of the synthesized sine wave using by the 3-segment straight line approximation has been found to be large, we adopt 4 or more segments straight line approximation to synthesize a sinusoid. By thorough MATLAB simulations, the precision of the 4-segments straight line approximation is 2^{-6}, which is sufficient

to meet the requirement of our design. Then, we try to find out the minimum samples for the quadrant of a synthesized sine wave. The number of the samples under test is 128, 64, 32, and 16 samples. The SFDR is found to be not improved notably by 128 or 64 samples or more. Besides, 16 samples per quadrant is insufficient to provide a satisfactory SFDR. Hence, we adopted the 32 samplings for the synthesized sine wave after all.

Theoretically, the error compensation will be 32 values corresponding to the number of sampling. However, it will cause too much cost and slow speed. Thus, we propose to group close error values and average these values into an error correction value. Therefore, the errors are classified into 10 groups corresponding, respectively, to 10 categories of error compensation. According to the samples of the quadrant sine wave, we can select the corresponding error value e_k. The coefficients, m_i, b_i, and e_k, are obtained from an exhaustive attack method by using the simulations of MATLAB's Mathworks. A sup-optimal selection of straight line approximation's coefficients, m_i, and b_i, is shown in Table I. Table II shows the error compensation values, e_k. The maximum error is reduced to be less than 0.1%. Fig. 2 shows the error and the corresponding error correction value between real sinusoid and the proposed approximation, where the maximum error attained graphically is 0.0225. Since the addition and multiplication can be easily implemented by analog current mode design, we can select the suitable m_i, b_i, and e_k without paying too much cost of the hardware complexity for DDFS implementations.

TABLE I
COEFFICIENTS OF m_i, b_i VS. x

i	m_i	b_i	x
0	3/2	0.0196	0/32 ∼ 11/32
1	1	0.2030	12/32 ∼ 22/32
2	1/2	0.5414	23/32 ∼ 27/32
3	1/4	0.7465	28/32 ∼ 31/32

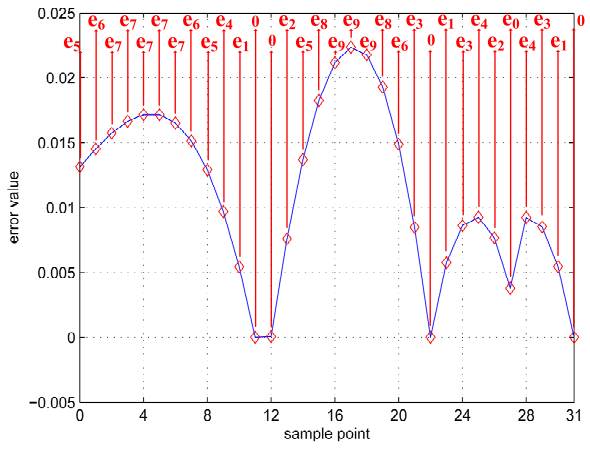

Fig. 2. The error between the real sinusoid and the synthesized one

B. Proposed DDFS Architecture

Fig. 3 shows the architecture of the proposed DDFS. It can be partitioned into the following building blocks : a phase accumulator (PA), a selective 1's complementor (SC), a nonlinear DAC with error compensation, an analog complementor (AC), and a differential-to-single voltage amplifier. The PA is used to translate the "frequency control word" into control signals for the other function blocks. The two highest most significant bits (MSB) of the PA output are used to address the quarter-wave symmetry. The SC and AC produce the corresponding quadrant of the sine wave. The nonlinear DAC converts the digital phase data into the sine amplitude by the straight line approximation method. The nonlinear DAC is implemented as a current mode DAC. The MSB from the output of the PA is adopted as a sign bit, and then the Gilbert multiplier generates the counterpart of the synthesize of the sinusoidal wave. However the swing of the sinusoidal wave generated by the Gilbert multiplier is relatively small. A differential-to-single voltage amplifier is added to magnify the output.

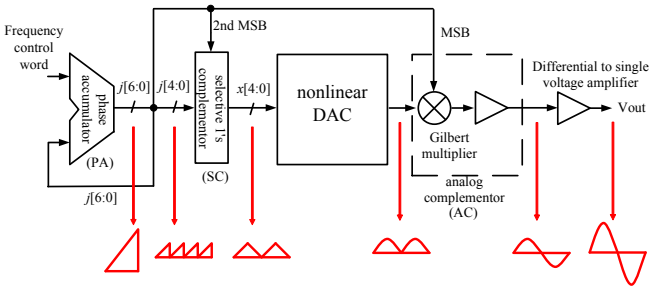

Fig. 3. The block of the proposed DDFS

C. Nonlinear DAC Design

The block diagram of the proposed nonlinear DAC is shown in Fig. 4. The current array converts the complement phase word "x" into a current signal. Then, the current signal is multiplied with m_i by the slope current mirror (SCM). The intercept current array (ICA) generates the current signal "b_i". The error compensation current array (ECCA) generates the corresponding error compensation current, e_k, $0 \leq k \leq 9$. Hence, the straight line approximation is completed by the summation of the current current signals, $m_i x$, b_i, and e_k. According to the signal x[4:0], decoders, DEC1 and DEC2, send the selecting signal, respectively, to the corresponding slope, intercept, and compensation current arrays. Besides, we use the bandgap reference to provide a stable temperature-insensitive bias for the current array.

An improved active-feedback cascade (IAFC) current mirror [7] is adopted in the current arrays. The structure of IAFC is illustrated in Fig. 5. The output stage of IAFC current mirror employs the regulated-gate cascade stage [8], where the source follower M53 and the active negative feedback composed of M5E and M5K increase the output impedance. The M5B, M5C, M5D and M5E are used to equalize the voltage V_{dsM5A} and V_{dsM5K}. Therefore, V_{gsM5A} will be equal to V_{gsM5K}, and then V_{dsM51} and V_{gsM52} will be the same. The simulation result of the error of the current mirroring is shown in Fig. 6. The maximum error is less than 0.3%, which is more than enough to meet the requirement of our design.

The basic current mirror array structure for SCM, ICA, and ECCA is shown in Fig. 7. Digital signals select current mirror branches to determine whether individual current flows through the load to synthesize sine wave or through the dummy resistor. Since one of the selected transistors in a current mirror branch will be on, and the settling time of the current mirrors is drastically reduced.

TABLE II
COEFFICIENTS OF e_k

error correction category	e_0	e_1	e_2	e_3	e_4
error correction value	0.00375	0.005625	0.0075	0.0084375	0.009375
error correction category	e_5	e_6	e_7	e_8	e_9
error correction value	0.0134375	0.0146875	0.01625	0.01875	0.021875

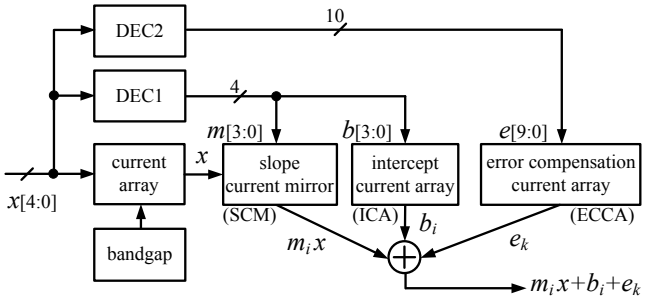

Fig. 4. The block of the proposed nonlinear DAC

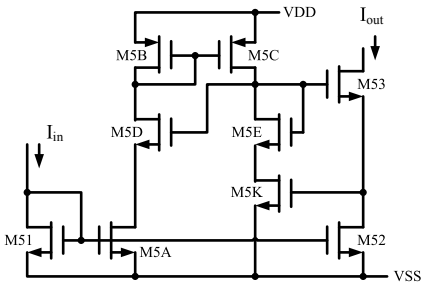

Fig. 5. IAFC current mirror

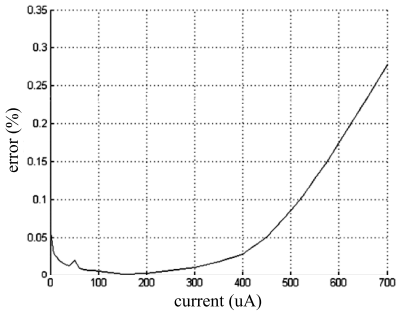

Fig. 6. Current mirroring error

D. Differential-to-single voltage amplifier

The swing of the output signal of the Gilbert multiplier is less than 100 mV. A differential-to-single voltage amplifier is designed as shown in Fig. 8 to magnify the output amplitude. OP1 and OP2 are unit gain buffers, where V_A=$Vo1$ and V_B=$Vo2$. The common-mode voltage V_C can be derived by ratio of the resistors R1 and R2 between V_A and V_B. In order to obtain V_{out} as h times of $Vo1$ and $Vo2$, R8=$h\times$R7, where R7 is the impedance looking into OP4. By applying the superposition to derive V_{out}, the voltage V_E has been set as $-h/(h+1)$ times of V_A. Therefore, the ratio of R3 to R5 is $h:(h+1)$. Besides, R4 is equal to R6. Finally, the voltage of V_{out}

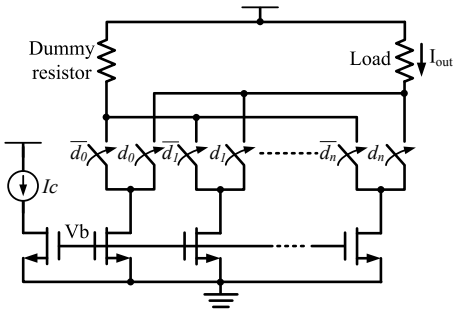

Fig. 7. The schematic of the current mirror array

can be expressed as follows:

$$\begin{aligned} & V_{out} = (h+1)\times V_E - h\times V_G \\ & \Rightarrow (h+1)\times(\tfrac{-h}{h+1})\times V_A + h\times V_B \\ & \Rightarrow h\times V_B - h\times V_A \\ & \Rightarrow h\times(V_B - V_A) \\ & \Rightarrow h\times(Vo2 - Vo1) \end{aligned} \tag{2}$$

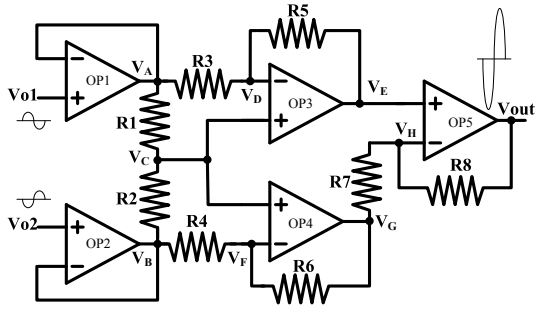

Fig. 8. The differentia-to-single voltage amplifier

III. Simulation and Implementation

TSMC (Taiwan Semiconductor Manufacturing Company) standard 0.35 μm CMOS technology is adopted to verify the performance of the proposed DDFS. Fig. 9 is the layout of the proposed design. Fig. 10 illustrates the simulation of the synthesized sine wave given the clock rate of 250 MHz. Fig. 11 shows that the spurious free dynamic range (SFDR) of the synthesized sine wave is -62.42 dBc at 3 MHz. Table III shows the specifications and the comparison between the proposed design and the prior works. The proposed design possesses the superiority of highest frequency, lowest power dissipation and the best SFDR among all of DDFS designs.

IV. Conclusion

In this paper, a low power DDFS with error compensation is proposed. This design using a nonlinear DAC is based on the

TABLE III
COMPARISON BETWEEN THE PRIOR WORKS AND THE PROPOSED PROTOTYPE

	Ours	[9]	[10]	[11]	[12]
CMOS technology (μ)	0.35	0.5	0.5	0.35	0.5
Power supply	3.3	3.3	2.7	3.3	5
Max. clock rate (MHz)	250	230	130	50	150
Max. output freq. (MHz)	3	0.1	0.1	1	n/a
Power consumption (mW)	3.37 (250 MHz)*	92 (230 MHz)	8 (100 MHz)	0.4 (50 MHz)**	496 (150 MHz)
Amplitude resolution (bits)	10	11	8	n/a	10
Area	2.04	1.6	1.4	0.0085*	9
SFDR	63.22 @ 3 MHz	55 @ 0.1 MHz	57.3 @ 0.1 MHz	50 @ 1MHz	57.6

* : The chip's area and power consumption has not include the output amplifier.
** : The chip's area and power consumption has not include the phase accumulator and the linear DAC.

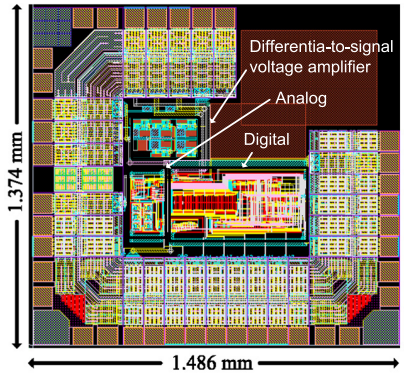

Fig. 9. The layout of the proposed DDFS

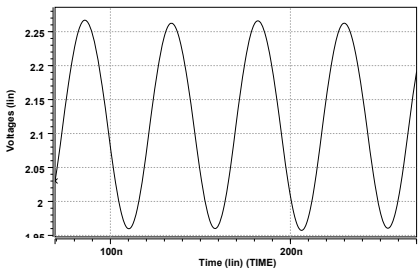

Fig. 10. The synthesized sine wave

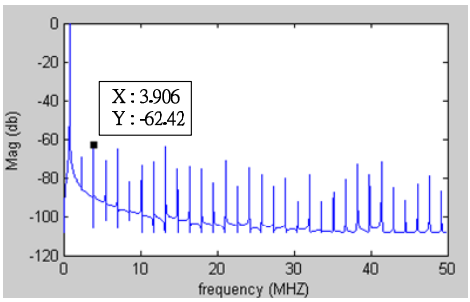

Fig. 11. The spectrum of the synthesized sine wave

straight line approximation. This technique transforms the conventional ROM-based phase conversion into one nonlinear DAC. The power consumption as well as hardware complexity is greatly reduced without any loss of SFDR.

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