# 0.9 V to 5.0 V Mixed-Voltage I/O Buffer Design Using 0.18 $\mu$m 1.8-V CMOS Technology

Tzung-Je Lee, Jen-Wei Liu, Tong-Han Tsai, and Chua-Chin Wang
Department of Electrical Engineering
National Sun Yat-Sen University
Kaohsiung, Taiwan 80424
Email : ccwang@ee.nsysu.edu.tw

***Abstract*— This paper proposes a mixed-voltage I/O buffer which can simultaneously transmit and receive the signal of 0.9 V to 5.0 V in a typical 0.18 $\mu$m 1.8-V CMOS process. In order to achieve such a very wide range specification, the proposed I/O buffer overcomes the challenge of avoiding the gate-oxide overstress in 1.8-V devices with high supply voltage (VDDH = 5.0 V) larger than two times of the tolerant operating voltage (1.8 V). Thus, triple stacked MOS transistors are used in the output stage to ensure the gate-oxide reliability. Besides, a 3.2 V voltage must be generated to deal with a 5.0 V signal using a Bias circuit and NMOS clamping technique. The simulation results reveal the gate-oxide overstress is avoided in the output stage. The maximum output data rate is simulated to be 120/100/110/100/80/40 Mbps for 5.0/3.3/2.5/1.8/1.2/0.9 V given a capacitive load of 10 pF.**

## I. Introduction

Up to now, there is no I/O buffer which can simultaneously transmit and receive the signal with the voltage from 1/2×VDD to ∼3×VDD [1]-[6]. Thus, this paper proposes a very wide range I/O buffer able to transmit and receive the signal from 0.9 V to 5.0 V based on 1.8 V devices. In order to communicate the signal at ∼3×VDD, triple stacked MOS transistors are used in the output stage to avoid the gate-oxide overstress. Besides, the traditional gate-tracking circuit and floating N-well circuit can not be used directly due to the high voltage signal very close to 3×VDD. Therefore, the high voltage VDDH (5.0 V) is detected and a protection voltage equal to VDDH-VDD (3.2 V) is generated to ensure the gate-oxide reliability. The NMOS clamping technique, which can avoid a power-consuming DC current path, is employed to generate this protection voltage.

## II. The proposed 0.9 V to 5.0 V I/O buffer

Fig. 1 shows the block diagram of the proposed very wide range I/O buffer, comprising Pre-driver, Output stage, Input stage, Dynamic gate bias generator, and Floating N-well circuit.

**Output stage:** Because the supply voltage would be applied to the voltage ∼3×VDD, triple stacked MOS transistors should be used to avoid the gate-oxide overstress. Besides, the gate voltages should be biased at appropriate voltages to ensure the function and the reliability, as shown in the truth table in Fig. 1. When logic 1 is transmitted and VDDIO > VDD, Vg1∼Vg3 should be biased at the voltage > VDDIO-VDD such that Po1∼Po3 can be turned on with their gate-drain and gate-source voltages < 1.8 V. Vg4 should be pulled to the voltage of 3.2 V (= VDDH-VDD) when $V_{PAD}$ is at 5.0 V. When logic 0 is transmitted, Vg4 must be discharged to VDD such that Vgd of No1 can be less than 1.8 V. When VDDIO < VDD and logic 1 is transmitted, Vg1∼Vg3 must be pulled to 0 V to turn on Po1∼Po3.

In the receiving mode, Vg1 is equaled to VDDIO to turn off Po1. When VDDIO > VDD, Vg2 should be biased at the voltage larger than 3.2 V to avoid the gate-oxide overstress. When VDDIO ≤ VDD, Vg2 just needs to be biased at 1.8 V. At the same time, Vg3 is biased at 1.8 V until $V_{PAD}$ > VDD is received. Vg3 is then pulled to $V_{PAD}$ by the gate-tracking mechanism in the Dynamic gate bias generator to avoid the the leakage current path due to the turned-on Po3. Vg4 should be pulled to 3.2 V for $V_{PAD}$ = 5.0 V to ensure the reliability of No1∼No3. Besides, the N-well of Po3 is biased at the output of the Floating N-well circuit, $V_{well\_out}$. When $V_{PAD}$ > VDD, $V_{well\_out}$ is pulled to $V_{PAD}$ to eliminate the leakage current path through the parasitic diode of Po3.

**Pre-driver:** The Pre-driver is a simple logic circuit to decode and pre-drive. When OE = 1.8 V, the I/O buffer operates at the transmitting mode. The logic state of $V_{PAD}$ is determined by DOUT. When OE = 0 V, the I/O buffer is at the receiving mode. The receiving signal DIN would be determined by $V_{PAD}$.

**Dynamic gate bias generator:** The Dynamic gate bias generator receives the signals UP, $V_{well\_out}$ and $V_{PAD}$, and generates the appropriate gate voltages for the Output stage. The Dynamic gate bias generator consists of the Bias circuit, VDDIO detector, $V_{PAD}$ detector, Vg1 generator, Vg2 generator, Vg3 generator, and Vg4 generator, as shown in Fig. 2. The Bias circuit and $V_{PAD}$ detector can provide the required DC voltages according to VDDIO and $V_{PAD}$, respectively, for the other circuits in the Dynamic gate bias generator. VDDIO detector outputs 4 control signals (VD50, VD33, VD25, and VD18) to determine the VDDIO mode. Logic 1 at VD50, VD33, VD25, and VD18 represent VDDIO = 5.0 V, 3.3 V, 2.5 V, and ≤ 1.8 V, respectively. Vg1 generator is based on a voltage level converter. Vg2 generator outputs the gate voltage Vg2 from Vg1 by using MOS switches. Vg3 and Vg4 generators possess the gate-tracking mechanism, which can determine Vg3 and Vg4 according to $V_{PAD}$.

*Bias circuit and $V_{PAD}$ detector:* Referring to Fig. 2 (a), the Bias circuit and $V_{PAD}$ detector are composed of two individual strings of diode-connected PMOS transistors, respectively. The DC signals, V43, V37, V33, V28, and V11, are fed into Vg1

generator to be the clamping voltages or the protection voltages. The summation of the threshold voltages of the PMOS must be larger than VDDIO and $V_{PAD}$ such that the transistors would operate at sub-threshold region and the static current can be reduced.

*VDDIO detector:* VDDIO detector is composed of a string of diode-connected PMOS, four detection circuits, (DT0, DT1, DT2, and DT3), and a Thermometer code to one-hot code decoder, as shown in Fig. 2 (b). As mentioned previously, the total threshold voltages are larger than VDDIO such that the operation current in the PMOS string is very small. The PMOS string provides 10 DC voltage VX1∼VX11, which are all proportional to VDDIO. VX4, VX5, VX7, VX8, VX10 are fed into DT0∼DT3 for VDDIO detection. Because VX4 and VX5 would be larger than 1.8 V for VDDIO at VDDH, a protection NMOS should be added at the gate of the PM701 and PM702. For VDDIO = 5.0 V, 3.3 V, 2.5 V, and 1.8 V, VX4 is biased at 3.23 V, 2.31 V, 1.86 V, and 1.335 V, respectively, while VX10 is at 1.0 V, 0.82 V, 0.78 V, and 0.56 V, respectively. Due to VX4 $>$ 1.8 V for VDDIO $>$ 1.8 V, the gate of MP701 would be at ∼1.8 V such that MP701 is turned off. MN701 is turned on by VX10. Thus, DT0 outputs the signal VD0 at 0 V. On the other hand, MP701 is on and MN701 is off such that VD0 is pulled to 1.8 V for VDDIO $\leq$ 1.8 V. By selecting the DC voltage, the PMOS and NMOS in DT0∼DT3 would not be turned on simultaneously such that the static current is very small. The thermometer code VD0∼VD3 can be obtained according to different VDDIO, as shown in Fig. 2 (b). The thermometer code VD0∼VD3 could be easily converted into the one-hot code VD50, VD33, VD25, and VD18. Logic 1 at VD50, VD33, VD25, and VD18 indicates VDDIO is at 5.0 V, 3.3 V, 2.5 V or $\leq$ 1.8 V, respectively.

*Vg1 generator:* Referring to Fig. 2 (d), Vg1 generator is a modified voltage level converter which outputs the dual signals Q (Vg1) and QB. A basic voltage level converter is composed of two cross-coupled PMOS (like MP101 and MP102) transistors with two NMOS transistors in series to be the discharging paths. There are only two of the six discharging paths would be activated for different VDDIO modes, [5.0 V], [3.3 and 2.5 V], and [<1.8 V]. The discharging paths are controlled by the signals UP50, UPL, UP18, and their complementary signals. When VDDIO = 5.0 V, UP50 and UP50 are activated and UP18, UPL, $\overline{\text{UP18}}$, and $\overline{\text{UPL}}$ are at 0 V. Thus, only the branches through MN105 and MN106 are activated. According to UP, QB and Q would be vary between VDDIO (pulled by MP101 and MP102) and V28 + |Vtp| (clamped by MP103 and MP104). MN101∼MN104, MP105, and MP106 are the protection transistors to prevent transistors from the gate-oxide overstress for VDDIO $>$ 1.8 V. Similarly, Q and QB can change between VDDIO and V11 + |Vtp| for VDDIO = 3.3 V and 2.5 V by activating UPL, and change between 0 V and VDDIO for VDDIO $\leq$ 1.8 V by activating UP18. Notably, V11 is biased at 1.24 V and 0.38 V for VDDIO = 3.3 V and 2.5 V, respectively, by the state of MN705. Thus, the lower bound of Q and QB can be 1.5 V (= 3.3 V - 1.8 V) and 0.7 V (= 2.5 V - 1.8 V) for VDDIO = 3.3 V and 2.5 V, respectively. V33 is the protection voltage, while MP103, MP104, and MN111∼MN114 are the protection transistors.

*Vg2 generator:* Fig. 2 (e) shows the schematic of Vg2 generator. MN201 is a clamping NMOS, which can only pass the signal smaller than V37-Vtn. When VDDIO = 5.0 V, OE18 and OE50 are both biased at 1.8 V such that Vg2 can be biased at 3.2 V (≈ V37-Vtn) through MN202 and MP201 without gate-oxide overstress. MP202 is turned off due to VX3 $>$ 3.2 V . For VDDIO $<$ 1.8 V in the receiving mode, OE18 is at 0 V and OE50 is at 1.8 V such that MN202 and MP201 are off. Vg2 can be biased at 1.8 V through MP203 and MP203 due to VX3 $<$ 1.8 V. Notably, the unwanted leakage current through the parasitic diodes of MP202 and MP203 can be removed by connecting their N-well to a traditional floating N-well circuit composed of MN203, and MP204∼MP206.

*Vg3 generator:* Fig. 2 (f) shows the schematic of Vg3 generator. When $V_{PAD}$ = 5.0 V in the receiving mode, QB and Vg4 are biased at 3.2 V such that $V_{PAD}$ can be passed to Vg3 through MP303 and MP304. Because Vg1 is at 5.0 V, MP302 would be turned off such that the internal transistors in Vg2 generator are protected from the high voltage (5.0 V) at Vg3. When $V_{PAD}$ = 0 V, MN302, MP302, and MP303 can not provide any discharge paths for Vg3 due to Vg1 = 5.0 V and QB = 3.2 V. Thus, Vg2 and Vg3 are both biased at 3.2 V. It causes the gate-drain voltage of Po3 to be larger than 1.8 V, because $V_{PAD}$ = 0 V. DIN edge detector is used to provide a discharge path in this situation. A negative pulse (Vpulse), which is triggered at the negative edge at DIN, would pull Vg3 to ∼1.8 V. Thus, the gate-oxide overstress can be avoided. When VDDIO is at 5.0 V and logic 1 is transmitted, QB is biased at 5.0 V such that the voltage of 5.0 V at $V_{PAD}$ can not be passed through MP303. Besides, Vg4 is at 3.2 V to protect MP304 from gate-oxide overstress. Vg3 is determined by Vg2 through MN301 and MN302. Similarly, the gate-tracking mechanism is shutdown and Vg3 is determined by Vg2 for other VDDIO in the transmitting mode.

*Vg4 generator:* Vg4 generator is shown in Fig. 2 (g). It pulls Vg4 to 3.2 V for $V_{PAD}$ = 5.0 V and keeps Vg4 at 1.8 V for $V_{PAD}$ $\leq$ 3.3 V. When $V_{PAD}$ is at 5.0 V, Vg4 is biased at 3.2 V (≈ VY4 - Vtn) by the clamping NMOS MN401. At the same time, MP402 is turned off due to VY3 $>$ VY4 - Vtn. When $V_{PAD}$ is biased at 3.3/2.5/1.8/1.2/0.9/0 V, VY4 - Vtn is smaller than 1.8 V and blocked by MP401. Vg4 is then biased at 1.8 V by MP402 due to VY3 $<$ 1.8 V.

**Floating N-well circuit:** The Floating N-well circuit biases $V_{well\_out}$ at an appropriate voltage to avoid the unwanted leakage current path through the parasitic diode of Po3 according to $V_{PAD}$. The Floating N-well circuit is composed of two modified floating N-well circuit, FN51 and FN52, as shown in Fig. 3. With the clamping NMOS MN503, FN52 can output the signal $V_{well\_cont}$ = Max(VY2-Vtn, 1.8 V).When $V_{PAD}$ $\leq$ 3.3 V, $V_{well\_cont}$ is biased at 1.8 V. When $V_{PAD}$ = 5.0 V, $V_{well\_cont}$ at 3.2 V (= VY2-Vtn) is used as the protection voltage for MP503. On the other hand, FN1 can generate the

output signal $V_{well\_out}$ = Max($V_{PAD}$, $V_{well\_cont}$).

**Input stage:** The Input stage is based on a conventional input stage, which can receive the signal with high voltage VDDH > VDD, as shown in Fig. 2 (h). With the signal OE and the transistors MP601, MN602, and MP604, DIN would be biased at 0 V in the transmitting mode. $V_{well\_cont}$ = 3.2 V is used to protect the transistors from gate-oxide overstress for $V_{PAD}$ = 5.0 V.

## III. Implementation and Simulation

The proposed design is implemented using a typical 0.18 $\mu$m CMOS process. Fig. 4 shows the layout of the proposed I/O buffer. Fig. 5 and Fig. 6 show the simulated waveforms of the gate voltages and $V_{well\_out}$ for the worst corner of [SS, 100$^o$C] in the transmitting mode and the receiving mode, respectively. The gate voltages and $V_{well\_out}$ are verified to meet the requirements mentioned in Section II. Fig. 7 reveals the simulated $V_{PAD}$ at the maximum speed of 120/100/110/100/80/40 Mbps for VDDIO = 5.0/3.3/2.5/1.8/1.2/0.9 V, respectively, given a 10 pF load. Fig. 8 shows that DIN can be obtained correctly in the receiving mode for different receiving signals.

## IV. Conclusions

A 0.9 to 5.0 V I/O buffer is proposed in this paper. The gate-oxide overstress can be avoided by using the triple stacked transistors in the Output stage and a 3.2 V voltage generated using the Bias circuit and the NMOS clamping technique. The functions are verified according to the simulation results.


## Acknowledgment

This research was partially supported by National Science Council under grant NSC 95-2221-E-110-113 and by Himax Technologies, Inc., under grant 96A20763. The authors would like to express their deepest gratefulness to CIC (Chip Implementation Center) of NARL (National Applied Research Laboratories), Taiwan, for their thoughtful chip fabrication service. The authors also like to thank "Aim for Top University Plan" project of NSYSU and Ministry of Education, Taiwan, for partially supporting the research.


## References


[1] M. J. M. Pelgrom and E. C. Dijkmans, "A 3/5 V compatible I/O buffer," *IEEE J. Solid-State Circuits*, vol. 30, no. 7, pp. 823-825, July 1995.

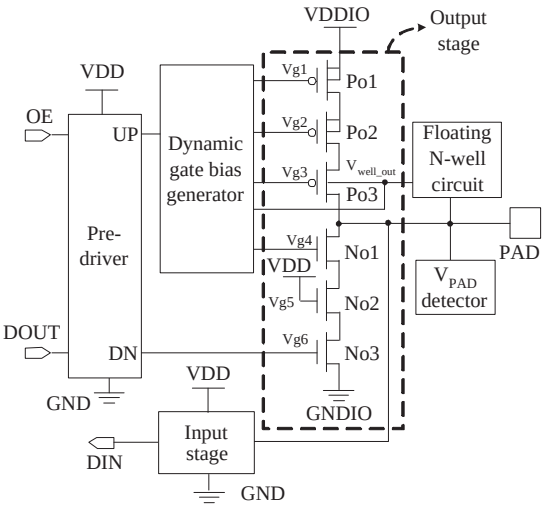
[2] G. P. Singh, and R. B. Salem, "High-voltage-tolerant I/O buffers with low-voltage CMOS process," *IEEE J. Solid-State Circuits*, vol. 34, no. 11, pp. 1512-1525, Nov. 1999.

[3] C.-H. Chuang, and M.-D. Ker, "Design on mixed-voltage-tolerant I/O interface with novel tracking circuits in a 0.13-um CMOS technology," in *Proc. of IEEE Int. Symp. on Circuits and Systems, 2004*, vol. 2, pp. 577-580, May 2004.

[4] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Overview and design of mixed-voltage I/O buffers with low-voltage thin-oxide CMOS transistors," *IEEE Tran. On Circuits and Systems I: Regular Papers*, vol. 53, no. 9, pp. 1934-1945, Sept. 2006.

[5] M.-D. Ker, and S.-L. Chen, "Design of mixed-voltage I/O buffer by using NMOS-blocking technique," *IEEE J. Solid-State Circuits*, vol. 41, no. 10, pp. 2324-2333, Oct. 2006.

[6] T.-J. Lee, W.-C. Chang, and C.-C. Wang, "Mixed-voltage-tolerant I/O buffer using a clamping dynamic gate bias generator," *2007 IEEE Region 10 Conference- Tencon 2007*, pp. 1-4, Nov. 2007.


**(a) Schematic of the proposed I/O buffer**

| Operating mode | VDDIO | Vg1 | Vg2 | Vg3 | Vg4 | Vg5 | Vg6 | $V_{well\ out}$ |
|---|---|---|---|---|---|---|---|---|
| Rx mode | 5.0 V | 5.0 V | >3.2V | 1.8 /$V_{PAD}$ # | 1.8/>3.2*V | 1.8 V | 0 V | 1.8 /$V_{PAD}$ b |
| | 3.3 V | 3.3 V | 3.3 V | 1.8 /$V_{PAD}$ # | 1.8/>3.2*V | 1.8 V | 0 V | 1.8 /$V_{PAD}$ b |
| | 2.5 V | 2.5 V | 2.5 V | 1.8 /$V_{PAD}$ # | 1.8/>3.2*V | 1.8 V | 0 V | 1.8 /$V_{PAD}$ b |
| | 1.8 V | 1.8 V | 1.8 V | 1.8 /$V_{PAD}$ # | 1.8/>3.2*V | 1.8 V | 0 V | 1.8 /$V_{PAD}$ b |
| | 1.2 V | 1.2 V | 1.8 V | 1.8 /$V_{PAD}$ # | 1.8/>3.2*V | 1.8 V | 0 V | 1.8 /$V_{PAD}$ b |
| | 0.9 V | 0.9 V | 1.8 V | 1.8 /$V_{PAD}$ # | 1.8/>3.2*V | 1.8 V | 0 V | 1.8 /$V_{PAD}$ b |
| Tx mode | 5.0 V | >3.2/5 V | >3.2 V | >3.2/1.8 V | >3.2/1.8 V | 1.8 V | 0/1.8 V | 1.8 /$V_{PAD}$ b |
| | 3.3 V | >1.5/3.3 V | >1.5 V | >1.5 V | 1.8 V | 1.8 V | 0/1.8 V | 1.8 /$V_{PAD}$ b |
| | 2.5 V | >0.7/2.5 V | >0.7 V | >0.7 V | 1.8 V | 1.8 V | 0/1.8 V | 1.8 /$V_{PAD}$ b |
| | 1.8 V | 0/1.8 V | 0 V | 0 V | 1.8 V | 1.8 V | 0/1.8 V | 1.8 /$V_{PAD}$ b |
| | 1.2 V | 0/1.2 V | 0 V | 0 V | 1.8 V | 1.8 V | 0/1.8 V | 1.8 /$V_{PAD}$ b |
| | 0.9 V | 0/0.9 V | 0 V | 0 V | 1.8 V | 1.8 V | 0/1.8 V | 1.8 /$V_{PAD}$ b |
| *When $V_{PAD}$ = 5.0 V in the Rx mode | | | | | | | | |
| #When $V_{PAD}$ > 1.8 V in the Rx mode | | | | | | | | |
| bWhen $V_{PAD}$ > VDD in the Rx mode and Tx mode | | | | | | | | |

**(b) Truth table of the proposed I/O buffer**

Fig. 1. Block diagram and truth table of the proposed I/O buffer.

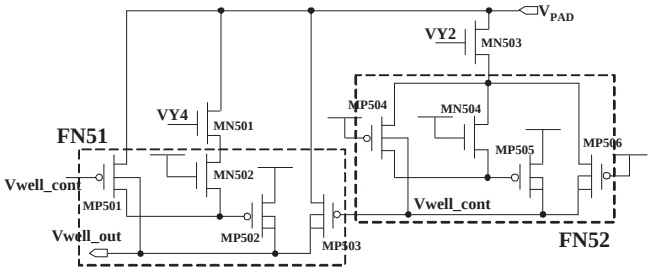



Fig. 3. Schematic of Floating N-well circuit.

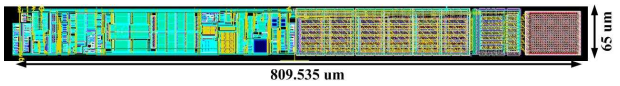



Fig. 4. Layout of the proposed I/O buffer.

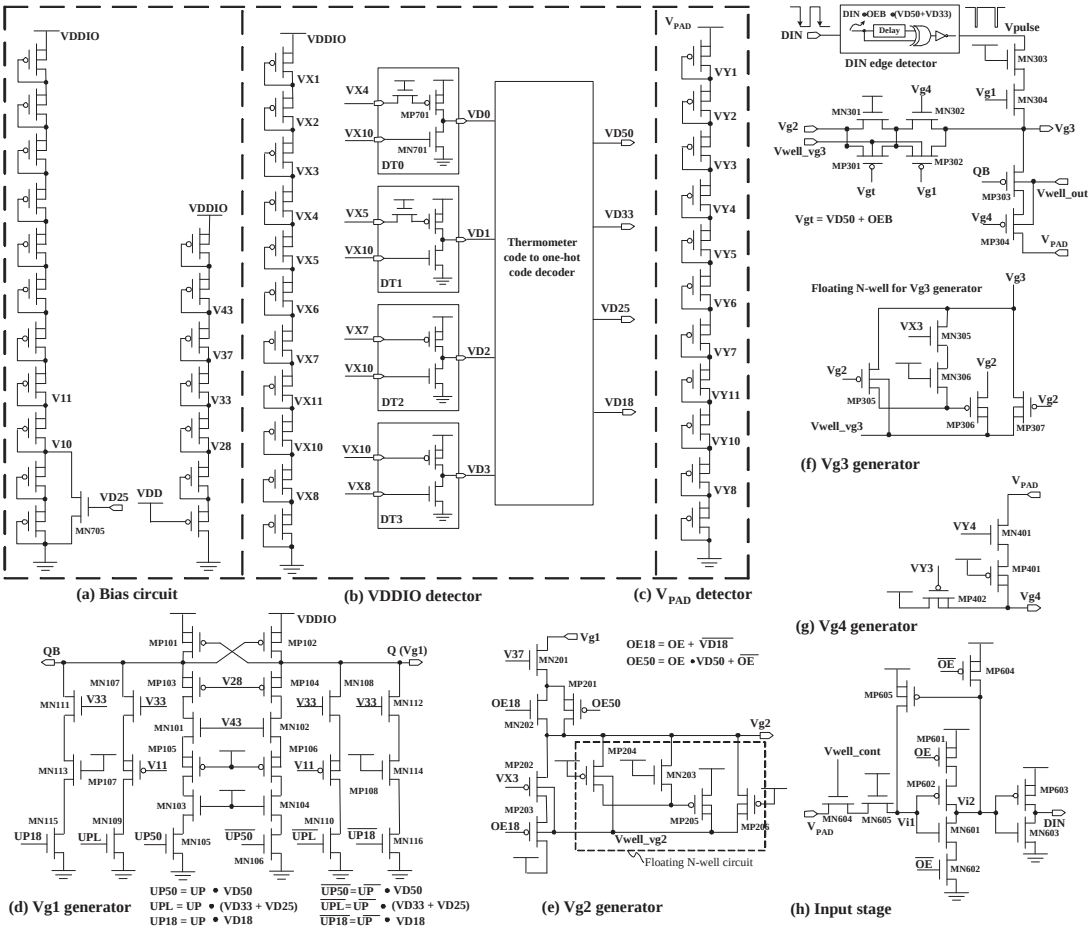



Fig. 2. Schematic of the Dynamic gate bias generator (a)∼(g) and the Input stage (h).

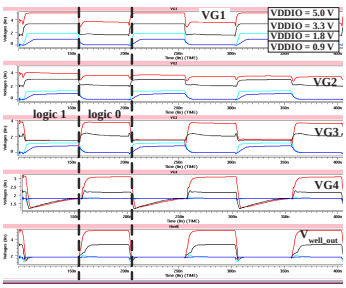



Fig. 5. Simulated waveform of Vg1∼Vg4 and $V_{well\_out}$ in the transmitting mode at 10 MHz for the worst corner of [SS, 100$^o$C].

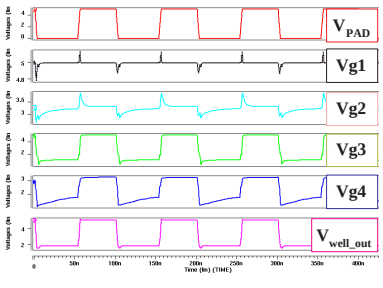



Fig. 6. Simulated $V_{PAD}$, Vg1∼Vg4 and $V_{well\_out}$ in the receiving mode at 10 MHz for the worst corner of [SS, 100$^o$C] for VDDIO = 5.0 V.

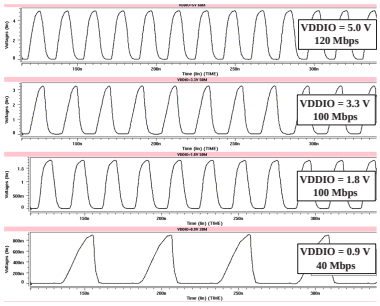



Fig. 7. $V_{PAD}$ at the maximum speed for different VDDIO given a 10 pF load at the worst simulation corner of [SS, 100$^o$C].

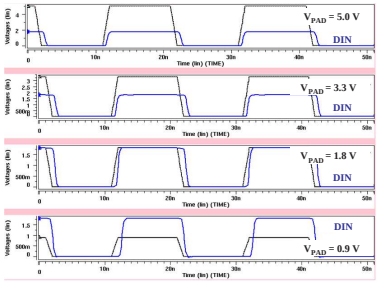



Fig. 8. Simulated DIN and $V_{PAD}$ at 50 MHz given a 1 pF load.