Mixed-Voltage I/O Buffer Using 0.35 μm CMOS Technology

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***Abstract*— A 0.9 V to 5.0 V (0.9/1.2/1.8/2.5/3.3/5 V) mixed-voltage-tolerant I/O buffer carried out using CMOS 2P4M 0.35 μm process is proposed in this paper. By using a Dynamic gate bias generator to provide appropriate gate voltages for the output stage composed of stacked PMOS and stacked NMOS, the I/O buffer can transmit the signal with higher voltage level (VDDH). Besides, a new floating N-well circuit is proposed to remove the body effect at the output PMOS. Moreover, a Dynamic driving detector is used to balance the turn-on voltages for the PMOS and NMOS in the output stage. The duty cycle of the output signal of the proposed I/O buffer can then be equalized for VDDIO biased at low voltage. The maximum output speed of the proposed design is simulated to be 110/125/110/80/50/20 MHz for VDDIO = 5.0/3.3/2.5/1.8/1.2/0.9 V, respectively. The static power consumption is merely 553 nW in the worst simulation case of [SS, 100^{o}C].**

I. Introduction

Mixed-voltage-tolerant I/O buffer were needed for communication between the signals with different voltage level [1]-[3]. The mixed-voltage-tolerant I/O buffers in these prior works employed a gate-tracking circuit and a floating N-well circuit to avoid the gate-oxide overstress, hot-carrier degradation, and the unwanted leakage current paths when a high voltage (VDDH) is biased at the PAD [2]. However, these I/O buffers would suffer from problems of Vsd or Vsg larger than the constrained voltage (VDD) when VDDIO is biased at VDDH, as shown in Fig. 1 (b)-(d). Hence, these traditional mixed-voltage-tolerant I/O buffer can not transmit the signals with higher voltage level. Therefore, their applications are limited.

In order to enlarge the application range, this paper proposes a very wide range mixed-voltage-tolerant I/O buffer which can both transmit and receive the signals with voltage level from 0.9 V to 5.0 V.

II. 0.9 V to 5.0 V Mixed-voltage-tolerant I/O Buffer

Referring to Fig. 2, the proposed I/O buffer possesses an output stage composed of stacked PMOS and stacked NMOS, and a Dynamic gate bias generator to provide appropriate gate biases. Therefore, the problems revealed in Fig. 1 can be all resolved. However, a DC bias required in the Dynamic gate bias generator would possess large static power consumption by using a simple MOS resistor string [4], or a penalty of circuit complexity by using diode-connected MOS and charge redistribution topology [5]. A Low power clamping bias circuit, as shown in Fig. 3, is employed in this paper by using clamping MOS to avoid any DC leakage path such that the static power consumption can be reduced.

On the other hand, the output PMOS PM202 would have body effect by using the traditional floating N-well circuit, which would bias the N-well at 3.3 V in the transmitting mode. Besides, when VDDIO is biased at VDDL (= 2.5/1.8/1.2/0.9 V), the turn-on voltage supplied for the output PMOS would be smaller than that for the output NMOS by using the control signal DN (3.3 V). The above phenomena would reduce the driving current I_{OH} such that the duty cycle of the output signal is not 50% for VDD = VDDL. That might cause missing code which should be avoided in most digital systems. The proposed design employs a new Floating N-well circuit, which provides a dynamic N-well voltage (Vnwell2) in the transmitting mode for VDDIO = VDDL to avoid the body effect. Moreover, a Dynamic driving detector, as shown in Fig. 3, is used to provide a dynamic Vg4 for the output NMOS such that the turn-on voltages could be identical. Therefore, the duty cycle of the output signal could be 50% for VDDIO = 0.9 V $\sim$ 5.0 V.

Pre-driver: The Pre-driver is for pre-driving and decoding. When OE = 3.3 V, the output signal Dout would be transmitted. In this case, UP and DN will be both biased at 3.3 V (0 V) for Dout = 0 V (3.3 V). When OE = 0 V, the I/O buffer is in the receiving mode and UP and DN would be biased at 3.3 V and 0 V, respectively.

Output stage: The output stage is composed of the stacked PMOS, PM201 and PM202, and the stacked NMOS, NM201 and NM202. Besides the stacked topologies, the output stage requires appropriate gate bias voltages to avoid gate-oxide overstress and operate correctly for different VDDIO supplied, as shown in Fig. 1. In the receiving mode, Vg1 is biased at voltage equal to VDDIO to turn PM201 off. While Vg2, Vg3, and Vg4 are biased at 3.3 V, 3.3 V, and 0 V, respectively. Notably, when V_{PAD} = 5.0 V, Vg2 should be pulled to 5.0 V by the gate-tracking circuit to avoid the leakage current path through PM202. In the transmitting mode, Vg1 and Vg2 are biased at the voltage larger than 1.7 V for VDDIO = 5.0 V and biased at 0 V for VDDIO $\leq$ 3.3 V. Thus, logic 1 can be transmitted and the gate-oxide overstress is avoided. For transmitting logic 0, Vg4 is biased at the voltage equal to VDDIO for VDDIO $\leq$ 3.3 V such that the equalized turn-on gate-source voltage would be accomplished. These gate bias voltages are provided by the Dynamic gate bias generator.

Dynamic gate bias generator: The Dynamic gate bias

generator is composed of a Low power clamping bias circuit, a VDDIO detector, a Voltage level converter, a Vg2 generator, and a Dynamic driving detector, as shown in Fig. 3.

Low power clamping bias circuit: The Low power clamping bias circuit provides a 1.7 V output (Vbias) for the Voltage level converter and the Vg2 generator. The Low power clamping bias circuit is composed of five stages of serial NMOS and PMOS. The common source node of the PMOS and NMOS in each stage is clamped at a steady voltage. If the voltage of the common source node is initially higher than that the expected value, it would be discharged by the PMOS. Contrarily, if the voltage of the node is low initially, it would be charged by the NMOS. Hence, the voltage of the common source node in each stage is clamped. Therefore, Vbias can be tuned to be 1.7 V, which is around five times of the threshold voltage of the PMOS.

VDDIO detector: The VDDIO detector can provide a output signal VL, which is 0 V for VDDIO = 5.0 V and is 3.3 V for VDDIO $\leq$ 3.3 V, to control the Voltage level converter, the Vg2 generator, the Dynamic driving detector, the Gate-tracking circuit, and the Floating N-well circuit automatically. When VDDIO = 5.0 V, PM403 and PM401 are turned on. V_Y is then pulled high to turn on NM402. Additionally, NM404 is turned on to pull V_X high such that PM405 is off. Therefore, VL is discharged to 0 V. When VDDIO $\leq$ 3.3 V, PM404 and NM403 would be turned on such that V_Y would be discharged to 0 V. It turns off NM402. Moreover, PM405 is turned on because of V_X pulled low. Therefore, VL is biased at 3.3 V for VDDIO $\leq$ 3.3 V.

Voltage level converter: Voltage level converter receives the control signal UP with voltage level of 3.3 V and outputs the complementary signals Q and QB. When VDDIO = 5.0 V and UP = 0 V, NM405 and NM406 are turned on, and Q is discharged through PM402, NM405, and NM406. Because Vbias is 1.7 V, Q would be clamped at 2.5 V (= 1.7 V + $|V_{th,PM402}|$). It turns on PM406 and pulls QB to 5.0 V. By contrast, Q and QB are biased at 5.0 V and 2.5 V, when UP = 3.3 V, respectively. When VDDIO = 0.9 $\sim$ 3.3 V and UP = 0 V, Q is discharged to 0 V through NM407, NM408, and NM406 such that QB is pulled to VDDIO (= 0.9 $\sim$ 3.3 V) by PM406. Similarly, when UP = 3.3 V, Q and QB are biased at 0.9 $\sim$ 3.3 V and 0 V, respectively.

Vg2 generator: Vg2 generator is composed of a Level converter and Logic switches. The Level converter is similar to the Voltage level converter, which receives the control signal UP, and outputs a level-shifted signal V_Z at 2.5 V when VDDIO = 5.0 V and UP = 0 V. For VDDIO = 0.9 $\sim$ 3.3 V, V_Z would be equal to UP. The state of logic switches would bias Vg2 at V_Z or not depending on the control signal OE and V_{PAD}. When OE = 0 V (receiving mode) and V_{PAD} = 5.0 V, PM441 is turned off. Vg2 is determined by the Gate-tracking circuit, and the logic switch NM441 and PM441 would protect the gates of the internal transistors from the high voltage of 5.0 V.

Dynamic driving detector: When VDDIO = 5.0 V, VL is biased at 0 V such that PM451 in on and PM452 is off. Then Vg4 is biased at 3.3 V through PM451. When VDDIO = 0.9 $\sim$ 3.3 V, PM451 is off and PM452 is on such that Vg4 is pulled to VDDIO through PM452. Therefore, Vg4 can be biased at the voltage shown in Fig. 2.

Gate-tracking circuit: In the receiving mode, the Gate-tracking circuit would monitor V_{PAD}. When V_{PAD} = 5.0 V, PM206 would be turned on and Vg2 can be pulled up to 5.0 V through PM206 such that the leakage current path through PM202 is avoided. In the transmitting mode, PM207 would be turned on for VDDIO = 5.0 V. Then, the gate voltage of PM206 will be biased at 5.0 V such that V_{PAD} can not affect Vg2.

Floating N-well circuit: The Floating N-well circuit receives the control signals VL, OE, Dout, and V_{PAD}. Besides the output, Vnwell, which is similar to the traditional floating N-well voltage to trace V_{PAD} in the receiving mode, another output Vnwell2 can trace V_{PAD} when transmitting logic 1. Hence, the body effect on PM202 can be removed and the driving strength is improved. When VDDIO = 0.9 $\sim$ 3.3 V and logic 1 is transmitted, the gate of PM252 is biased at 0 V such that Vnwell2 is equal to V_{PAD}. Therefore, the N-well voltage of PM202 can trace its drain and source voltage and the body effect is eliminated. At the same time, Vnwell is biased at 3.3 V by PM253. When 5.0 V is transmitted, the gate of PM252 is biased at 3.3 V. PM251 and PM252 would be turned on such that Vnwell and Vnwell2 are both biased at 5.0 V by V_{PAD}. The leakage currents through the parasitic diodes of PM202 and PM206 can be avoided. Similarly, Vnwell and Vnwell2 can be biased at 5.0 V for V_{PAD} = 5.0 V in the receiving mode through PM251 and PM252, respectively. For other cases in the receiving mode, Vnwell and Vnwell2 are biased at 3.3 V through PM253, and PM254 as well as PM255, respectively.

Input buffer: The Input buffer is composed of a traditional high voltage input buffer, which can receive the input signal with high voltage without any gate oxide overstress, and a Logic calibration circuit. By tuning the aspects of the the transistors, the traditional high-voltage input buffer can even receive 1.8 V input signal. However, when V_{PAD} = 0.9 V or 1.2 V, Vi2 would be biased at 3.3 V and Din is at 0 V, since the switching voltage of Pi2 and Ni2 is higher than 1.2 V. The logic error can be resolved by adding the logic calibration circuit, which is similar to the traditional high-voltage input buffer. When V_{PAD} = 1.2 V or 0.9 V, Vi3 is biased at 3.3 V to turn on Ni7 such that Vi2 can be pulled to 0 V by Ni7 and the feedback loop composed of Pi1, Pi2, and Ni2. Then, the logic error can be resolved.

ESD protection circuit: PM221 and NM222 form the ESD protection circuit, which is to improve the ESD strength from PAD to VDD.

III. Implementation and Simulation

The proposed design is implemented using a typical 0.35 μm 2P4M CMOS process. Fig. 4 reveals the layout of the proposed I/O buffer. The area is 497 $\times$ 111 μm^2. Fig. 5 shows the simulation waveform of Vg1, Vg2, Vg4, and Vnwell2 in the transmitting mode. These voltages are verified to satisfy the requirements shown in Fig. 2. Fig. 6 shows Vg2, Vnwell, and

Vnwell2 in the receiving mode. Vg2, Vnwell, and Vnwell2 could be pulled high to 5 V for V_{PAD} = 5 V by the Gate-tracking circuit and the Floating N-well circuit. Fig. 7 shows the output signal at the maximum speed for various VDDIO at the worst-case corner of [SS model, 100^{o}C]. The maximum output speed is 110/125/110/80/50/20 MHz for VDDIO = 5.0/3.3/2.5/1.8/1.2/0.9 V given a load of 20 pF. The worst duty cycle is 54.5% for VDDIO = 1.8 V at 80 MHz. Fig. 8 shows the input signal Din and V_{PAD}. The Input buffer can convert V_{PAD} with different voltage to a 3.3 V signal. The maximum static average power consumption of the proposed I/O buffer is 553 nW at the simulation corner of SS model and 100^{o}C when VDDIO = 5.0 V. Table I shows the comparison with several prior works.

IV. Conclusion

A 0.9 V to 5.0 V mixed-voltage-tolerant I/O buffer is proposed in the paper. By eliminating the body effect of the output PMOS by a novel Floating N-well circuit and equalizing the turn-on voltage for output PMOS and NMOS, the proposed I/O buffer can output the signal with almost 50% duty cycle even with 0.9 V level in 0.35 μm CMOS process. Besides, the static power consumption of the proposed design is only 553 nW by using the Low power clamping bias.

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		Transmitted signal			Received signal		
	Process	VDDH	VDD	VDDL	VDDH	VDD	VDDL
IO1 in [2]	0.25 μm CMOS	No	Yes	No	Yes	Yes	No
IO2 in [2]	0.25 μm CMOS	No	Yes	No	Yes	Yes	No
IO in [6]	0.13 μm CMOS	Yes	No	No	No	No	No
Ours	0.35 μm CMOS	Yes	Yes	Yes	Yes	Yes	Yes

Note : [1] The VDDH/VDD in [2] are 5/2.5 V, respectively.
[2] The VDDH/VDD in [6] are 3.3/1.0 V, respectively. And it is only a output buffer.
[3] VDDL = 2.5/1.8/1.2/0.9 V in this work.

TABLE I
COMPARISON WITH SEVERAL PRIOR WORKS

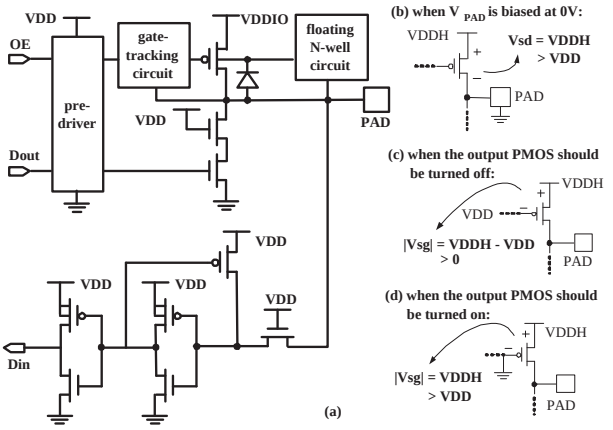


Fig. 1. A typical mixed-voltage-tolerant output buffer and the problems when VDDIO is biased at VDDH.

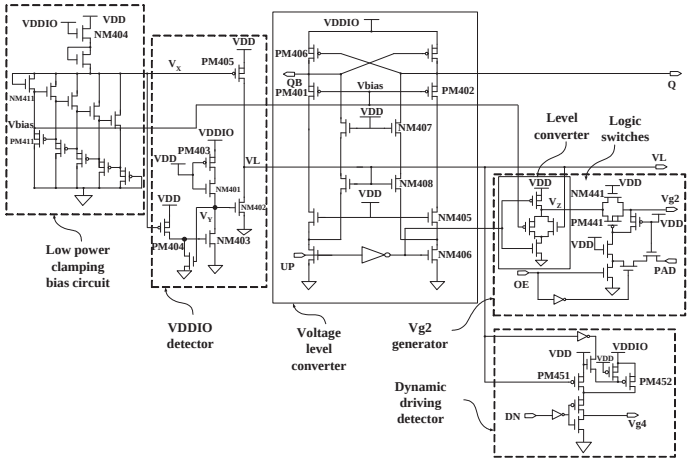


Fig. 3. The proposed Dynamic gate bias generator.

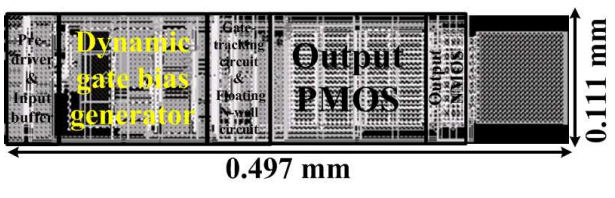
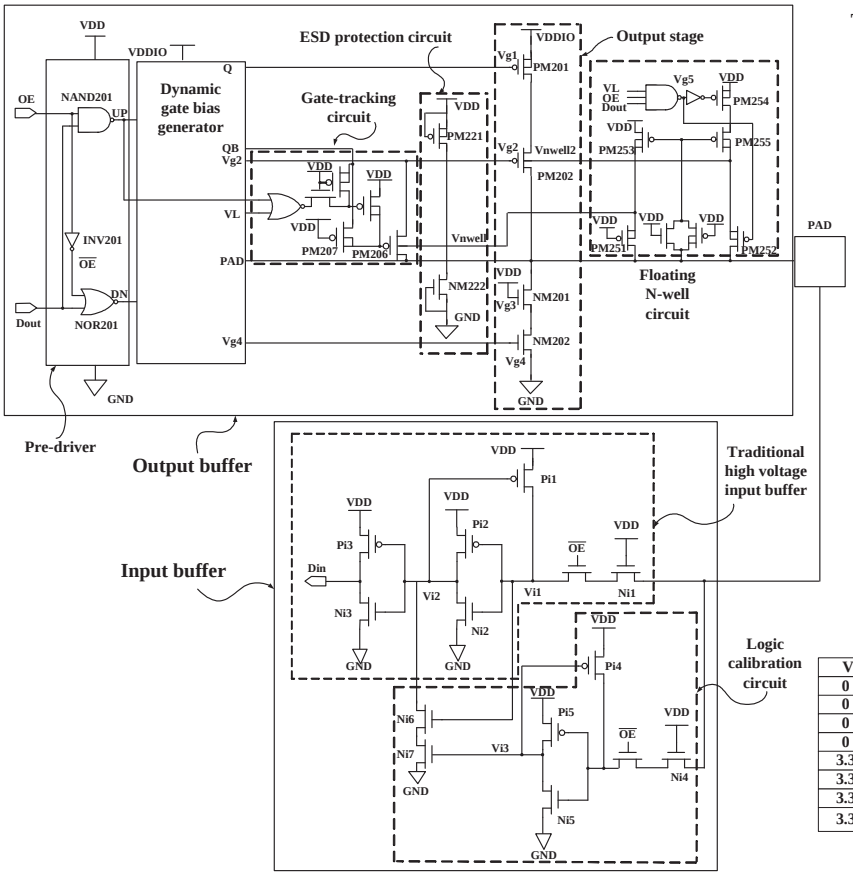


Fig. 4. Layout of the proposed design.



Truth table for gate voltages of the Output stage.

Operating mode	VDDIO	Vg1	Vg2	Vg3	Vg4
Receiving mode	0.9 V	0.9 V	3.3/5.0 V*	3.3 V	0 V
	1.2 V	1.2 V	3.3/5.0 V*	3.3 V	0 V
	1.8 V	1.8 V	3.3/5.0 V*	3.3 V	0 V
	2.5 V	2.5 V	3.3/5.0 V*	3.3 V	0 V
	3.3 V	3.3 V	3.3/5.0 V*	3.3 V	0 V
	5.0 V	5.0 V	3.3/5.0 V*	3.3 V	0 V
Transmitting mode (logic 1/0)	0.9 V	0/0.9 V	0/3.3 V	3.3 V	0/0.9 V
	1.2 V	0/1.2 V	0/3.3 V	3.3 V	0/1.2 V
	1.8 V	0/1.8 V	0/3.3 V	3.3 V	0/1.8 V
	2.5 V	0/2.5 V	0/3.3 V	3.3 V	0/2.5 V
	3.3 V	0/3.3 V	0/3.3 V	3.3 V	0/3.3 V
	5.0 V	>1.7/5.0 V	>1.7/3.3 V	3.3 V	0/3.3 V

*When V_{PAD} = 5 V, Vg2 must be biased at 5 V in the receiving mode.

Truth table for the outputs of Voltage level converter.

VDDIO	UP	VL	Q	QB
5.0 V	0 V	0 V	2.5 V	5.0 V
	3.3 V		5.0 V	2.5 V
3.3 V	0 V	3.3 V	0 V	3.3 V
	3.3 V		3.3 V	0 V
2.5 V	0 V	3.3 V	0 V	2.5 V
	3.3 V		2.5 V	0 V
1.8 V	0 V	3.3 V	0 V	1.8 V
	3.3 V		1.8 V	0 V
1.2 V	0 V	3.3 V	0 V	1.2 V
	3.3 V		1.2 V	0 V
0.9 V	0 V	3.3 V	0 V	0.9 V
	3.3 V		0.9 V	0 V

Truth table for the outputs of Floating N-well circuit.

VL	OE	Dout	DN	Vg5	Vnwell	Vnwell2
0 V	0 V	0 V	0 V	3.3 V	5.0 V	5.0 V
0 V	0 V	3.3 V	0 V	3.3 V	5.0 V	5.0 V
0 V	3.3 V	0 V	3.3 V	3.3 V	5.0 V	5.0 V
0 V	3.3 V	3.3 V	0 V	3.3 V	5.0 V	5.0 V
3.3 V	0 V	0 V	0 V	3.3 V	3.3 V	3.3 V
3.3 V	0 V	3.3 V	0 V	3.3 V	3.3 V	3.3 V
3.3 V	3.3 V	0 V	3.3 V	3.3 V	3.3 V	3.3 V
3.3 V	3.3 V	3.3 V	0 V	0 V	3.3 V	Tracing V_{PAD}

Fig. 2. The proposed mixed-voltage-tolerant I/O buffer.

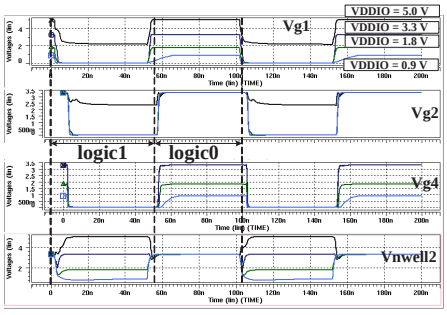


Fig. 5. Simulated waveform of Vg1, Vg2, Vg4, and Vnwell2 in the transmitting mode at 10 MHz for the corner of [SS, 100^{o}C].

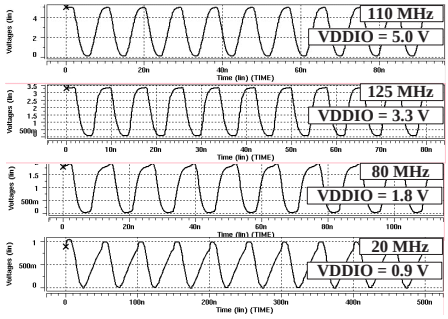


Fig. 7. Output signals at maximum speed for different VDDIO given for a 20 pF load at the worst simulation corner of [SS, 100^{o}C].

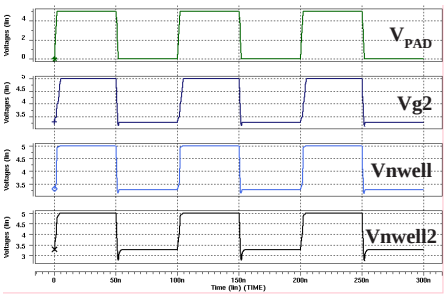


Fig. 6. Simulated waveform of V_{PAD}, Vg2, Vnwell, and Vnwell2 in the receiving mode at 10 MHz for the worst simulation corner of [SS, 100^{o}C].

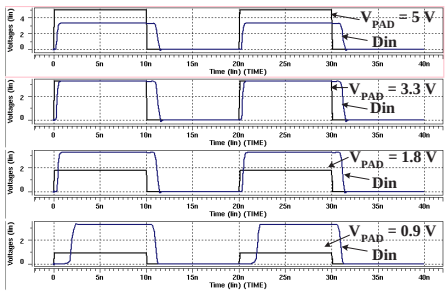


Fig. 8. Simulated input signals Din and V_{PAD} at 50 MHz for a 0.5 pF load.