Power-saving Nano-scale DRAMs with An Adaptive Refreshing Clock Generator[§]

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***Abstract*— An adaptive refreshing circuitry design for DRAMs is presented in this work. The proposed refreshing circuitry uses a voltage comparator to monitor the voltage drop caused by the data loss of a memory cell that results from leakage currents in order to dynamically adjust the refreshing period of the memory cell. Besides, a process variation monitor is also included in the proposed design to compensate the process drifting problem. Therefore, the proposed design is insensitive to temperature variations as well as process drifts. The period of the refreshing clock is automatically adjusted to save a great portion of standby power of DRAMs. A 4-Kb DRAM is implemented by a typical 0.13-μm 1P8M digital CMOS process. The post-layout simulation verifies the correctness of the adaptive refreshing cycles generated by the proposed design.**

Keywords : DRAM, adaptive refreshing circuitry, voltage comparator

I. Introduction

The trend toward portable and small digital equipments or systems is rapidly booming [1]. Hence, the reduction of data retention power of DRAMs is one of the major targets in memory designs [3], [5]. Self-refreshing methodology perhaps is the most widely used scheme to reduce the data retention power. However, extending the refreshing period which has been considered an effective way to reduce the data retention power can not catch up the evolution of the number of memory cells which is increased four times every generation. It is very difficult to extend the data retention time by four times every generation, since the cell size and the supply voltage are scaled in nano-meter technology. Besides, prior self-refreshing methods are either mode selection schemes [2], [3], [4], [8] or by pseudo-SRAM schemes [5], [6]. They are still vulnerable to the temperature variations as well as the process drifts such that they are unable to adjust the refreshing period automatically. Fig. 1 shows the voltage drop of the data loss of a memory cell at different temperature and process scenarios. It reveals that the speed of voltage drop of memory cell between different corners have very significant difference. If the refreshing cycle is determined by the worst case, too much power would be consumed. In this paper, we present an adaptive refreshing design for DRAMs by monitoring the voltage drop of the data loss in the memory cell. As soon as the voltage drop reaches to a reference voltage, a refreshing signal is triggered to boost the data back to its original voltage level. Hence, the refreshing period will not depend on any mode selection. When the temperature varies or the process drifts, the refreshing period also changes accordingly.

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II. Adaptive Refreshing Circuitry

Most of the prior self-refreshing designs for DRAMs are focused on the mode selection in which certain monitoring mechanism detects a few parameters and then initiate one of several oscillators with pre-determined refreshing periods. However, this scheme is very prone to the temperature variations. Technically, when the temperature rises or the process is at FF corner, the leakage current goes up drastically. A short refreshing period, then, is required. It is opposite when the temperature drops or the process shifted to the SS corner.

A. Adaptive Refreshing Datapath

A simple though to initiate a refresh cycle is to monitor a specific parameter which is supposed to be varied with the temperature and the process corner in order to avoid those drawbacks introduced by the prior works. Another consideration is that the data loss must be avoided, either. Hence, an effective way to initiate a refresh cycle is to monitor the voltage of the data in the memory cell. As soon as it drops to a reference voltage, the refresh cycle is triggered to recharge the cell to retain the data.

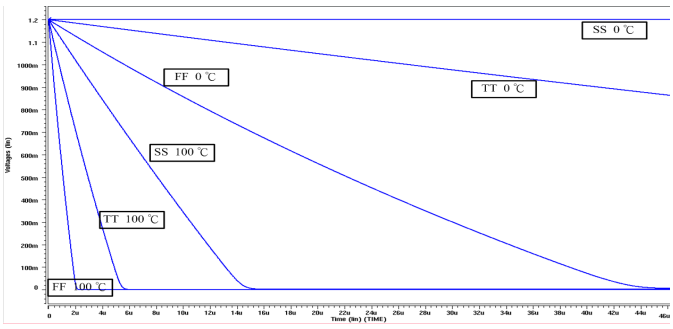


Fig. 1. Voltage drop of the data loss of a memory cell at different temperature and process scenarios

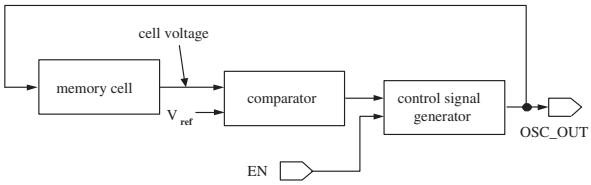


Fig. 2. Datapath of the proposed design

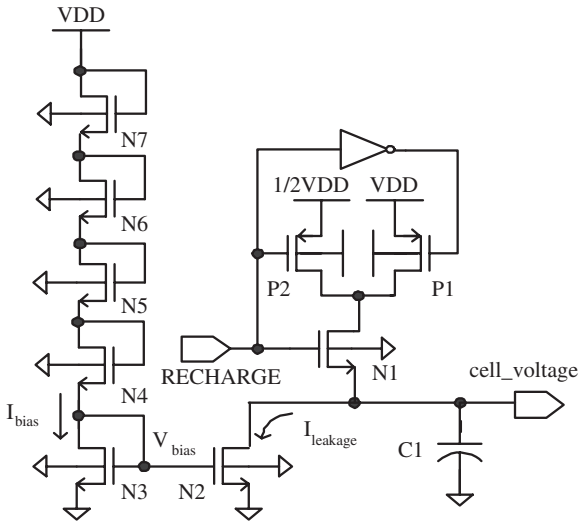


Fig. 3. Simulation circuit and results of the NB scheme

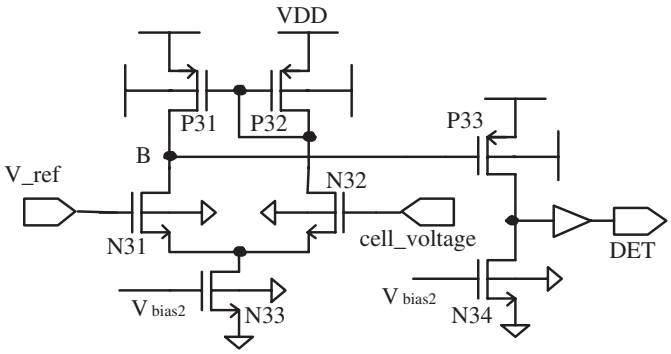


Fig. 4. Comparator

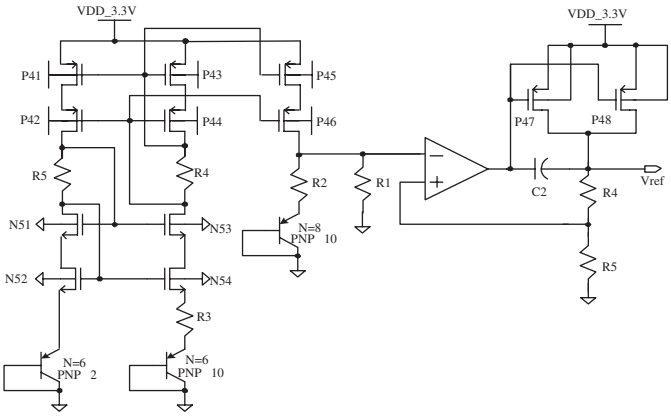


Fig. 5. Voltage regulator

Referring to Fig. 2, the datapath of the initiation of an adaptive refreshing cycle consists of a memory cell, a voltage comparator, and a control signal generator (CSG). The EN signal is to activate the control signal generator to start a recharging cycle. The inputs to the comparator are the output of the memory cell and one reference voltage, V_{ref}. The output of the CSG is feedback to restore the voltage of the memory cell such that the data loss is prevented. The key point of such a design is that since the leakage current of memory cell, $I_{leakage}$, is temperature and process corner dependent, the duration for the voltage of the memory cell affected by the leakage current also depends on temperature and process corner. This leads to the entire self-refreshing design is adaptive.

B. Circuitry of the datapath

1) Memory cell: The memory cell and the emulated leakage current source are shown in Fig. 3. As soon as the RECHARGE is high, P1 and N1 are turned on to refresh the data at C1. If RECHARGE is low, N1 is off. In the meantime, the cascode load of N4 $\sim$ N7 supplies a tiny current which is roughly in the range of the leakage current and the subthreshold current. The N2 and N3 consist of a current mirror to mimic the data degradation. The charge at C1 will be leaked via N2 of which the gate is driven by the current mirror [7]. Notably, the voltage drop of C1 must be faster than that of a real DRAM cell to ensure the correctness of the memory cell.

Assume that $T_{refresh}$ is the duration for the cell to restore its voltage level. Meanwhile, there are a total of n rows in the memory. Thus, the refreshing duration for each row becomes $\frac{T_{refresh}}{n}$. Hence, in order to speed up the self-recharging, the N2 and N3 might be added purposedly.

2) Comparator: A voltage comparator, as sown in Fig. 4, is required to monitor the voltage drop of the cell. A 0.75 V voltage is applied to V_{ref} as the reference voltage. P31, P32, N31, N32, and N33 consist of a differential amplifier of which inputs are the voltages of the cell and V_{ref}. As soon as the cell voltage drops to V_{ref}, node B is pulled down to turn on P33 such that a high strobe is generated at DET given N34 is properly biased.

3) Voltage regulator: In order to provide a stable V_{ref}, i.e., insensitive to temperature and power variations and process drifts, a voltage regulator is required. Fig. 5 shows the voltage regulator which is composed of a bandgap circuit, OPAMP, and PMOS transistors. The post-layout simulations prove that all supply voltage (2.97 V $\sim$ 3.63 V), model (FF, TT, and SS), and temperature ($0^oC \sim 100^oC$) corner, the output voltage drift of the regulator is less than ± 3.6 %.

4) CSG: Referring to Fig 6, the schematic of the CSG is illustrated. The external EN signal is detected by the rise edge detector (RED) to validate the DET signal fed by the comparator. NAND2 and NAND3 consist of a SR latch which

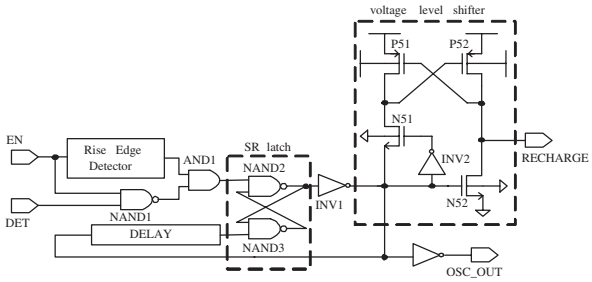
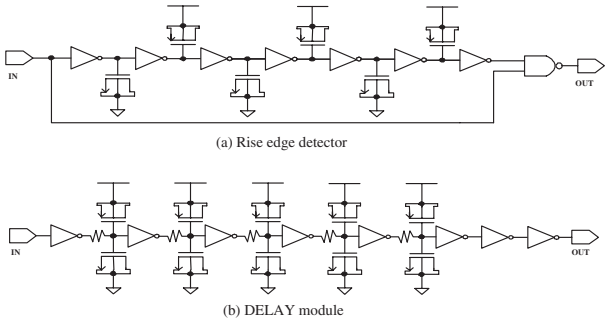


Fig. 6. Schematic of the CSG



(a) Rise edge detector

(b) DELAY module

Fig. 7. Rise edge detector and DELAY module

extends the length of the valid strobe by the DELAY module. A voltage level shifter comprising P51, P52, N51 N52, and INV2 to boost the RECHARGE to be VDD + V_{th}. Notably, the power supply of the shifter is VDD + V_{th} instead of VDD owing to that the recharging path is via a NMOS, N2 in Fig 3, to the data cell, C1. Thus, the voltage at RECHARGE must be VDD + V_{th} to restore C1 back to VDD. The RED module and the DELAY module are shown in Fig. 7.

III. Simulation and Implementation

In order to verify the robustness of the proposed adaptive refreshing design, we carry out the implementation of a 4-Kb DRAM by using TSMC (Taiwan Semiconductor Manufacturing Company) 0.13 μm 1P8M CMOS process. Fig. 8 is the layout of the overall 4-Kb DRAM with the proposed self-recharging circuitry. We have simulated every transistor model, including FF, FS, TT, SF, and SS, at a variety of temperatures, e.g., 0^{o}C, 25^{o}C, 50^{o}C, 70^{o}C, and 100^{o}C, to attain the refreshing performance. Fig. 9 shows the worst-case post-layout simulation waveforms of the adaptive refreshing circuitry given FF model, 100^{o}C. Fig. 10 shows the refreshing cycles in different corners. It is obvious that the refreshing period is adaptive according to the temperature and process variations. Fig. 11 shows the simulation waveforms of the read, write, and refreshing operation. Notably, read, write, refresh, and sense amplifier signal are active high, while wordline and column signal are active low. If refreshing occurs when read is executing, the DRAM will be read first then refresh. The simulation results show the correct functionality of the proposed design. Although Table I only shows the comparison of the refreshing period of FF-modeled (worst model) MOS transistors, the performance of the other models are very much alike. Table II shows the comparison with our prior work. It is obvious that the proposed design possesses smaller power consumption than the prior work.

TABLE I

Comparison of the refreshing period of FF-modeled MOS transistors

	0^{o}C	25^{o}C	50^{o}C	75^{o}C	100^{o}C
$T_{refresh}$ μs	9	5.7	3.9	2.9	2.6

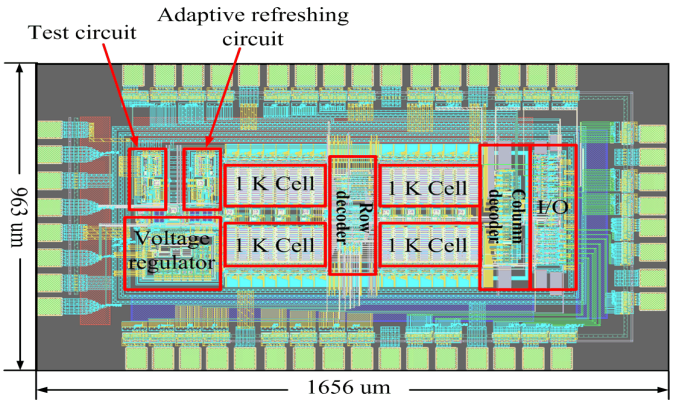


Fig. 8. Layout of the 4-Kb DRAM design

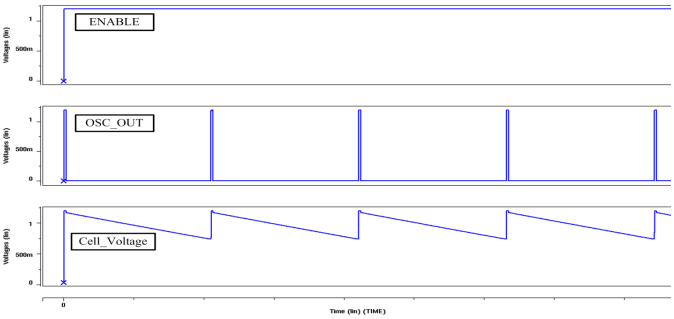


Fig. 9. Worst-case post-layout simulation waveforms of the adaptive refreshing circuit given FF model, 100^{o}C

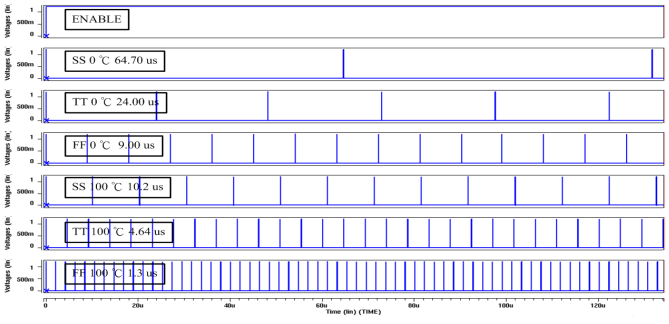


Fig. 10. Refreshing cycles in different corners

TABLE II

COMPARISON WITH PRIOR WORK

	[9]	Proposed design
CMOS process	2P4M 0.35 μm	1P8M 0.13 μm
Memory capacity	1 Kb	4 Kb
Function	Temperature insenetive	Temperature and process insenstive
VDD	3.3 V	1.2 V
Max. operation freq.	10 MHz	20 MHz
Avg. power	12.602 mW	0.963 mW
Power reduction (Memory capacity ratio $\times$ Voltage scaling $\times$ Energy operation scaling $\times$ Operation freq. scaling)	2.54$\times$ (0.25 $\times$ 7.56 $\times$ 2.69 $\times$ 0.5)	1$\times$ (1 $\times$ 1 $\times$ 1 $\times$ 1)
Scale power	4.96 mW	0.963 mW

$$\text{Memory capacity ratio} = \frac{\text{Memory capacity of the prior design}}{\text{Memory capacity of the proposed design}}$$

$$\text{Voltage scaling} = \left(\frac{\text{VDD of the prior design}}{\text{VDD of the proposed design}}\right)^2$$

$$\text{Energy operation scaling} = \left(\frac{\text{Process of the prior design}}{\text{Process of the proposed design}}\right)$$

$$\text{Operation freq. scaling} = \left(\frac{\text{Operation freq. of the prior design}}{\text{Operation freq. of the proposed design}}\right)$$

$$\text{Scaled power} = \frac{\text{Avg. power}}{\text{Power reduction}}$$

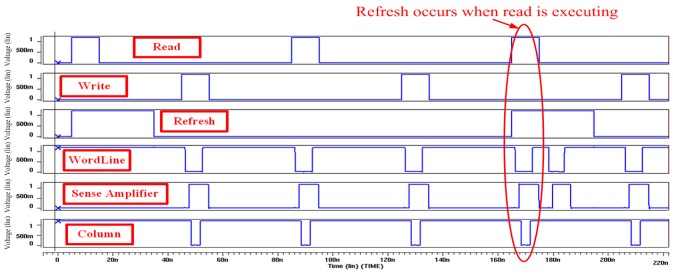


Fig. 11. Simulation waveforms of the read, write, and refreshing operation

IV. Conclusion

A novel adaptive refreshing oscillator design is proposed to be added at DRAMs. The shortcoming of the pre-determined refreshing cycles in prior works is removed. The proposed design is proposed to be temperature and process insensitive. On top of these advantages, the power dissipation will also be reduced since the unwanted refreshing cycles no long exist.

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References

[1] B. Prince, "Semiconductor memories," New York: Wiley, 1991.

[2] T. Kirihata, P. Parries, D. R. Hanson, H. Kim, J. Golz, G. Fredeman, R. Rajeevakumar, J. Griessemer, N. Robson, A. Cestero, B. A. Khan, G. Wang, M. Wordeman, and S. S. Iyer, "An 800-MHz embedded DRAM with a concurrent refresh mode," *IEEE J. Solid-State Circuits,* vol. 40, no. 6, pp. 1377-1387, June 2005.

[3] Y. Idei, K. Shimohigashi, M. Aold, H. Noda, H. Iwai, K. Sato, and T. Tachibana, "Dual-period self-refresh scheme for low-power DRAM's with on-chip PROM mode registers," *IEEE J. Solid-State Circuits,* vol. 33, no. 2, pp. 253-259, Feb. 1998.

[4] J. Kim, M. C. Papaefthymios, "Block-based multi-period refresh for energy efficient dynamic memory," *14th Annual IEEE Inter. ASIC/SOC Conference Proceedings,* pp. 193-197, 2001.

[5] T. Janik, E. Liau, H. Lorenz, M. Menke, E. Plaettner, J. Scheden, H. Seitz, and E. Vega-Ordonez "A 1.8V p(seudo)SRAM using standard 140nm DRAM technology with self adapting clocked standby operation," *2006 IEEE inter. Symp. on Circuits and Systems Proceedings,* pp. 193-197, 2001.

[6] K. Takeda, Y. Aimoto, N. Nakamura, H. Toyoshima, T. Iwasaki, K. Noda, K. Matsui, S. Itoh, S. Masuoka, T. Horiushi, A. Nakagawa, K. Shimogawa, and H. Takahashi, "A 16-Mb 400-MHz loadless CMOS four-transistor SRAM macro," *IEEE J. of Solid-State Circuits,* vol. 35, no. 11, pp. 1631-1640, Nov. 2000.

[7] H. Yamauchi, T. Iwata, A. Uno, M. Fukumoto, and T. Fujita, "A circuit technology for a self-refresh 16Mb DRAM with less than 0.5μA/Mb data-retention current," *IEEE J. of Solid-State Circuits,* vol. 35, no. 11, pp. 1174-1182, Nov. 1995.

[8] H.-J Song, "A self-off-time detector for reducing standby current of DRAM," *IEEE J. of Solid-State Circuits,* vol. 32, no. 10, pp. 1535-1542, Oct. 1997.

[9] C.-C Wang, Y.-L. Tseng, and C.-C Chiu, "A temperature-insensitive self-recharging circuitry used in DRAMs," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems,* vol. 13, no. 3, pp. 405-408, March 2005.