1.8 V to 5.0 V Mixed-Voltage-Tolerant I/O Buffer With 54.59% Output Duty Cycle

Tzung-Je Lee*, *Student Member, IEEE*, Yi-Cheng Liu*, and Chua-Chin Wang*, *Senior Member, IEEE*
*Department of Electrical Engineering
National Sun Yat-Sen University
Kaohsiung, Taiwan

***Abstract*— This paper proposes a 1.8 V to 5.0 V mixed-voltage-tolerant I/O buffer. Unlike traditional mixed-voltage-tolerant I/O buffers, the proposed I/O buffer can transmit and receive the signal with high voltage level (VDDH) and low voltage level (VDDL) by employing an output stage composed of stacked PMOS and staked NMOS. Besides, an auxiliary charging circuit is employed to enhance the driving current I_{OH} due to the slow mobility and body effect of the stacked PMOS. With the auxiliary driving mechanism, the duty cycle can be improved to be 54.59% at the worst simulation corner of [SS, 100°C]. The maximum output speed is 90/90/125/90 MHz given a load of 20 pF for VDDIO = 1.8/2.5/3.3/5.0 V. Moreover, the maximum static power consumption is simulated to be 749.73 nW.**

I. Introduction

With the evolution of the CMOS technology, a PCB-based system might employ various chips implemented using different processes, which are operated at different supply voltages. Traditional I/O buffers would suffer from the hazards of the gate-oxide overstress, leakage current and the hot-carrier degradation in the receiving mode when a high voltage level (VDDH) is biased at the PAD [2]. Therefore, mixed-voltage-tolerant I/O buffers were presented to resolve these problems by using a gate-tracking circuit and a floating N-well circuit, as shown in Fig. 1 (a) [1]-[5]. However, when the supply voltage (VDDIO) for the output stage is biased at VDDH, Vsg or Vsd would be larger than the constrained voltage (VDD) in three scenarios, as shown in Fig. 1 (b)-(d). Thus, these traditional mixed-voltage-tolerant I/O buffers can not transmit the signals of high voltage level. Therefore, the applications would be limited.

In order to resolve these problems, this paper proposes a mixed-voltage-tolerant I/O buffer using stacked PMOS (PM201 and PM202) and stacked NMOS (NM201 and NM202) in the output stage and a Dynamic gate bias circuit for providing appropriate gate biases for PM201 and PM202, as shown in Fig. 2. However, the carrier mobility of the stacked PMOS is much slower than that of the stacked NMOS in current NMOS technology. Besides, the output PMOS PM202 possesses body effect in the transmitting mode. It reduce the driving current by the stacked PMOS such that I_{OH} would be much smaller than I_{OL}. Thus, the duty cycle of the output signal would be less than 50%. It might result in missing codes which should be avoided in most of digital systems. Thus, the proposed circuit employs an additional charging path of NM204 and NM203 to improve the duty cycle of the output signal to be almost 50% for VDDIO = 1.8/2.5/3.3/5.0 V.

II. 1.8 V to 5.0 V Mixed-voltage-tolerant I/O Buffer

Referring to Fig. 2, the proposed I/O buffer is composed of an Output stage, an Input stage, a Pre-driver, a Gate-tracking circuit, a Floating N-well circuit, and a Dynamic gate bias generator.

Pre-driver: The Pre-driver receives a mode-selection signal OE and an output signal Dout from the core and outputs two control signals, UP and DN, to control the Output stage. OE determines the I/O buffer in the transmitting mode or in the receiving mode, as shown in the truth table in Fig. 2.

Output stage: The Output stage is composed of a stacked PMOS pair (PM201 and PM202), a stacked NMOS pair (NM201 and NM202) and an auxiliary charging circuit (NM204 and NM203). In order to avoid the hazards revealed in Fig. 1, the gate voltages VG1 and VG2 should vary according to the operation mode and the choice of VDDIO, as shown in Fig. 3. In the receiving mode, VG1 would be biased at VDDIO to turn off PM201. VG2 would be pulled to 5 V by Gate-tracking circuit to avoid the leakage current through PM202 when V_{PAD} is biased at 5 V. When logic 0 is transmitted (OE = 3.3 V and UP = 0 V), VG1 and VG2 would be biased at VDDIO and 3.3 V, respectively. When logic 1 is transmitted (UP = 0 V), VG1 and VG2 is biased at the voltage larger than 1.7 V (= 5.0 V - 3.3 V) for VDDIO = 5.0 V. Thus, PM201 and PM202 could be turned on for transmitting logic 1 and the gate-oxide overstress at PM201 and PM202 is avoided. For VDDIO $\leq$ 3.3 V, VG1 and VG2 are both biased at 0 V to transmit logic 1. Notably, because the driving current of stacked PMOS is smaller than that of the stacked NMOS, NM204 should be turned on to provide another charging path through NM203, NM204, and NM201 when logic 1 is transmitted. Therefore, VG3 would be biased at 3.3 V for transmitting logic 1 and biased at 0 V for other cases.

Dynamic gate bias generator: The Dynamic gate bias generator is composed of a Low-power clamping bias circuit, a VDDIO detector, and a Voltage level converter.

Low power clamping bias circuit: The Low-power clamping bias circuit provides a DC bias Vbias for the Voltage level converter when VDDIO = 5.0 V. With five stages of serial PMOS and NMOS in a feedback loop, Vbias would be clamped at 1.7 V, which almost equals to four times of the threshold voltage of the NMOS. If Vbias is larger than 1.7 V, Vbias

would be discharged by PM315. If Vbias is smaller than 1.7 V, NM315 will be turned on to charge the node Vbias. Therefore, Vbias is clamped at 1.7 V without any DC leakage current and the static power consumption could be reduced to only 749.73 nW.

VDDIO detector: VDDIO detector outputs a detection signal VL for the Voltage level converter and the NOR2 logic gate for the Gate-tracking circuit such that the circuits can operate in different functions for various VDDIO. When VDDIO is biased at 5 V, PM303, NM301, and NM302 are turned on and NM304 is off such that the gate of NM303 would be pulled high. Hence, NM303 is turned on. Moreover, the gate of PM305 is biased at 3.3 V by NM303. Thus, VL is biased at 0 V for VDDIO = 5.0 V. When VDDIO $\leq$ 3.3 V, the gates of PM305 and PM304 are pulled low such that PM305 and PM304 would be turned on. Besides, PM303 is off and the gate of NM303 is discharged to 0 V by NM304, which is turned on by PM304. Thus, VL would be biased at 3.3 V for VDDIO $\leq$ 3.3 V and at 0 V for VDDIO = 5.0 V.

Voltage level converter: Voltage level converter receives the control signal UP and converts the voltage level of UP according to the detection signal VL and VDDIO. When VDDIO is biased at 5.0 V and UP is biased at 0 V, VG3 will be pulled to 3.3 V by PM310. Because VL is at 0 V, NM305 would be turned off. With Vbias at 1.7 V, VG1 would be discharged to 2.5 V through PM302, NM305, and NM307. QB is then pulled to 5.0 V by PM309. VG2 is biased at 2.5 V by NM308 and PM306. When UP is biased at 3.3 V, QB will be discharged to 2.5 V and VG1 will be pulled to 5.0 V. VG3 is then discharged to 0 V through NM316 and NM317. VG2 is biased at 3.3 V by PM308 and PM307. Because the gate of NM308 is biased at 2.5 V, which is smaller than its source and drain voltage, NM308 would be turned off. Thus, VG1 and VG2 will not affect each other.

When VDDIO $\leq$ 3.3 V and UP = 0 V, VG3 is biased at 3.3 V by PM310. With VL biased at 3.3 V, VG1 is discharged to 0 V through NM309, NM305, and NM307. QB is then pulled to VDDIO by PM309. VG2 would be discharged to 0 V by NM314 and NM308. When UP is biased at 3.3 V, VG3 would be discharged to 0 V. Similarly, VG1 and QB would be biased at VDDIO and 0 V, respectively. Moreover, VG2 will be pulled to VDDIO (= 1.8/2.5/3.3 V) by PM308 and PM307. Because the gate of NM308 is biased at 0 V, NM308 would be off. Then, VG1 and VG2 would not interfere each other.

High voltage protection circuit: The High voltage protection circuit protects the internal transistor from the high voltage of 5.0 V at the PAD in the receiving mode. When the I/O buffer operates in the transmitting mode, OE is biased at 3.3 V such that Vx would be discharged to 0 V by NM310 and NM311. It turns on PM307 and PM306 such that VG2 could be determined by the Voltage level converter as mentioned above. When the I/O buffer operates in the receiving mode, OE is at 0 V and NM311 is turned off. Vx is then determined by V_{PAD}. When V_{PAD} = 5.0 V, VG2 would be pulled to 5.0 V by the Gate-tracking circuit. The gate of PM307 and PM306 (Vx) is then biased at 5.0 V by PM316. Thus, PM307 and PM306 are turned off such that the internal transistors are protected from the high voltage of 5.0 V. When V_{PAD} is at 0/1.8/2.5/3.3 V, Vx would be discharged to 0/1.8/2.5/2.7 V by NM313, NM312, NM310 such that PM307 and PM306 would be turned on. Therefore, VG2 is biased at 3.3 V by the Voltage level converter.

Gate-tracking circuit: The Gate-tracking circuit detects V_{PAD} and provides a gate bias of 5.0 V for PM202 to avoid the leakage current through PM202 when V_{PAD} is biased at 5.0 V in the receiving mode. When the I/O buffer operates in the receiving mode, UP is biased at 3.3 V. The gate of PM503 is then biased at 0 V by NM501. Thus, PM503 is turned on such that the gate of PM502 would be biased at 3.3 V. Therefore, PM502 would be turned on to provide a 5.0 V for the gate of PM202 only when V_{PAD} = 5.0 V. In the transmitting mode, the gate of PM503 would be biased at 0 V due to VL at 3.3 V. Similarly, the gate of PM502 would be biased at 3.3 V by PM503. Therefore, PM502 is off. If VDDIO = 5.0 V, VL would be at 0 V such that PM503 is turned off. Then, QB of 5.0 V could be sent to the gate of PM502. It turns off PM502 even when logic 1 (= 5.0 V) for VDDIO = 5.0 V. Therefore, VG2 will not be affected by V_{PAD} in the transmitting mode.

Floating N-well circuit: The Floating N-well circuit provides a dynamic N-well bias Vnwell for PM202 and PM502 to avoid the leakage current through the parasitic diode in PM202 and PM502 when V_{PAD} = 5.0 V. If V_{PAD} = 5.0 V, PM402 is turned off by PM403. Vnwell is biased at 5.0 V by PM401. For V_{PAD} = 0/1.8/2.5/3.3 V, PM402 would be turned on by NM401. At the same time, PM403 and PM401 are off. Therefore, Vnwell is biased at 3.3 V through PM402.

Input buffer: The Input buffer is a traditional high voltage receiver. It can receive high voltage (5.0 V) without gate-oxide overstress by the separation of Ni1 and the feedback loop of Pi1, Pi2, and Ni2. By carefully tuning the aspects of the transistors, the Input buffer can receive the signal with a voltage level of 1.8 V.

III. Implementation and Simulation

The proposed I/O buffer is implemented using TSMC (Taiwan Semiconductor Manufacturing Company) 2P4M 0.35 μm CMOS process. By using the Dynamic gate bias generator, the gate-oxide overstress is avoided with only one poly and thin devices used. Thus, the cost of process could be reduced. Fig. 5 shows the layout of the proposed I/O buffer. The area is 495 $\times$ 114 μm^2. Fig. 6 shows the gate voltages VG1, VG2, and VG3 for the Output stage and Vnwell in the transmitting mode at 10 MHz. VG1 and VG2 are biased at the voltage larger than 1.7 V for transmitting logic 1 when VDDIO is supplied to 5.0 V. When transmitting logic 0, VG1 is pulled to 5.0 V and VG2 is biased at 3.3 V. Besides, VG3 is pulled to 3.3 V to turn on the auxiliary charging circuit such that the driving current I_{OH} could be enhanced. Fig. 7 shows V_{PAD}, VG2, and Vnwell in the receiving mode. VG2 would be pulled to 5.0 V to turn off PM202 for VDDIO = 5.0 V. Thus, the leakage current through PM202 can be avoided. Similarly, Vnwell is pulled to 5.0 V to eliminate the leakage current through the parasitic diode in

PM202. Fig. 8 shows the waveform of the output signal at the maximum speed. For VDDIO = 1.8/2.5/3.3/5.0 V, the maximum speed of the output signal is simulated to be 90/90/125/90 MHz given a load of 20 pF at the worst case of [SS, 100^{o}C]. The worst duty cycle of the output signal is 54.59% for VDDIO = 5.0 V at 90 MHz at the simulation corner of SS model and 100^{o}C. Fig. 9 shows the waveforms of V_{PAD} and the input signal Din at 10 MHz. For the signal from 1.8 V to 5.0 V, Din is converted to be a 3.3 V signal. The maximum static power consumption is 749.73 nW in the worst simulation corner of [SS, 100^{o}C]. The performance comparison with prior works is shown in Table I.

IV. Conclusion

An additional charging current path is provided in the proposed I/O buffer to enhance the driving current I_{OH}. Therefore, the output duty cycle is merely 54.59% in the worst simulation case even when the stacked PMOS are employed in the Output stage. Besides, the gate-oxide overstress and leakage current path are avoided by using the Dynamic gate bias generator, the Gate-tracking circuit and the Floating N-well circuit. Therefore, the proposed I/O buffer can receive and transmit the signal with voltage level from 1.8 V to 5.0 V.

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		Transmitted signal			Received signal		
	Process	VDDH	VDD	VDDL	VDDH	VDD	VDDL
IO1 in [4]	0.25 μm CMOS	No	Yes	No	Yes	Yes	No
IO2 in [4]	0.25 μm CMOS	No	Yes	No	Yes	Yes	No
IO in [6]	0.13 μm CMOS	Yes	No	No	No	No	No
Ours	0.35 μm CMOS	Yes	Yes	Yes	Yes	Yes	Yes

Note : [1] The VDDH/VDD in [4] are 5/2.5 V, respectively.
[2] The VDDH/VDD in [6] are 3.3/1.0 V, respectively. And it is only a output buffer.
[3] VDDL = 2.5/1.8/ V in this work.

TABLE I
Comparison with several prior works

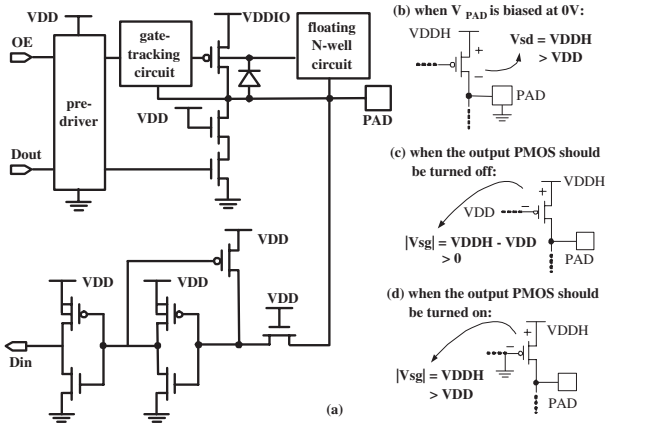


Fig. 1. A typical mixed-voltage-tolerant output buffer and the problems when VDDIO is biased at VDDH.

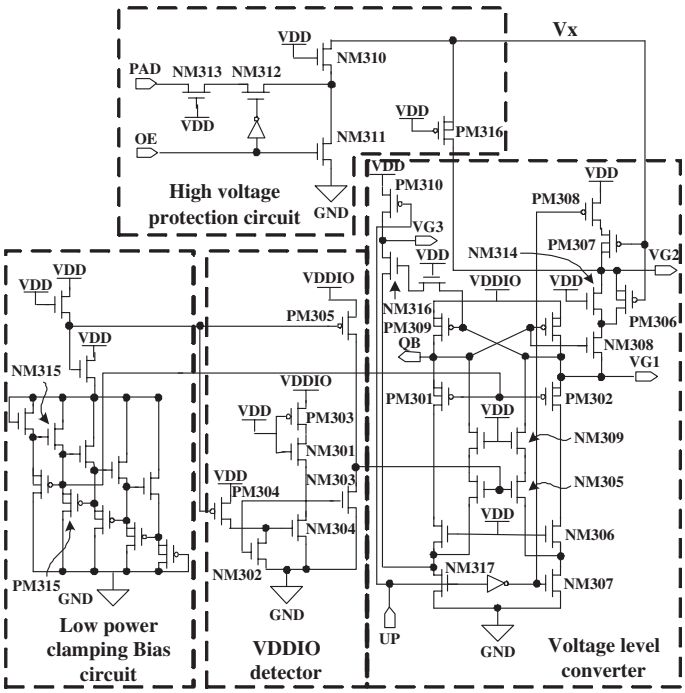
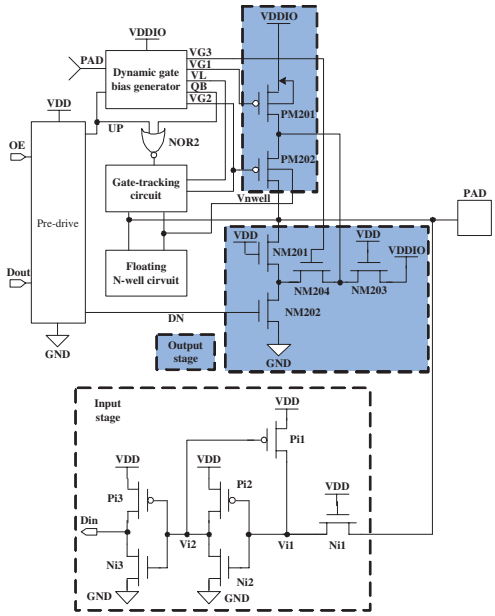


Fig. 3. The proposed Dynamic gate bias circuit.



The truth table for the Pre-driver

Operating mode	IN		OUT	
	OE	Dout	UP	DN
Receiving mode	0	0	1	0
	0	1	1	0
Transmitting mode	1	0	1	1
	1	1	0	0

The gate voltage for the Output stage :

Operating mode	VDDIO	VG1	VG2	VG3
Receiving mode	5 V	5 V	3.3 V/5 V*	0 V
	3.3 V	3.3 V	3.3 V/5 V*	0 V
	1.8 V	1.8 V	3.3 V/5 V*	0 V
Transmitting mode logic1/0	5 V	>1.7 V/5 V	>1.7 V/3.3 V	3.3 V/0 V
	3.3 V	0 V/3.3 V	0 V/3.3 V	3.3 V/0 V
	1.8 V	0 V/1.8 V	0 V/1.8 V	3.3 V/0 V

*When V_{PAD} = 5 V, VG2 must be biased at 5 V in the receiving mode.

The truth table for the Dynamic gate bias generator :

VDDIO	UP	VL	VG1	VG2	VG3	QB
5 V	0 V	5 V	2.5 V	2.5 V	3.3 V	5 V
	3.3 V		5 V	3.3 V/5 V*	0 V	2.5 V
3.3 V	0 V	3.3 V	0 V	0 V	3.3 V	3.3 V
	3.3 V		3.3 V	3.3 V/5 V*	0 V	0 V
1.8 V	0 V	3.3 V	0 V	0 V	3.3 V	1.8 V
	3.3 V		1.8 V	3.3 V/5 V*	0 V	0 V

*When V_{PAD} = 5 V, VG2 must be biased at 5 V in the receiving mode.

Fig. 2. The proposed mixed-voltage-tolerant I/O buffer.

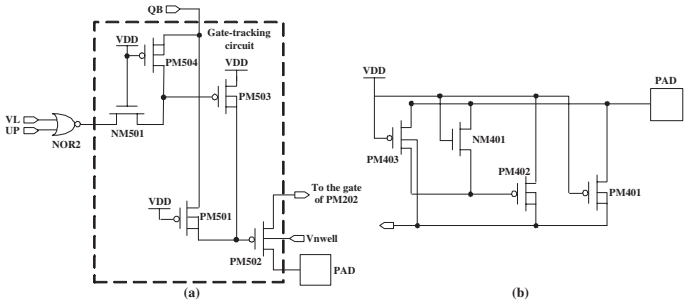


Fig. 4. Schematic of (a) Gate-tracking circuit and (b) Floating N-well circuit.

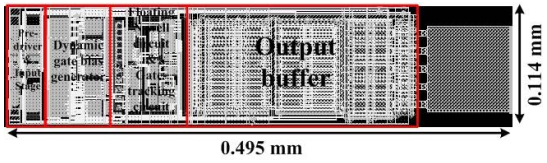


Fig. 5. Layout of the proposed design.

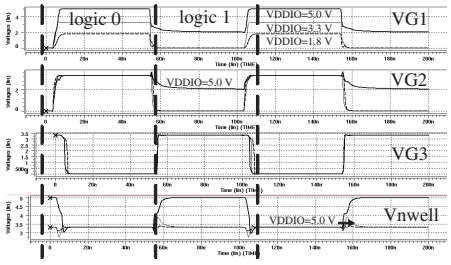


Fig. 6. Simulated waveforms of VG1, VG2, VG3, and Vnwell in the transmitting mode at 10 MHz for the [SS, 100^{o}C] corner.

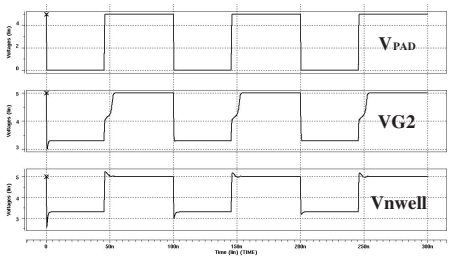


Fig. 7. Simulated waveforms of V_{PAD}, VG2, and Vnwell in the receiving mode at 10 MHz for the worst simulation corner of [SS, 100^{o}C].

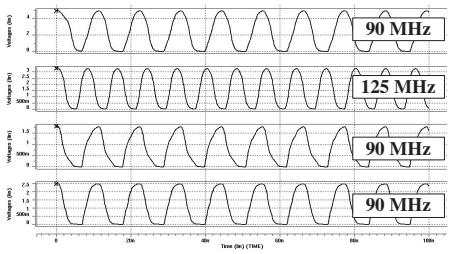


Fig. 8. Output signals at maximum speed for different VDDIO given a 20 pF load at the worst simulation corner of [SS, 100^{o}C].

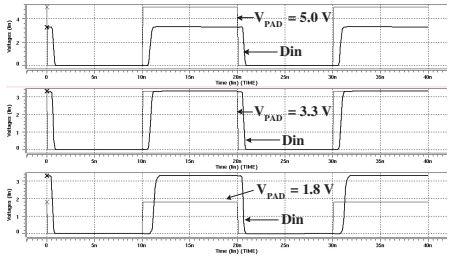


Fig. 9. Simulated input signals Din and V_{PAD} at 50 MHz for a 0.5 pF load.