Mixed-Voltage-Tolerant I/O Buffer Using a Clamping Dynamic Gate Bias Generator

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***Abstract*— A mixed-voltage-tolerant I/O buffer implemented in CMOS 2P4M 0.35 μm process is proposed in this paper. By using a clamping dynamic gate bias circuit, which possesses the ability of low-power DC bias generation using clamping transistor in feedback loop, VDDIO detection, and level shift, the proposed design can transmit and receive digital signals with voltage levels of 5/3.3/1.8 V without any gate-oxide overstress and leakage current path. The maximum transmitting speed of the proposed I/O buffer is simulated to be 142/166/100 MHz given the load of 20 pF using HSPICE for VDDIO = 5/3.3/1.8 V, respectively.**

I. Introduction

Because of the development of CMOS technology, the supply voltage of the integrated circuit (IC) is scaled down to reduce power consumption. When these chips using different processes and supply voltages are integrated in a PCB-based system, conventional I/O buffers are no longer suitable to be the I/O interface due to the problems of gate-oxide reliability, hot-carrier degradation, and the undesirable leakage current paths from PAD to VDDIO (the supply voltage provided for the I/O PAD) [1]. The stacked-NMOS [1]-[3], NMOS blocking topologies [4], the gate-tracking and floating N-well circuits [3] have been used in I/O buffer to avoid these problems in the receiving mode when V_{PAD} = VDDH (the logic 1 signal with voltage level higher than VDD). However, these designs can only receive the signals with voltage level of VDD and VDDH such that the function is limited.

In order to transmit the signals at VDDH, the output buffers using stacked transistors and separate supply voltages for the cores and the output buffers were presented in [5]-[7], as shown in Fig. 1. The pre-driver is to decode the control signal (OE) and the output signal (Dout) to generate the UP and DN signals for the output stage. When VDDIO is biased at VDDH, the output buffer can transmit signals with high voltage. To avoid the gate-oxide overstress at MP2 and MN1, the gate voltages, Vg1, Vg2, and Vg3, must be biased at the appropriate levels to keep Vgd, Vgs, and Vds less than the allowed voltage for the transistors, denoted by $V_{allowed}$. For example, $V_{allowed}$ is equal to 3.3 V for the typical device using 0.35-μm process. When VDDIO is biased at high voltage level (VDDH), Vg1 and Vg2 must be larger than V_{limit} = VDDIO $-$ $V_{allowed}$ to turn on MP1 and MP2 such that logic 1 can be transmitted. Similarly, when VDDH is present at the PAD in the receiving mode, Vg3 must be larger than V_{PAD} $-$ $V_{allowed}$. Therefore, a bias circuit is required to generate the desired gate voltages for Vg2 and Vg3. Besides, a level converter is used to convert the UP signal from 0/VDD to V_{limit}/VDDIO for Vg1. Therefore, the bias circuit and level converter are the most important components in the mixed-voltage-tolerant I/O circuit. [5] employed a MOS resistor string to construct the bias circuits. However, using resistor string causes serious trade-off between area and static power consumption. [6] employed diode-connected MOS and charge redistribution topologies to generate the desired bias voltage. However, it requires several additional control signals to determine the operation state, and the generation of these signals are not mentioned in [6]. [7] employed the existing core power supply (VDD) for Vg2 and Vg3. Thus, no additional bias circuits are required. However, this method requires a large difference between VDDIO and VDD. Otherwise, the operating speed will be reduced because the output MOS can not be turned on entirely. Besides, MP1, MP2, MN1 and MN2 must be implemented using thicker devices such that the process cost is increased. Most importantly, these prior works did not consider the gate-oxide reliability for VDDIO or V_{limit} biased at VDDL.

Therefore, this paper proposes a mixed-voltage-tolerant I/O buffer using a dynamic gate bias generator. The proposed dynamic gate bias generator uses the MOS clamping topology to generate the desired DC bias. Hence, no static DC path exists in the proposed design. Moreover, the proposed dynamic gate bias generator can detect the operation modes according to different applied VDDIO, and convert the UP signal to the desired voltage levels. The proposed design is implemented using TSMC 2P4M 0.35 μm process. By using the proposed dynamic gate bias generator, the proposed design can keep the gate-oxide reliability in three supply voltage modes based on the simulation results. Moreover, all MOS transistors are implemented using just typical (thin gate-oxide) devices and only one poly is required. Thus, no additional mask is needed and the process cost can be reduced. Notably, VDDIO could be easily obtained from the existing voltage source in the system by engineers. Therefore, no excess cost will be increased. The only penalty is the additional power PADs for VDDIO.

II. Mixed-voltage-tolerant I/O Buffer

Fig. 2 shows the schematic of the proposed mixed-voltage-tolerant I/O buffer. The I/O buffer is composed of a Pre-driver, a Dynamic gate bias generator, an Output stage, an Input stage, a Gate-tracking circuit, a Floating N-well circuit, a

NMOS buffer control circuit, and a bonding PAD. With various applications, the supply voltage for the I/O buffer (VDDIO) might be 5/3.3/1.8 V depending on usages, while the supply voltage for the core (VDD) is always 3.3 V.

Pre-driver: OE is the control signal to determine whether the transmitting (OE = 3.3 V) or receiving (OE = 0 V) mode is selected, as shown in the truth table in Fig. 2. The signal Dout is sent by the cores and expected to be transmitted to the external driven devices in the transmitting mode. In the receiving mode, the signal Dout is ignored.

Input stage: Ni1 is to isolate any unexpected high voltage at the PAD to ensure the gate-oxide reliability. With the feedback loop by Pi1, Vi1 would be pulled up to the full swing to reduce the static power consumption. Therefore, if V_{PAD} = 5/3.3/1.8/0 V, Din = 3.3/3.3/3.3/0 V.

Output stage: Besides the topology of stacked PMOS and stacked NMOS, the appropriate gate voltages must be provided for MP1, MP2, and MN1 to keep the gate-oxide reliability and correct function. The required gate voltages for various modes are shown in Fig. 2.

Floating N-well circuit: Referring to Fig. 2, MP3, MP4, MP5, and MN4 consist of the Floating N-well circuit [1]. The Floating N-well circuit is to provide the N-well voltage for MP2 to avoid the leakage current path from the parasitic diodes.

Gate-tracking circuit: Referring to the required gate voltages shown in Fig. 2, Vg2 must be changed according to V_{PAD} in the receiving mode. Thus, the Gate-tracking circuit, as shown in Fig. 3, is proposed to detect V_{PAD} and to provide the appropriate Vg2 coupled from the proposed dynamic gate bias generator. With the logic composed of NOR2, MP21-MP23, and MN24, the gate voltage of MP24 will be biased at 5 V from QB in the transmitting mode for VDDIO = 5 V. Thus, MP24 can not be turned on. With the turned-off MP24, Vg2 is biased at 2.5 V through MN31 and MN32 in this case. In other cases, the gate voltage of MP24 will be at 3.3 V. Thus, Vg2 will be pulled to 5 V through MP24 only for V_{PAD} = 5 V in the receiving mode.

Dynamic gate bias circuit: Fig. 4 shows the schematic of the Dynamic gate bias circuit, which is composed of a Bias circuit, a VDDIO detector, and a Level converter.

The proposed Bias circuit employs the clamping MOSs in closed-loop mechanism. Because the transistors are only turned on when $|Vgs| > |V_{th}|$. By setting $V8 - V9 < V_{th,MN9}$ and $V9 - V10 < |V_{th,MP9}|$, V9 will be at a static voltage level with MN9 and MP9 in the off state. If V9 is too low, it will be charge through MN9. By contrast, if V9 is too high, it will be discharge by MP9. By choosing V_{th} of PMOS and NMOS in each stage, a stable static bias Vbias = V9 = 1.8 V will be obtained.

The VDDIO detector is to detect the different modes of VDDIO = 5 V and VDDIO = 3.3/1.8 V. Thus, the gate-oxide overstress when VDDIO is biased in 5 V can be avoided by using the detection signal. When VDDIO = 5 V, MP15, MN13, and MN15 are turned on such that VL is discharged to 0 V. MN13 is to isolate the 5-V VDDIO to destroy the gates of MN14, MN15 and the inverter. Because MN7 is turned on, MP16, MP13, and MN14 will also be switched off. When VDDIO = 3.3/1.8 V, the static V_X is smaller than $VDD - |V_{th,MP16}|$ and $VDD - |V_{th,MP13}|$, MP16 and MP13 will be turned on. Besides, MP15 is switched off because of VDDIO biased at 3.3/1.8 V. Thus, V_Y is discharged to 0 V because the positive feedback of INV3 and MN14. MN15 is then in the off state. VL is then pulled to 3.3 V. Therefore, the detection for VDDIO = 5 V and VDDIO =3.3/1.8 V is achieved.

The Level converter is based on the cross-coupling topology. The gates of MP17 and MP18 are cross-coupled to the drains of each other. This method used for level shift was presented in lots of previous works. However, the consideration for switching off any possible static leakage current paths and keeping the gate-oxide reliability for each transistors must be taken into account carefully in the mixed-voltage applications with different VDDIO modes. Because VL will be biased at 3.3 V for VDDIO = 3.3/1.8 V. When VDDIO = 3.3/1.8 V and UP = 0 V, Q is discharged to 0 V through MN17 and MN19. Simultaneously, QB is charged to 3.3/1.8 V through MP17. Similarly, Q and QB will be coupled to 3.3/1.8 V and 0 V, respectively, for UP = 3.3 V. When VDDIO = 5 V, MN18 and MN19 are turned off because VL = 0 V. Thus, Q is discharged to from MP20, MN21, and MN23 for UP = 0 V. Because Vbias is coupled to 1.8 V, Q will be discharged to 1.8 V + $|V_{th,MP20}|$, which is around 2.5 V. QB is then biased at 5 V by MP17. Contrarily, Q is at 5 V and QB is at 2.5 V for UP = 3.3 V. By using the detection signal VL, no leakage current path and gate-oxide overstress occur.

NMOS buffer controller: Because the driving ability of stacked PMOS is reduced drastically in the 1.8-V VDDIO mode. Thus, the NMOS buffer controller is employed to turn off 1/2 of total fingers of the output NMOS (MN3 in Fig. 2) to balance the rising time and falling time. Referring to Fig. 5, the NMOS buffer controller is composed of a bias circuit, and a 1.8-V detector. The bias circuit, which is based on the proposed bias circuit mentioned in Section 2, provides a 1.8 V voltage for MP29. Thus, when VDDIO = 5/3.3 V, MP29, MN29, and MP31 are turned on such that VG will be coupled to the control signal DN. When VDDIO = 1.8 V, MP29, MN26, MP28, MN28, MN29, and MP31 are turned off. At the same time, MN30 is turned on to pull VG to 0 V. The fingers of MN3 in the output stage are then turned off. Therefore, the driving ability is balanced.

III. Implementation and Simulation

The proposed mixed-voltage tolerant I/O buffer is carried out using TSMC (Taiwan Semiconductor Manufacturing Company) 2P4M 0.35 μm CMOS silicide process. Fig. 6 shows the layout of the proposed design. IO3 is the proposed I/O buffer, which has area of 0.526×0.1 mm^2. IO1 and IO2 are the I/O buffers for testing without the buffer controller included. For avoiding the latchup, double guarding is drawn around the transistors. Moreover, the ESD strength of the stacked NMOS with their width of 60 μm can up to 1 KV for HBM (human body model) [8]. In our design, the width of the stacked NMOS is 210 μm.

Thus, the ESD strength is predicted to be larger than 3 KV for HBM which is better than lots of commercial requirements (2 KV with HBM).

Fig. 7 reveals the simulated Vg1 in the receiving mode at different PVT corners. Vg1 is biased at VDDIO for VDDIO = 5/3.3/1.8 V, respectively. Thus, MP1 would be turned off. Fig 8 shows the simulated waveform of Vg2 in the receiving mode. As mentioned in Section 2, Vg2 is pulled up to 5 V to turn off the leakage current path through MP2 when V_{PAD} is biased at 5 V and stay at 3.3 V to avoid the gate-oxide overstress on MP2 for V_{PAD} at 3.3/1.8 V. Fig. 9 shows simulated Vg1 and Vg2 in different PVT corners in the transmitting mode. When VDDIO = 5 V, Vg1 is biased at VDDIO/2.5 V, and Vg2 is at ∼2.5/∼2.5 V for transmitting logic 0/1. When VDDIO = 3.3/1.8 V, Vg1 and Vg2 are both biased at VDDIO/0 V for transmitting logic 0/1. The maximum speed of the output signal is 142/166/100 MHz for VDDIO = 5/3.3/1.8 V, as shown in Fig. 10. The static power consumption for VDDIO = 3.3 V is simulated to be 532.3 nW given VDD = 3.63 V, FF model , and -20^{o}C. It proves that no any DC leakage current paths exist. A performance comparison with prior works are given in Table I. The proposed design is the only one which can transmit and receive the signal with different level of VDDH/VDD/VDDL.

IV. Conclusion

This paper proposes a mixed-voltage-tolerant I/O buffer implemented using 2P4M 0.35 μm process. In order to receive and transmit the signal with 5/3.3/1.8 V, the topology of stacked transistors is employed. Moreover, a dynamic gate bias circuit is proposed to provide the appropriate gate voltages for the output stage. Thus, only thin oxide device and one poly are required such that the design cost can be further reduced.

Acknowledgment

This research was partially supported by National Science Council under grant NSC 95-2221-E-110-113 and by Himax Technologies, Inc., under grant 95A20281. The authors would like to express their deepest gratefulness to CIC (Chip Implementation Center) of NARL (National Applied Research Laboratories), Taiwan, for their thoughtful chip fabrication service. The authors also like to thank "Aim for Top University Plan" project of NSYSU and Ministry of Education, Taiwan, for partially supporting the research. Moreover, the authors would also like to thank Mr. Wen-Yu Lo with Himax Technologies, Inc., for fruitful suggestions.

References

[1] C.-H. Chuang, and M.-D. Ker, "Design on mixed-voltage-tolerant I/O interface with novel tracking circuits in a 0.13-um CMOS technology," in *Proc. of IEEE Int. Symp. on Circuits and Systems, 2004,* vol. 2, pp. 577-580, May 2004.

[2] M. J. M. Pelgrom and E. C. Dijkmans, "A 3/5 V compatible I/O buffer," *IEEE J. Solid-State Circuits,* vol. 30, no. 7, pp. 823-825, July 1995.

[3] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Overview and design of mixed-voltage I/O buffers with low-voltage thin-oxide CMOS transistors," *IEEE Tran. On Circuits and Systems I: Regular Papers,* vol. 53, no. 9, pp. 1934-1945, Sept. 2006.

[4] M.-D. Ker, and S.-L. Chen, "Design of mixed-voltage I/O buffer by using NMOS-blocking technique," *IEEE J. Solid-State Circuits,* vol. 41, no. 10, pp. 2324-2333, Oct. 2006.

[5] G. P. Singh, and R. B. Salem, "High-voltage-tolerant I/O buffers with low-voltage CMOS process," *IEEE J. Solid-State Circuits,* vol. 34, no. 11, pp. 1512-1525, Nov. 1999.

[6] H. Sanchez, J. Siegel, C. Nicoletta, J. P. Nissen, and J. Alvarez, "A versatile 3.3/2.5/1.8-V CMOS I/O driver built in a 0.2-μm, 3.5-nm Tox, 1.8-V CMOS technology," *IEEE J. Solid-State Circuits,* vol. 34, no. 11, pp. 1501-1511, Nov. 1999.

[7] S.-L. Chen, and M.-D. Ker, "An output buffer for 3.3-V applications in a 0.13-μm 1/2.5-V CMOS process," *IEEE Trans. Circuits and Systems-II:Express Brief,* vol. 54, no. 1, pp. 14-18, Jan. 2007.

[8] M.-D. Ker and C.-H. Chung, "Electrostatic discharge protection for design for mixed-voltage CMOS I/O buffers," *IEEE J. Solid-State Circuits,* vol. 37, no. 8, pp. 1046-1055, Aug. 2002.

	Transmitted signal			Received signal		
	VDDH	VDD	VDDL	VDDH	VDD	VDDL
IO1 in [3]	No	Yes	No	Yes	Yes	Yes
IO2 in [3]	No	Yes	No	Yes	Yes	Yes
Ours	Yes	Yes	Yes	Yes	Yes	Yes

Note : VDDH/VDD in [3] are 5/2.5 V.

TABLE I

Comparison with several prior works

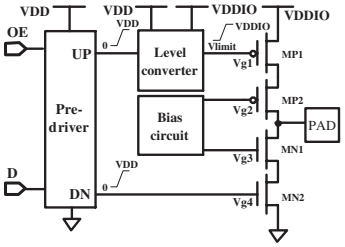


Fig. 1. A typical mixed-voltage-tolerant output buffer.

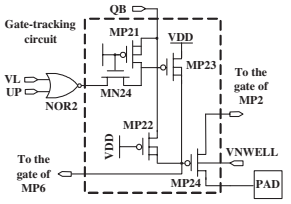


Fig. 3. The proposed gate-tracking circuit.

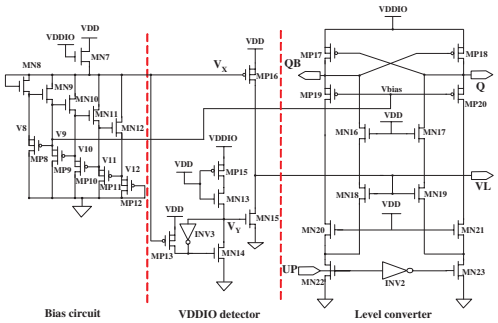
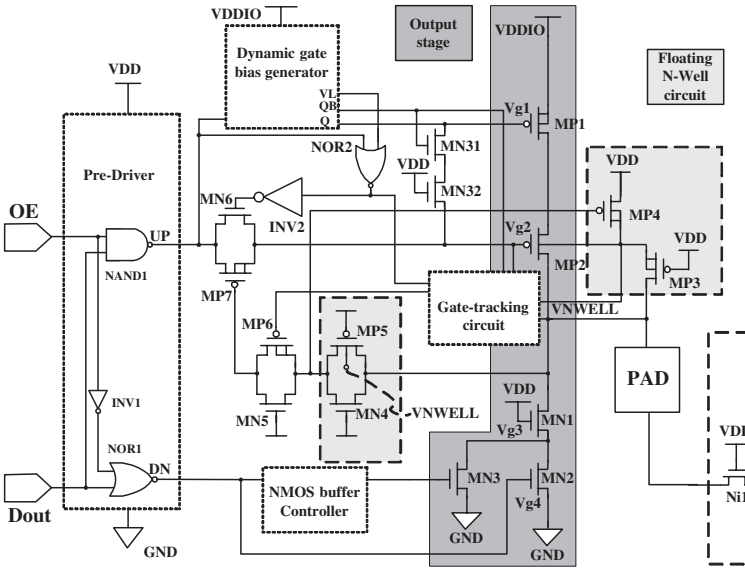


Fig. 4. The proposed dynamic gate bias generator.



Required gate voltages of output stage for various modes.					
Operating mode	VDDIO	Vg1	Vg2	Vg3	Vg4
receiving mode	1.8 V	1.8 V	3.3/5 V*	3.3 V	0 V
	3.3 V	3.3 V	3.3/5 V*	3.3 V	0 V
	5 V	5 V	3.3/5 V*	3.3 V	0 V
transmitting mode (logic 1/0)	1.8 V	0/1.8 V	0/3.3 V	3.3 V	0/3.3 V
	3.3 V	0/3.3 V	0/3.3 V	3.3 V	0/3.3 V
	5 V	>1.7/5 V	>1.7/3.3 V	3.3 V	0/3.3 V
*When VPAD = 5 V, Vg2 must be biased at 5 V in the receiving mode.					

Truth table for Pre-driver.				
Operating mode	OE	Dout	UP	DN
receiving mode	0	X	1	0
	0	X	1	0
transmitting mode	1	0	1	1
	1	1	0	0

Truth table for Dynamic gate bias generator.				
VDDIO	UP	VL	Q	QB
5 V	0 V	0 V	2.5 V	5 V
	3.3 V		5 V	2.5 V
3.3 V	0 V	3.3 V	0 V	3.3 V
	3.3 V		3.3 V	0 V
1.8 V	0 V	3.3 V	0 V	1.8 V
	3.3 V		1.8 V	0 V

Fig. 2. The proposed fully mixed-voltage-tolerant I/O buffer.

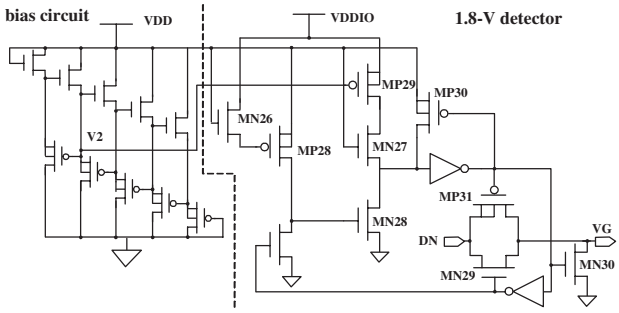


Fig. 5. The NMOS buffer controller.

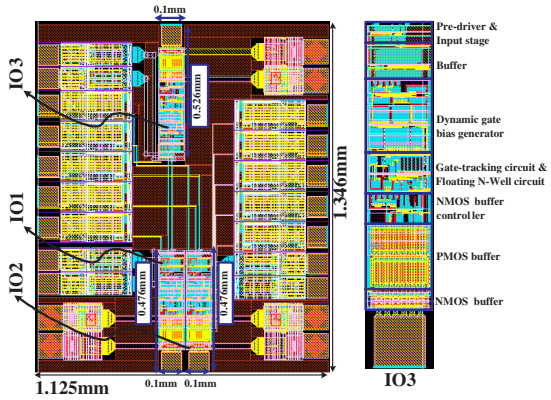


Fig. 6. Layout of the proposed fully mixed-voltage-tolerant I/O buffer.

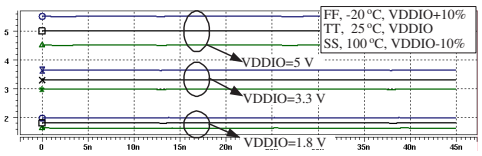


Fig. 7. The simulated waveform of Vg1 in receiving mode for different corners, [TT, 25^{o}C], [FF, -20^{o}C], [SS, 100^{o}C].

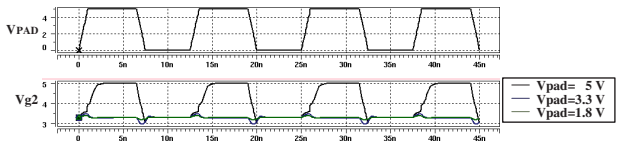


Fig. 8. The simulated waveform of Vg2 in receiving mode for different corners, [TT, 25^{o}C], [FF, -20^{o}C], [SS, 100^{o}C].

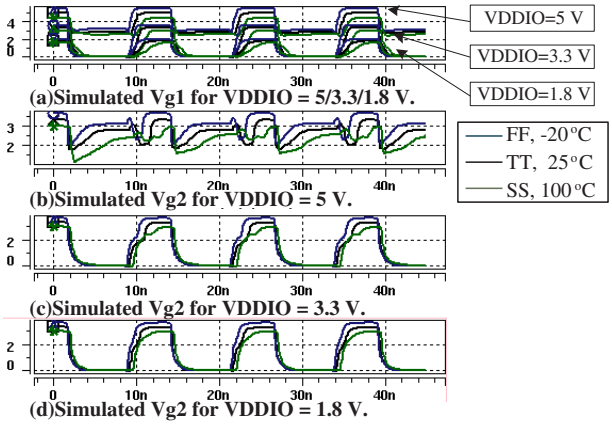


Fig. 9. The simulated waveforms of Vg1 and Vg2 in the transmitting mode for different corners, [TT, 25^{o}C], [FF, -20^{o}C], [SS, 100^{o}C].

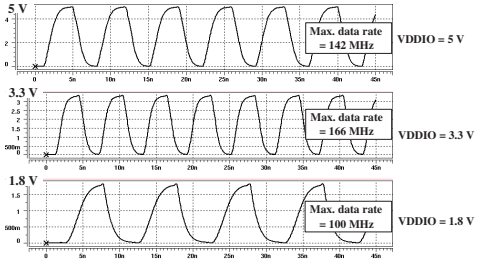


Fig. 10. The simulated output waveforms with the load of 10 pF at the corner of [SS, 100^{o}C].