A Low Power DDFS Design with Error Compensation Using A Nonlinear Digital-to-Analog Converter[§]

Jian-Ming Huang, *Student Member, IEEE,* Ching-Li Lee[†],
Jian-Ting Chen, and Chua-Chin Wang, *Senior Member, IEEE*
Department of Electrical Engineering
National Sun Yat-Sen University
Kaohsiung, Taiwan 80424
Email: ccwang@ee.nsysu.edu.tw

***Abstract*— This paper presents the architecture as well as the circuit implementation of a direct digital frequency synthesizer (DDFS) with error compensation. The proposed DDFS based on the straight line approximation with a 10-bit amplitude resolution. The proposed technique replaces the conventional ROM-based phase-to-amplitude conversion circuitry and the linear digital-to-analog converter with a nonlinear digital-to-analog converter (DAC). Thus, the overall power dissipation as well as hardware complexity can be significantly reduced. For a single 3.3-V supply, the maximum power dissipation is 3.37 mW at the clock rate of 385 MHz. The spurious free dynamic range (SFDR) of the synthesized sinusoid is -62.42 dBc at a 3 MHz output.**

Keywords : DDFS, nonlinear DAC, line approximation, current mode, error compensation

I. Introduction

The frequency synthesis is an essential part for communication systems. Conventionally, phase-locked loops (PLLs) are usually adopted to synthesize sinusoidal waves. However, PLL-based frequency synthesizers suffer from an inherent inability to simultaneously provide both fast frequency switching and high spectral purity [1]. In order to realize the fast frequency switching while keeping excellent spectral purity, the direct digital frequency synthesizer has been considered as an alternative other than PLL-based frequency synthesizers, since it does not have a feedback loop so as to provide fast frequency switching [9]. Besides, DDFSs are very much preferred in modern wireless communication systems owing to their additional superiority over PLL-based solutions, e.g., fine frequency resolution, continuous-phase frequency switching, and low phase noise [3].

Fig. 1 shows the conventional DDFS architecture which was firstly introduced in [4]. The digital phase information are converted into samples of sine amplitude by a ROM look-up table, and then the samples are passed to DAC and low pass filter (LPF) such that a sinusoid is generated. This architecture demands a very large ROM as the storage of sinusoidal amplitude parameters and consequently suffers from the inherent drawback of large power dissipation, large chip area, and slow speed. Even though the ROM size can be significantly reduced by truncating the output of the phase accumulator, the added spurious noise will degrade the spectral purity. Therefore, many prior researchers developed different techniques to reduce the ROM size, including interpolation-based method [5], approximation method [6]. The approximation method utilizes the mathematical approximation to obtain a sine function such that it only needs a small ROM or even no ROM. Furthermore, some approximation methods are suitable for analog signal processing. Therefore, the phase-to-amplitude conversion circuitry and the DAC in the Fig. 1 can be merged into a nonlinear DAC. According to the prior researches on the nonlinear-DAC-based DDFS [9], the reported power consumption as well as the die area are smaller than conventional DDFSs. In this paper, we use a nonlinear DAC to realize a simple approximation of the sine function. The prototypical DDFS with error compensation based on the proposed technique can achieve a 10-bit amplitude resolution with high output frequency and very low power.

II. Nonlinear DAC based DDFS design

A. Straight Line Approximation

Since a quadrant of sinusoid can be partitioned into n segments of straight lines. Provided that the straight line approximation is adopted to implement a DDFS with a j-bit phase accumulator, a quadrant of a synthesized sinusoid can be expressed as

$$y(x) = \begin{cases} m_0 x + b_0, & x_0 \le x < x_1 \\ m_1 x + b_1, & x_1 \le x < x_2 \\ \vdots & \\ m_{n-1} x + b_{n-1}, & x_{n-1} \le x < x_n \end{cases} \quad (1)$$

where x is the output of the selective complementor, and the range of x is $[0, \frac{2^{j-2}-1}{2^{j-2}}]$. By using quadrant symmetry, a

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[†] the contact author

complete sinusoid can be determined by merely n sets of slope m_i and intercept b_i. In digital designs, the coefficients m_i and b_i should be digitally represented and stored in ROMs, which lead to large power dissipation, large chip area, and low speed. Moreover, since the multiplication and addition can be easily implemented by analog current mode designs, we can select the appropriate m_i and b_i without considering the overhead of the hardware complexity.

Table I shows a nice selection of straight line approximation's coefficients, which are derived from the simulations by MATLAB of Mathworks. According to the chosen coefficients, we can use the straight line approximation to synthesize a sinusoid. The error between real sine function and the proposed approximation is illustrated in Fig. 2. The maximum error attained graphically is 0.0225. The SFDR of the proposed DDFS is poor without error compensation. In order to raise the SFDR, the errors in the Fig. 2 are classified into 10 intervals which correpond, individully, to 10 error compensation values. Thus, since the errors are equally normalized, the maximum error is reduced to be less than 0.1%. As a consequence, the approximation can achieve an amplitude resolution of 10 bits.

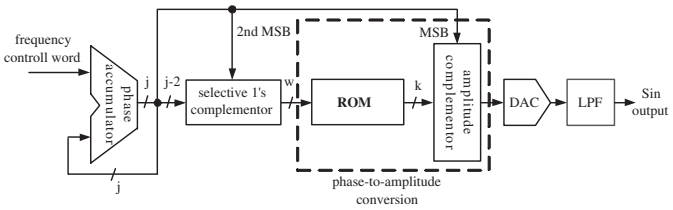

Fig. 1. Block diagram of the conventional DDFS

TABLE I

THE SELECTED COEFFICIENT

i	m_i	b_i	x
0	$3/2$	0.0196	$1/32 \sim 12/32$
1	1	0.2030	$13/32 \sim 23/32$
2	$1/2$	0.5414	$24/32 \sim 28/32$
3	$1/4$	0.7465	$29/32 \sim 32/32$

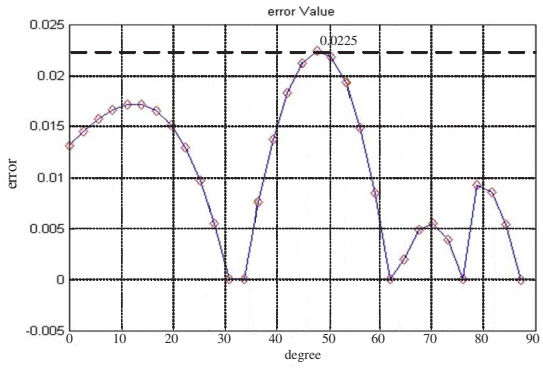

Fig. 2. Plot of the error between real sine function and synthesized sinusoid

B. Proposed DDFS Design

The architecture of the proposed DDFS based on the nonlinear DAC is shown in Fig. 3. It consists of the following building blocks : a phase accumulator (PA), a selective 1's complementor (SC), a nonlinear DAC with error compensation, and an analog complementor (AC). The PA controlled by the "frequency control word" is used to accumulate the digital phase count at each clock cycle. The most 2 significant bits of the PA output are used to address the quater-wave symmetry. Accordingly, the SC and the AC can contribute to produce the corresponding quadrants of the sine wave. The nonlinear DAC converts the digital phase count into the sine amplitude by the straight line approximation method. Owing to that the analog signal processing is realized more easily in current domain than in voltage domain, the nonlinear DAC is implemented as a current mode DAC. The output signal of the DAC is converted into a voltage signal by a termination resistor for the further processing. The most significant bit (MSB) from the output of the phase accumulator is adopted as a sign bit, and then the Gilbert multiplier generates the counterpart to completely synthesize the complete sine wave.

C. Nonlinear DAC Design

Fig. 4 shows the block diagram of the proposed nonlinear DAC, which is composed of six building blocks : current array (CA), decoder, slope current mirror (SCM), intercept current array (ICA), error compensation current array (ECCA), and bandgap. The CA converts the selective complement phase word, x, into a current signal. Then, the current signal is duplicated and multiplied by m_i through the SCM. The ICA generates the current signal, b_i. The ECCA generates the corresponding error compensation current, e_k, $0 \leq k \leq 10$. Hence, the straight line approximation is accomplished by summing the current signal $m_i x$,b_i, and e_k. The decoder sends the selecting signal to choose the corresponding slope, intercept, and compensation current according to x. The bandgap reference provides a stable temperature-insensitive reference for the current array.

D. Current Mirror Array

The settling time of the current mirrors decides the maximum operation clock rate and the maximum synthesized output frequency of the DDFS. A current mirror array as shown in Fig. 5 is the basic structure of the SCM, the ICA, and the ECCA. Pairs of true and complement digital signals select current mirror branches to decide each individual current in the mirror branch flowing through the load to synthesize sine wave or through the dummy resistor. Since the transistors in the current mirror branches are always on, the settling time of the current mirrors is drastically reduced.

Obviously, the accuracy of the current mirror circumscribes the performance of the analog signal processing. In our design, the mismatch due to the current mirroring should be less than 3.125% if the resolution of the approximation is chosen to be 5 bits ($\frac{1}{2^5} \approx 3.125\%$). The factors that affect the

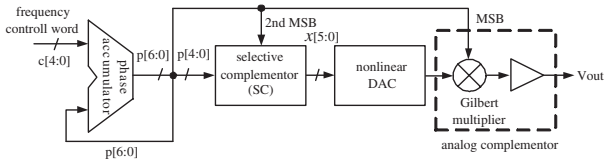

Fig. 3. The block diagram of the proposed DDFS

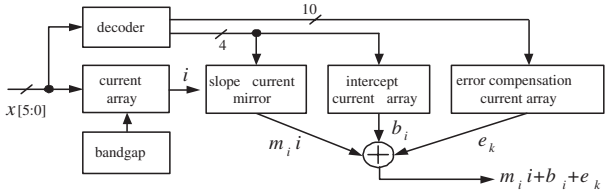

Fig. 4. The block diagram of the proposed nonlinear DAC

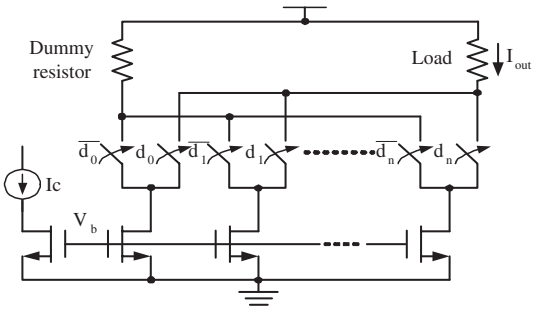

Fig. 5. Current mirror array

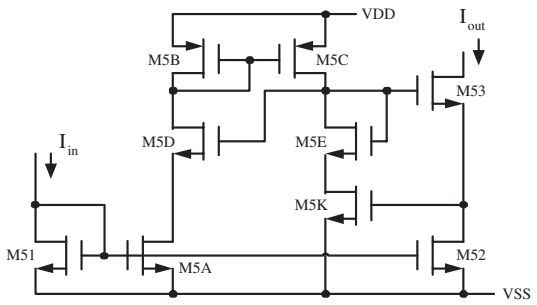

Fig. 6. The schematic of the IAFC current mirror

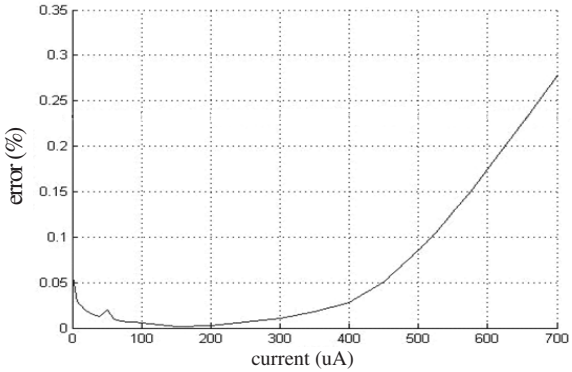

Fig. 7. The plot of current transfer error

accuracy of the current mirror include geometrical mismatch, technological parameter mismatch due to process gradient, and output impedance of the current mirror. The first two reasons can be alleviated by proper layout while the last one should be derived from the structure of the current mirror. Although the current mirrors based on a cascode structure have a higher output impedance, they suffer from the trade-off between the output impedance and the voltage swing. Besides, the output impedance can be improved by the aid of feedback. Fig. 6 shows the current mirror adopted in the nonlinear DAC, which is an improved active-feedback cascode (IAFC) current mirror [7]. The output stage of the IAFC current mirror is based on a regulated-gate cascode stage [8], which utilizes the active negative feedback loop composed of M5E, M5K and the source follower M53 to enhance the output impedance. The MOSFET M5B to M5E are used to make $V_{dsM5K} = V_{dsM5A}$. Thus, V_{gsM5A} will be equal to V_{gsM5K}, and the drain-to-source voltage of M51 and M52 will be the same. Fig. 7 shows the simulation result of the error of the current mirroring. The maximum error is below 0.3%, which is sufficient to meet the requirement of our design.

III. Simulation and Implementation

The proposed nonlinear DAC based DDFS prototype is carried out by TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm CMOS technology to verify the performance. All of the process corners : [0^{o}C, +100^{o}C], and (SS, TT, FF) models, are simulated. The layout of the proposed prototype is shown in Fig. 8. Fig. 9 shows the synthesized sinusoid at the clock rate of 385 MHz. Fig. 10 illustrates the spurious-free dynamic range (SFDR) of the synthesized sinusoid is -62.42 dBc at 3 MHz. The specifications of the proposed prototype is summarized in Table II. Table III shows a comparison between the proposed design and several prior works. It is note that the silicon area and the power consumption do not include accumulator and linear DAC in McEwan's work [11]. It is obvious that the proposed design possesses the edge of the highest output frequency, lowest power dissipation and the best SFDR among all DDFS designs.

IV. Conclusion

In this paper, we present a DDFS with error compensation design using a nonlinear DAC which is based on the straight line approximation. By using the proposed technique, the conventional ROM-based phase conversion circuitry and the linear DAC can be merged into one nonlinear DAC. The hardware complexity as well as power dissipation can be significantly reduced.

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TABLE III

COMPARISON BETWEEN THE PRIOR WORKS AND THE PROPOSED PROTOTYPE

	[9]	[10]	[11]	ours
Design methodology	Nonlinear DAC	Piecewise linear	Nonlinear interpolating	Nonlinear DAC
Technology (μm CMOS)	0.5	0.5	0.35	0.35
Power supply (V)	3.3	2.7	3.3	3.3
Max. clock rate (MHz)	230	130	50	385
Power consumption (mW)	92 (230 MHz)	8 (100 MHz)	0.4 (50 MHz)‡	3.37 (385 MHz)
Amplitude resolution (bits)	11	8	N/A	10
Active area (mm^2)	1.6	1.4	0.0085‡	1.721
SFDR (dBc)	55 @ 0.1 MHz	57.3 @ 0.1 MHz	50 @ 1 MHz	62.42 @ 3 MHz

‡ : The silicon area and the power consumption do not include accumulator and linear DAC.

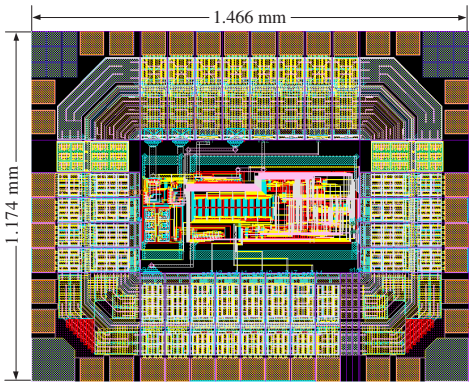

Fig. 8. The layout of the proposed prototype

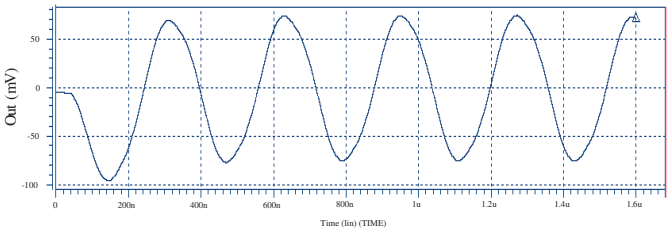

Fig. 9. The synthesized sine wave

TABLE II

SPECIFICATIONS OF THE PROPOSED DDFS

Technology	0.35 μm CMOS process
Power supply	3.3 V
Active area	1.174×1.466 mm^2
Phase resolution	7 bits
Amplitude resolution	10 bits
Max. clock rate	385 MHz
Power consumption	3.37 mW@385 MHz
SFDR	-62.42 dBc @ 3 MHz output freq.

chip fabrication service. The authors also like to thank "Aim for Top University Plan" project of NSYSU and MOE, Taiwan, for partially supporting this investigation.

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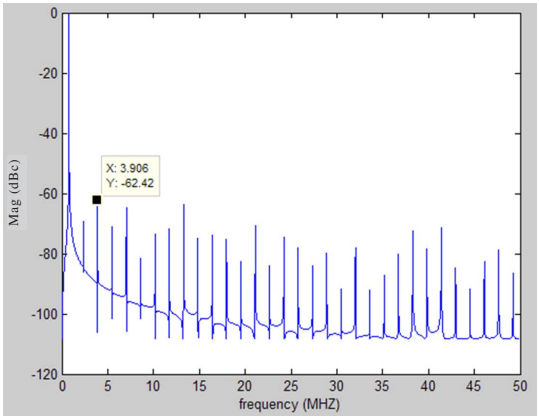

Fig. 10. The spectrum of the synthesized sine wave

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