A Direct Digital Frequency Synthesizer with CMOS OTP ROM[§]

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***Abstract*— A direct digital frequency synthesizer (DDFS) using on-chip CMOS one-time programmable read-only memory (OTP ROM) are presented. A straight-line approximation algorithm for sinusoid with compensation is adopted such that the accuracy could be maintained and the cost is reduced. Most important of all, a CMOS OTP ROM is employed as a look-up ROM table to simplify the ROM fabrication without any additional process steps. The proposed DDFS design is implemented using a typical 1P6M 0.18 μm CMOS process. It has a 12-bit amplitude resolution with 86.89 dB spurious free dynamic range (SFDR) using a small ROM size of 256 bits.**

***Keywords*—frequency synthesizer, DDFS, one-time programmable, OTP, straight-line approximation**

I. Introduction

The frequency synthesizer is an important part of a communication system, particularly in the receiver front-end, where sinusoidal signals are required to shift a high-frequency modulated input signal to an intermediate frequency (IF) band and then demodulate into a baseband signal [1]. The phase-locked loops (PLL) were employed for frequency synthesis traditionally. As the frequency is getting higher, the power consumption becomes a problem in a portable communication device. Compared with PLL, DDFS has faster frequency switching, higher resolution, better spectral purity, lower phase noise, and continuous-phase frequency switching. Moreover, DDFS allows direct phase and frequency modulation in the digital domain [2].

In prior DDFS researches, ROM-based (or namely table look-up) methods have been widely studied, e.g., [7], [8], and [10]. The conventional non-volatile ROM such as EPROM, EEPROM, and flash EEPROM, are manufactured with a special process. As the SOC evolving, the programmable non-volatile memory manufactured with typical logic CMOS process is strongly needed.

Many researches for OTP ROMs have been proposed. Most of them employed either fusing or anti-fusing technology [6], e.g., polyfusing, oxide-nitride-oxide (ONO) [3], metal-oxide-metal (MOM) [4], [5]. Polyfusing is not adaptable with process changing, while the ONO and MOM need additional process steps. Therefore, none of them is suitable for CMOS-based SOC. With the development of deep-submicron, the gate oxide of transistors becomes very thin which makes the break down very much easy. The transistor can be punched-through (anti-fused) without damaging other circuits. Then, OTP ROM on the CMOS process without any post-process is feasible. This kind of OTP ROM can be used to increase the flexibility and calibratablity of an ASIC or SOC after fabricated. In this paper, we propose a DDFS design using the straight-line approximation for quadrant sinusoid. The error compensation is carried out by a COMS OTP look-up ROM table to save the hardware cost.

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II. The Proposed DDFS Design

A. Compensated straight line approximation

A perfect sinusoidal wave is cyclic and symmetrical. It could be reconstructed with a quadrant waveform. The straight line approximation is deemed as one of the easiest algorithms to realize with digital circuitry. The classic straight line approximation is to approximate the quadrant sinusoid with n segment straight lines by choosing the closest slope m_i and intercept b_i. However, it will increase the cost of operating units to design a high accuracy DDFS in the classic way, if n becomes very large.

The proposed DDFS is divided in two parts, i.e., course approximation block (CAB) and fine approximation block (FAB). The low accuracy approximate waveform will be calculated in CAB part using straight line approximation. By contrast, the error compensation will be carried out by looking up a ROM table to get the waveform with high resolution in FAB part. The sinusoidal wave can be expressed as

$$y(x) = \begin{cases} (m_0 x + b_0)2^k + er_0(x), & x_0 \le x < x_1 \\ (m_1 x + b_1)2^k + er_1(x), & x_1 \le x < x_n \\ \vdots & \\ (m_{n-1} x + b_{n-1})2^k + er_{n-1}(x), & x_{n-1} \le x < x_n \end{cases}$$

where x is the output of the phase accumulator, while the m_i, b_i are the slope and intercept of each segment, respectively. The $er_i(x)$ is the error value of x to compensate the course

approximation. The k is the shift index for saving the number of multipliers.

B. DDFS design

Fig. 1 shows the block diagram of the proposed DDFS design. The phase accumulator (PA) translates the Frequency Control Word (FCW) into control signals of the other function block, P[6:0]. The first two bits of PA output (P[6:5]) are used to reconstruct the complete digital sinusoidal waveform in the quadrant state control (QSC) block. The other bits (P[4:0]) notify the CAB and FAB parts to calculate the quadrant approximate waveform magnitude, $y(x)$. The digital output, SINE, is the complete sinusoidal waveform approximation.

For example, if a DDFS with a 12-bit resolution is needed, k =6 is chosen. Table I is a good combination of coefficients in CAB part after detailed simulations. By Table I, CAB part calculates the course approximation as shown in Fig. 2. Then, we can derive each $er_i(x)$ by comparing it with the perfect sinusoidal waveform to build the look-up ROM table. The simulation result after error compensation is shown in Fig. 3. Fig. 4 shows the error value between the output waveform and the perfect waveform. Since the largest error value is about $0.000122 < 2^{12}$, the amplitude resolution of such a DDFS is 12 bits theoretically.

i	m_i	b_i	x
0	3	3	$0 \sim 11$
1	2	14	$12 \sim 21$
2	1	34	$22 \sim 29$
3	1	32	$30 \sim 31$

TABLE I
THE COEFFICIENT IN MSB PART.

C. CMOS OTP ROM

Generally, there is a huge equivalent resistance between two sides of gate oxide in a MOSFET fabricated by a standard CMOS process. If high voltage is applied on the gate of the MOSFET, breakdown occurs to reduce the equivalent resistance sharply. This characteristic makes the standard CMOS process possible to realize OTP ROM. As long as we can control the programming time and voltage, we can write the data in the OTP ROM by "anti-fusing" the gate oxide correctly without damaging other circuitry.

Referring to Fig. 5, the ROM cell is composed of three components : the storage element (SE), the high voltage blocking transistor (HVBT), and the data access transistor (DAT). In the programming mode, the target ROM cell will be selected by enabling word line (WL) and Data_in (DI). The gate voltage of the SE in the target ROM cell will be pulled high by VPP to anti-fuse the gate oxide. HVBT will be turned on to relay the programming voltage to ground via DAT. The Read_bar (RB), Data_in (DI), and Ready_to_Program (RTP) will be pulled high to ensure the current path of target ROM cell in programming mode. In the mean time, HVBT of other ROM cells will be cut off to prevent the programming voltage from damaging their data. In the reading mode. The binary digit stored in SE will be sensed from the current through the DAT, and differentiated by the sense amplifier (SA). In other words, the digit is stored in SE in a resistance state, which can be sensed by a transimpedance amplification. The OTP ROM cell array in the proposed design is shown in Fig. 6.

III. IMPLEMENTATION AND SIMULATION

TSMC (Taiwan Semiconductor Manufacturing Company) 0.18 μm 1P6M CMOS process is adopted to carry out the proposed chip design. The layout of the proposed design is shown in Fig. 7, The size of the chip core area is 841 μm $\times$ 1262 μm (1719 μm $\times$ 1883 μm with pads). Fig. 8 shows the 50 MHz output sinusoidal waveform. Test_Error is the output of a build-in self test, indicating the correctness of the proposed design. The FFT result of the waveform is shown in Fig. 9, where the spurious free dynamic range (SFDR) is 86.89 dB. The characteristics of the proposed design are tabulated in Table II. The proposed design has the smallest ROM size without sacrificing the amplitude resolution.

	[7]	[8]	[9]	[10]	Proposed Design
process (μm)	0.35	0.35	0.25	0.35	0.18
amplitude resolution (bits)	12	9	12	12	12
phase resolution (bits)	28	32	24	8	5
ROM size (bits)	448	368	N/A	3072	256
SFDR (dB)	84.2	55	80	78	86.89
MAX. input clock (MHz)	320	800	800	300	125

TABLE II
PERFORMANCE COMPARISON OF DDFSS.

IV. CONCLUSION

We have proposed a DDFS with a CMOS OTP ROM. The straight line approximation for the quadrant sinusoid has been adopted in addition to the error compensation with small look-up ROM table without any loss of resolution, the proposed DDFS design provides a better solution in terms of ROM size and SFDR.

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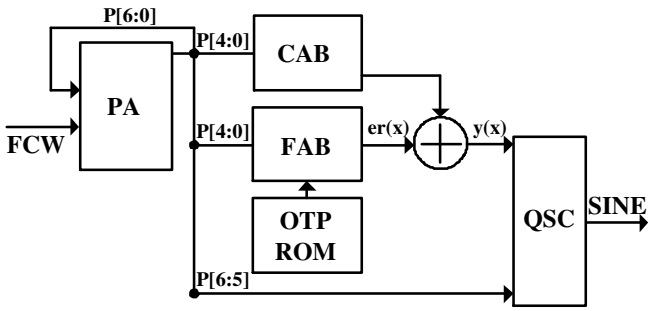

Fig. 1. The structure of the proposed DDFS.

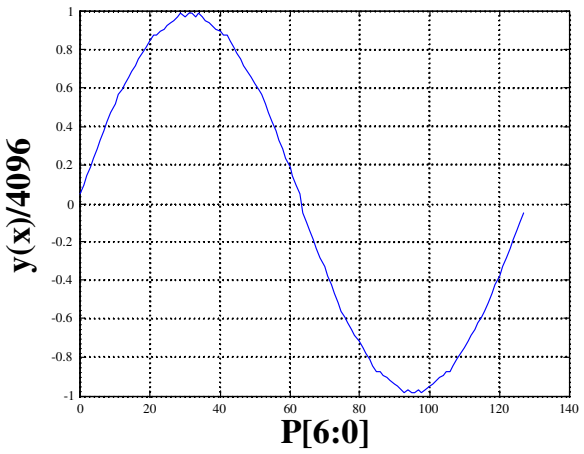

Fig. 2. The sinusoid approximation without error compensation.

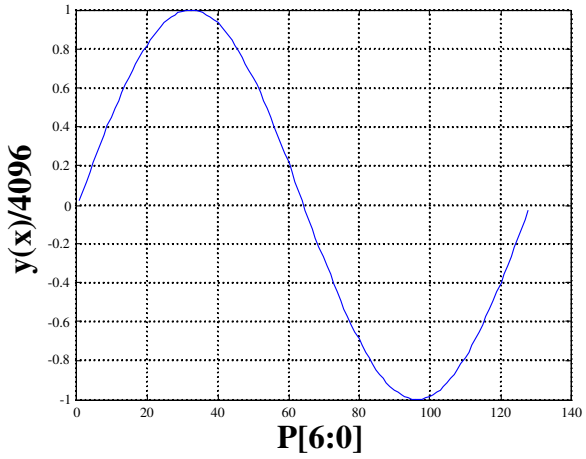

Fig. 3. The sinusoid approximation after compensation.

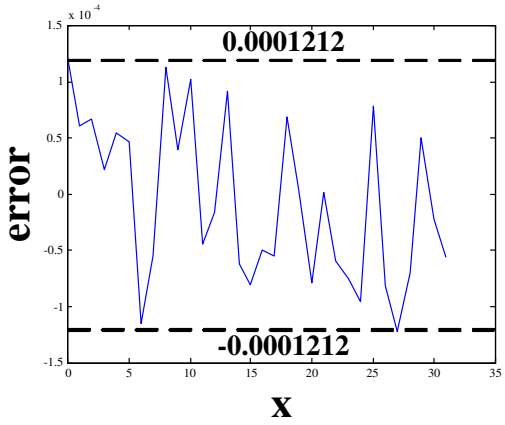

Fig. 4. The error between the perfect waveform and the output waveform.

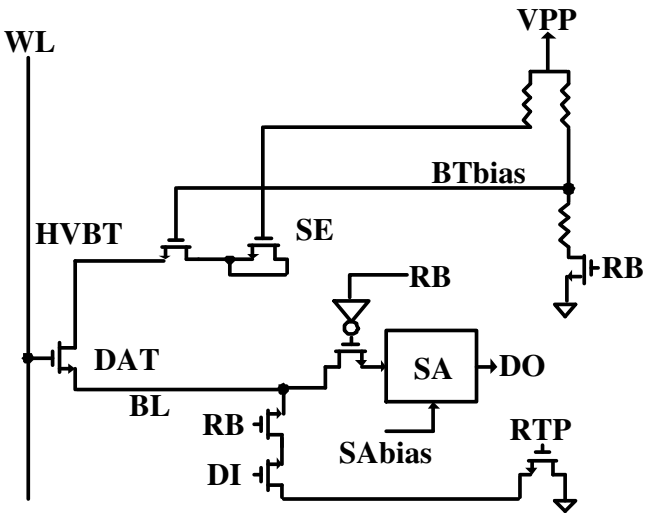

Fig. 5. The OTP ROM cell.

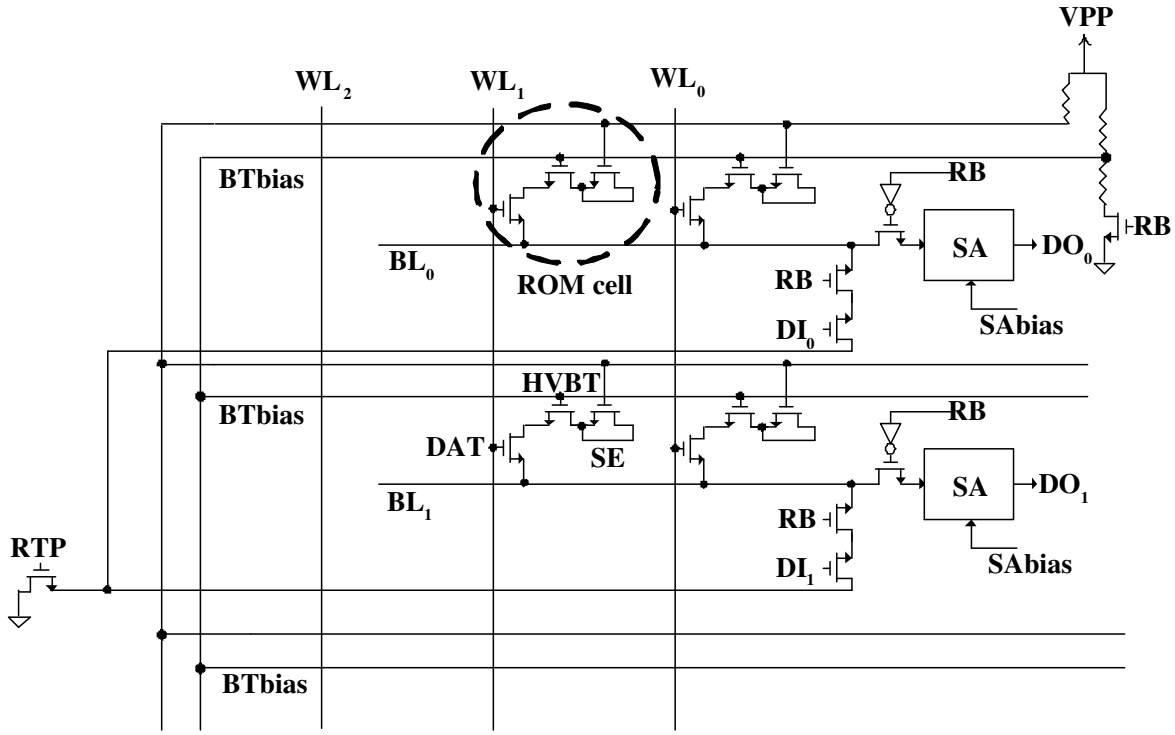

Fig. 6. The OTP ROM array.

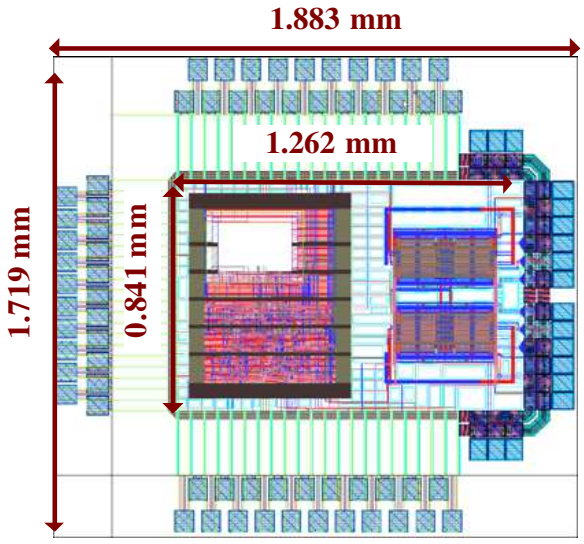

Fig. 7. Layout of the proposed design.

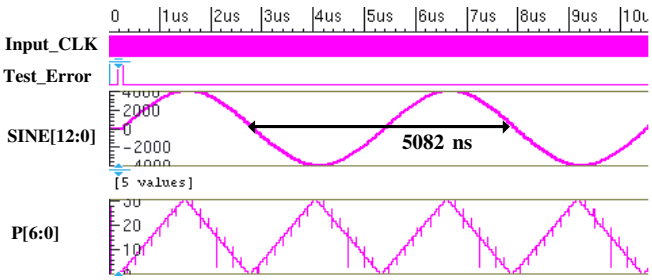

Fig. 8. The simulation of a synthesized sinusoid.

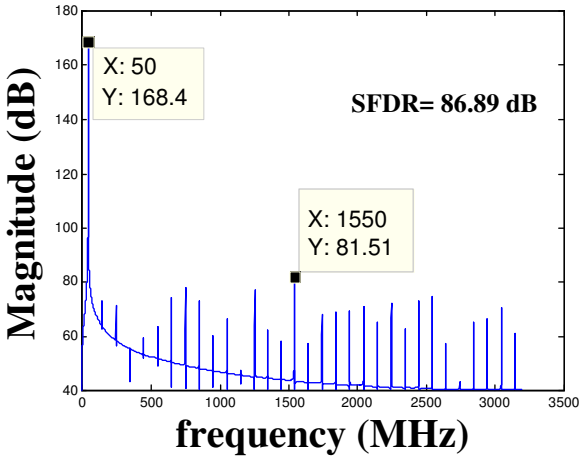

Fig. 9. The SFDR of the synthesized sinusoid.