Mixed-Voltage-Tolerant I/O Buffer Design[§]

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***Abstract*— A fully mixed-voltage-tolerant I/O buffer implemented using typical CMOS 2P4M 0.35 μm process is proposed in this paper. Unlike traditional mixed-voltage-tolerant I/O buffers, the fully mixed-voltage-tolerant I/O buffer can transmit and receive the signals with voltage levels of 5/3.3/1.8 V. By using stacked PMOS and stacked NMOS at the output stage and a level converter providing appropriate control voltages for the gates of the stacked PMOS, the gate-oxide overstress and hot-carrier degradation are avoided. Moreover, gate-tracking and floating N-well circuits are used to remove the undesirable leakage current paths. The HSPICE simulation results reveal that the gate-oxide reliability is confirmed. The maximum transmitting speed of the proposed I/O buffer is 103/120/84 Mbps for the supply voltage of I/O buffer at 5/3.3/1.8 V, respectively, given the load of 20 pF.**

Keywords—**fully mixed-voltage-tolerant, I/O buffer, gate-tracking, floating N-well, level converter, level converter**

I. Introduction

With the evolution of CMOS technology, the supply voltage of the integrated circuit (IC) is scaled down to reduce power consumption. For example, 5 V, 3.3 V, and 1.8 V voltage supplies are needed for 0.5 μm, 0.35 μm, and 0.18 μm processes, respectively. When these chips using different processes are integrated on a PCB-based system (Fig 1 (a)), conventional I/O buffers are no longer suitable to be the I/O interface because of the appearance of gate-oxide reliability, hot-carrier degradation, and the undesirable leakage current paths [1].

Mixed-voltage-tolerant I/O buffers using stacked-NMOS output stage, gate-tracking and floating N-well circuits were introduced to overcome these problems [2]- [4]. By using the stacked-NMOS schematic, the gate-oxide overstress and the hot-carrier degradation on the output stage can be avoided when a high supply voltage (VDDH) is provided at the PAD. Besides, two leakage current paths, the undesired turned-on PMOS at the output stage and the activated parasitic diode of the output PMOS, might be turned on when VDDH is present. The gate-tracking circuit can trace the voltage on the PAD (V_{PAD}) and then provide an appropriate voltage level for the gate of PMOS at the output stage. Thus, the leakage current path (from the PAD to VDD) through the PMOS at the output stage is eliminated. Similarly, the floating N-well circuit can provide an appropriate voltage level for the N-well of the output PMOS. With the floating N-well technique, the leakage current through the parasitic diode of the output PMOS would be removed because the parasitic diode would not be turned on. Even the signals with 3 $\times$ VDD can be received by using NMOS-blocking technique [5]. By using these circuits, the I/O buffers can receive the signals with higher voltage level without any hazards such that they can receive the signal from those chips using traditional processes (with high voltage levels) and advanced process (with low voltage levels) as shown in Fig. 1 (b). Because the mixed-voltage-tolerant I/O buffers can not transmit the signals with higher or lower voltage levels, the applications are drastically limited. Thus, this paper proposes a fully mixed-voltage-tolerant I/O buffer, which can receive and transmit the signals with either higher or lower voltage levels, as shown in Fig. 1 (c).

The proposed fully mixed-voltage-tolerant I/O buffer is implemented using typical 0.35 μm CMOS process and has the capability to transmit and receive the signals with voltage levels of 5/3.3/1.8 V. In order to avoid the gate-oxide overstress, the proposed I/O buffer employs the stacked PMOS at the output stage, as shown in Fig. 2. Moreover, Vg1 must be equal to 5 V and Vg2 must be larger than 1.65 V in the receiving mode when VDDIO = 5 V and V_{PAD} = 0 V. Similarly, Vg1 and Vg2 must be larger than 1.65 V in the transmitting mode when VDDIO = 5 V and logic 1 is transmitted. By controlling the gate voltages, the gate-oxide overstress can be avoided completely. To output the signals with different voltage levels, the voltage VDDIO must be supplied to the output stage. Notably, VDDIO could be easily obtained from the existing voltage source in the system by engineers. Therefore, no excess cost will be increased. The only penalty is the additional power PADs for VDDIO.

II. Fully Mixed-voltage-tolerant I/O Buffer

Fig. 3 shows the block diagram of the proposed fully mixed-voltage-tolerant I/O buffer. The I/O buffer is composed of a Pre-driver, a Voltage level converter, an Output stage, an Input stage, a Gate-tracking circuit, a Floating N-well circuit, and a bonding PAD. The major difference from the traditional mixed-voltage-tolerant I/O buffer is that it possesses the VDDIO (different from voltage level for the core, VDD). By using VDDIO, transmitting signals with different voltage levels can be achieved. However, it also brings several potential hazards

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of gate-oxide overstress. Therefore, the Voltage level converter is proposed to resolve the problems.

Fig. 4 shows the schematic of the proposed I/O buffer. With various applications, the supply voltage the for I/O buffer (VDDIO) might be 5/3.3/1.8 V depending on usages, while the supply voltage for the core (VDD) is always 3.3 V.

Pre-driver: EN is the control signal to determine whether the transmitting (EN = 0 V) or receiving (EN = 3.3 V) mode is selected. The signal I is sent by the cores and expected to be transmitted to the external driven devices. In the transmitting mode, if I = 3.3 V, No2 would be turned off while Po1 and Po2 are switched on such that V_{PAD} = VDDIO = 5/3.3/1.8 V. Contrarily, V_{PAD} = 0 V when I = 0 V. In the receiving mode, the signal I is ignored.

Input stage: Ni1 is to isolate any unexpected high voltage at the PAD. When V_{PAD} = 5/3.3 V, Vi1 would be close to VDD minus a threshold voltage (noted by ∼3.3 V). Because the high voltage of 5 V is isolated, the gate-oxide reliability is ensured. With the feedback loop by Pi1, Vi1 would be pulled up to the full swing to reduce the static power consumption. Also, Pi1 pulls Vi1 up to 3.3 V when V_{PAD} = 1.8 V is given. Therefore, if V_{PAD} = 5/3.3/1.8/0 V, Dout = 3.3/3.3/3.3/0 V.

Output stage: In order to keep the gate-oxide reliability, stacked PMOS and stacked NMOS are employed. Moreover, Vg1 = 5 V and Vg2 $>$ 1.65 V must be provided when VDDIO = 5 V and V_{PAD} = 0 V in the receiving mode. In the transmitting mode, Vg1 and Vg2 must be larger than 1.65 V when VDDIO = 5 V and logic 1 (= 5 V) is transmitted to turn on the stacked PMOS and avoid the gate-oxide overstress. Vg1 and Vg2 will be generated by the Voltage level converter.

Gate-tracking circuit: Po3 is the gate tracking circuit. When V_{PAD} = 5 V, Po3 will be turned on such that Vg2 is charged to 5 V. With the source and gate voltages at the same voltage level of 5 V, Po2 will not be turned on and no leakage current will be introduced. When V_{PAD} is biased at 3.3, 1.8, or 0 V, Po3 will be off and Vg2 is determined by the Voltage level converter.

Floating N-well circuit: Po10, Po11, Po12, No14, and No15 consist of the Floating N-well circuit. The Floating N-well circuit is to provide the N-well voltages for Po2 and Po3 to avoid the leakage current path from the parasitic diodes. When V_{PAD} = 5 V and VDDIO = 5/3.3/1.8 V, VC2 will be coupled to 5 V through Po10, while Po11 is off by Vg11 = 5 V. When V_{PAD} = 0 V and VDDIO = 5/3.3/1.8 V, Po10 and Po12 are off and No15 is on such that Vg11 is pulled to 0 V. Thus, VC2 will be charged to ∼VDDIO (= ∼5/∼3.3/1.8 V). Similarly, when V_{PAD} = 1.8 V and VDDIO = 5/3.3 V, VC2 will be charged to ∼VDDIO (= ∼5/∼3.3 V) from Po11. Notably, when VDDIO is at 1.8 V, VC2 will be coupled to 1.8 V such that all transistors are off. With VC2 = 1.8 V, the body effect of Po2 is avoided in this case. It is helpful for transmitting a signal with VDDIO at 1.8 V using 0.35 μm devices. Therefore, the output driving capability of the stacked PMOS will be strengthen by pulling down the N-well voltage to 1.8 V of Po2 when VDDIO is biased at 1.8 V.

Voltage level converter: In the transmitting mode, EN is coupled to 0 V. Thus, VC1 is determined by the output of the inverter inv4. When VDDIO = 5 V, the input of inv4 is pulled up to ∼3.3 V through Po13 and No13 such that VC1 is at 0 V. Because EN and VC1 are both biased to 0 V, Po5 is turned on and No5 is off. Thus, Vo2 will be biased to 1.67 V with Po4, No4, and Po5. Vo7 is pulled to 0 V such that No8 and No9 are turned off. If I = 0 V is driven, Vo5 will be at 0 V as well such that No12 is off and No13 is on. Therefore, Vo4 is discharged to the voltage of 2.47 (= 1.67 + 0.8) V by Po9 and Vg1 is pulled to VDDIO (= 5 V). With Vg1 at 5 V, Vg2 (= Vo2) at 1.67 V, and Vg4 at 3.3 V, V_{PAD} will be pulled to 0 V. That is, the signal of logic 0 is transmitted. Besides, the gate-oxide reliability for the Output stage will be ensured. If I = 3.3 V, Vg1 will be at 2.47 V and Vg4 will be at 0 V. Thus, V_{PAD} is pulled up to 5 V and logic 1 is transmitted. When VDDIO = 3.3/1.8 V, Po13 will be turned off such that VC1 is 3.3 V. Then, Vo2 and Vg2 is discharged to 0 V through No5 such that Vo7 is pulled to 3.3 V. Thus, Vg1 will be pulled down to 0 V through No6 and No8 for I = 3.3 V. When Vg1 and Vg2 are pulled to 0 V, the stacked PMOS can be turned on even the low VDDIO (= 1.8 V) is given. On the contrary, Vg1 will be charged to VDDIO (= 3.3/1.8 V) for I = 0 V. Thus, logic 0 could be sent.

In the receiving mode, EN is biased at 3.3 V. Vo5 will be pulled to 0 V because the output of inv1 is at 0 V. Thus, Vg1 is coupled to VDDIO (= 5/3.3/1.8 V) such that Po1 is turned off. Besides, Vg4 is pulled to 0 V by EN at 3.3 V such that No2 is turned off as well. Moreover, Vg2 will be charged to 5 V through the Gate-tracking circuit (Po3) when V_{PAD} = 5 V to avoid the leakage. No3 is to isolate the high voltage (5 V) at Vg2 such that the hazards of gate-oxide overstress at the internal devices is avoided. When V_{PAD} = 3.3/1.8 V, Po3 is off and Vg2 (= Vo2) is then at the voltage larger than 1.65 V because VC1 is pulled to 0 V. With Vg2 $>$ 1.65 V, the gate-oxide overstress on Po2 is avoided.

III. Implementation and Simulation

The proposed fully mixed-voltage-tolerant I/O buffer is carried out by using TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 2P4M CMOS process. In order to reduce the process and manufacture cost, only poly 1 is used and no silicide blocking is employed. Fig. 5 shows the layout of the proposed design. Two fully mixed-voltage-tolerant I/O buffers are included for testing consideration. Referring to Fig. 5, IO2 is for testing. The signals Vg1, Vg2 and VC2 of IO2 are outputs for observation. Moreover, guard ring is drawn for avoiding the possibility of latch up. The area of a fully mixed-voltage-tolerant I/O buffer is 385 $\times$ 87.4 μm. Moreover, the ESD strength of the stacked NMOS with their width of 60 μm can up to 1 KV for HBM (human body model) [6]. In our design, the width of the stacked NMOS is 240 μm. Thus, the ESD strength is predicted to be larger than 3 KV for HBM which is better than lots of commercial requirements (2 KV with HBM).

The proposed I/O buffer is simulated using HSPICE. Fig. 6 shows the simulated waveform of Vg1 in different corners, [TT, 25^{o}C], [FF, -20^{o}C], [SS, 125^{o}C]. Referring to Fig. 6 (a), Vg1 switches between 2.47 V (for logic 1 is transmitted) and 5 V (for logic 0 is transmitted) when VDDIO = 5 V. When VDDIO = 3.3/1.8 V, Vg1 switches between 0 V (for logic 1 to be transmitted) and 3.3/1.8 V (for logic 0 to be transmitted), as shown in Fig. 6 (b) and (c). Similarly, Vg2 is 1.65 V for VDDIO = 5 V and 0 V for VDDIO = 3.3/1.8 V in transmitting mode, as shown in Fig. 7. Fig. 8 shows the simulated output signals on the V_{PAD} at the worst corner of [SS, 125^{o}C]. The maximum transmitting data rate is 103/120/84 Mbps with the loads of 20 pF for VDDIO biased at 5/3.3/1.8 V. The simulated Vg2 in the receiving mode is shown in Fig. 9. Vg2 would be pulled to 5 V by the Gate-tracking circuit when V_{PAD} = 5 V is given. Thus, Po2 is kept off and no leakage current occurs. Fig. 10 shows the simulated VC2 for the case of VDDIO = 1.8 V. VC2 is charged to 5 V when V_{PAD} = 5 V and it is 1.8 V when V_{PAD} = 0 V.

IV. Conclusion

This paper proposes a fully mixed-voltage-tolerant I/O buffer. By using an extra supply voltage, the proposed I/O buffer can transmit and receive the signals with voltage levels of 5/3.3/1.8 V. Because the process mask of silicide blocking is not used, stacked PMOS and stacked NMOS are consisted at the Output stage to avoid the gate-oxide overstress and hot-carrier degradation. Further, the level converter is proposed to provide appropriate control voltages for the gate of the stacked PMOS for the gate-oxide reliability. Moreover, by controlling the gate voltages, the driving strength of the stacked PMOS would be enhanced with VDDIO at 1.8 V. Besides, the Gate-tracking and Floating N-well circuits are used to remove the undesirable leakage current paths. The maximum transmitting speed of the proposed I/O buffer is 103/120/84 Mbps for VDDIO at 5/3.3/1.8 V with the load of 20 pF. The area of the proposed fully mixed-voltage-tolerant I/O buffer is 385 $\times$ 87.4 μm.

V. Acknowledgment

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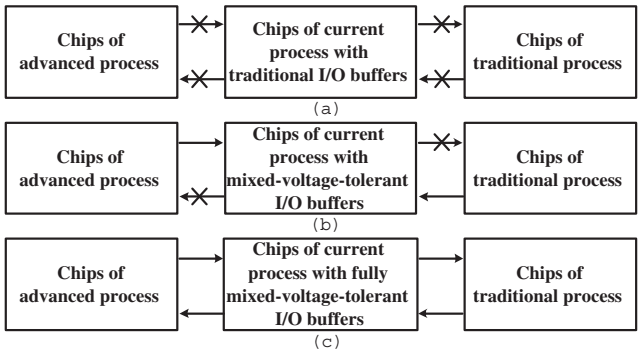

Fig. 1. Applications for different I/O buffers.

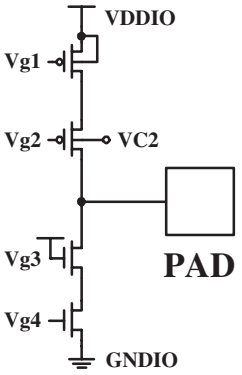

Fig. 2. Output stage of the fully mixed-voltage-tolerant I/O buffer.

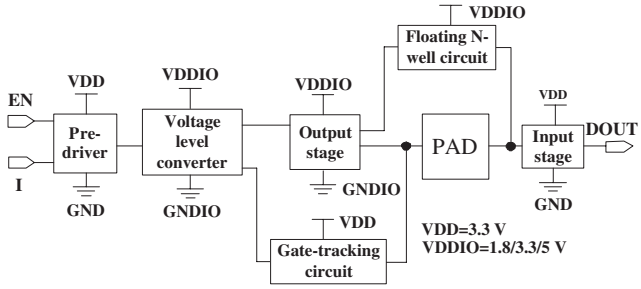

Fig. 3. Block diagram of the proposed fully mixed-voltage-tolerant I/O buffer.

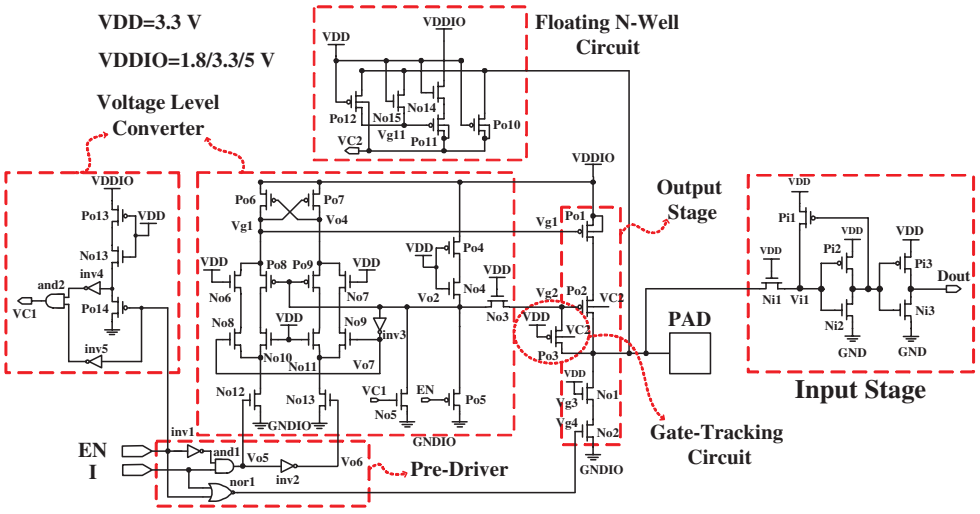

Fig. 4. Schematic of the proposed fully mixed-voltage-tolerant I/O buffer.

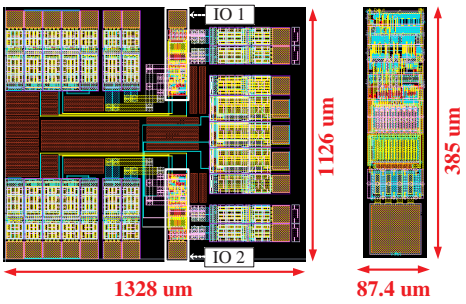

Fig. 5. Layout of the proposed fully mixed-voltage-tolerant I/O buffer.

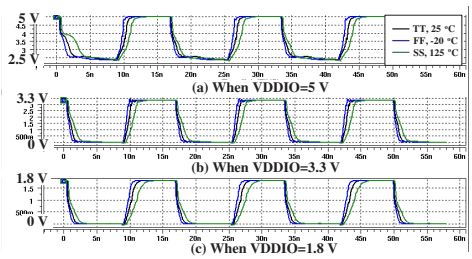

Fig. 6. The simulated waveform of Vg1 in different corners, [TT, 25^{o}C], [FF, -20^{o}C], [SS, 125^{o}C].

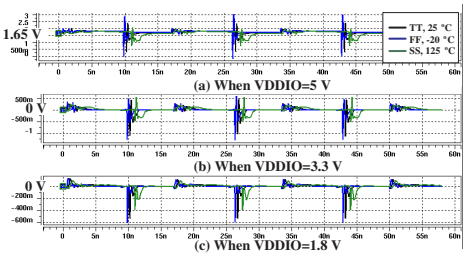

Fig. 7. The simulated waveform of Vg2 in the transmitting mode for different corners, [TT, 25^{o}C], [FF, -20^{o}C], [SS, 125^{o}C].

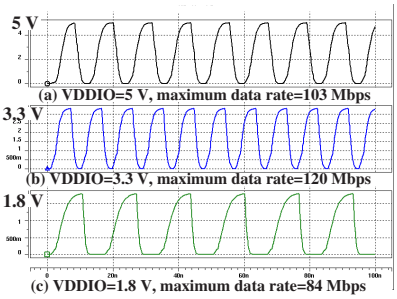

Fig. 8. The simulated output waveforms with the load of 10 pF at the corner of [SS, 125^{o}C].

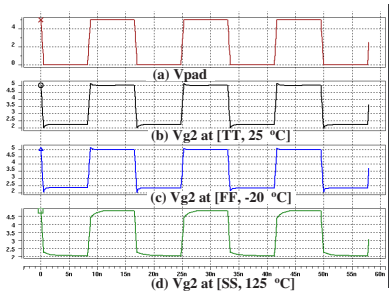

Fig. 9. The simulated waveform of Vg2 in the receiving mode for different corners, [TT, 25^{o}C], [FF, -20^{o}C], [SS, 125^{o}C].

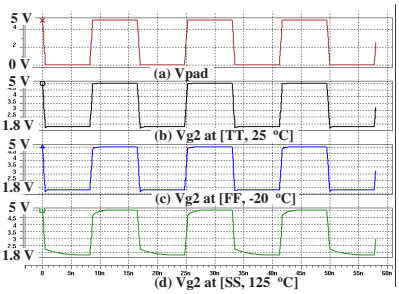

Fig. 10. Simulated VC2 for the case of VDDIO = 1.8 V.