A Low-power 4-T SAM Design for OFDM Demodulators in DVB Receiversers[§]

Chua-Chin Wang[†], *Senior Member, IEEE*, Gang-Neng Sung, *Student Member, IEEE*,
Ming-Kai Chang, Ching-Li Lee, Cheng-Mu Wu, and Ju-Ya Chen[¶]

Department of Electrical Engineering
National Sun Yat-Sen University
Kaohsiung, Taiwan 80424
email:ccwang@ee.nsysu.edu.tw

***Abstract*— This paper describes the design and implementation of a sequential access memory (SAM) in the OFDM demodulator of DVB-T receivers. The SAM decoder is based upon a ring counter to reduce the transistor count as well as the number of transitions per memory access. The SAM cell takes advantage of a negative word-line scheme to minimize the leakage current of the cell access transistors. The power consumption of memory access is then reduced. A 2-Kb SAM is carried out by 0.18 μm 1P6M CMOS process to verify the proposed design. The average power dissipation of the address decoder is 41.97 μW, while the average power dissipation of the overall SAM is 4.11 mW given a 20 MHz clock rate.**

***Keywords*—DVB-T, SAM, 4-T cell, negative word-line, ring**

I. Introduction

The trend toward portable and small digital equipments or systems is rapidly booming lately. Low power have replaced high speed becomes the key of VLSI designs aiming at portable devices. It is particularly crucial for embedded SRAMs and caches massively used in the portable devices. Notably, a large portion of the power is consumed in memory accesses [1]. In many DSP applications, SRAMs temporarily storing certain intermediately calculated numbers and data do not require random access. On the contrary, the memory accesses are strictly sequential read/write operations. For instance, programmable FIR filters read/write coefficients and data in first-in first-out (FIFO) memories [2]. Moreover, sequential access operations are also often used in memory built-in self test (BIST) or march test [3].

The DVB (Digital Video Broadcasting) compliant DTV (Digital TV) and STB (set-top box) have been gradually adopted in Europe as well as Asia mainly owing to that OFDM (orthogonal frequency division multiplexing) technique has been proven to overcome the multi-path effects in mobile receivers. The OFDM demodulator is the very critical part, since it directly affects the accuracy of the channel estimation as well as the symbol de-mapper. In a prior OFDM demodulator, six 2048×10 SRAM with 18 MHz clock rate were required to separately store Q and I symbols [4]. The numerical data of these symbols are sequentially read, calculated by FFT processors, and written back to the SRAMs. Therefore, large power consumption will arise during these R/W accesses to trigger the required address decoders and the corresponding binary counters in charge of generating sequential addresses. This paper describes a low-power SAM design which uses a multi-dimensional address decoder based upon a ring counter to reduce accessing power consumption and employs the negative word-line scheme to minimize the leakage current of the cell access transistors. A 2048×1 SAM is carried out by 0.18 μm 1P6M CMOS process to verify this design. The average power dissipation of the whole SAM is found to be 4.11 mW at 20 MHz clock rate, and a 1.8 V power supply.

[§] This research was partially supported by National Science Council under grant NSC 92-2220-E-110-001 and 92-2220-E-110-004.

[†] the contact author

[¶] J. -Y. Chen is with Institute of Communication Engineering, National Sun Yat-Sen University, Kaohsiung, 80424, Taiwan.

II. SAM Design

A. SAM address decoder

1) Conventional address decoder:

A typical 2-Kb SAM composed of four 512-b SAM banks is shown in Fig. 1. The address decoder needs a binary counter to generate sequential addresses. An AND gate is required for decoding each row, column and bank. As the number of output states increases, the complexity of the decoder with the binary counter also increases exponentially. Moreover, the decoder will result in more power consumption in some transition states, e.g., output switching from 01111 to 10000.

2) Multi-dimensional ring address decoder:

A basic ring counter circuit is shown in Fig. 2. If we assume that the circuit is initialized to the state Addr[0:n-1] = 100...0, it is easy to see that the 1 is shifted one bit right with each clock pulse. Only one flip-flop outputs 1 at any state. Hence, the ring counter can be used in SAMs as the address decoder. Fig. 3 shows the block diagram of the proposed 2-Kb SAM with a multi-dimensional ring address generator. It is also composed of four 512-b SAM banks. The address

1-4244-0387-1/06/$20.00 ©2006 IEEE

decoder is composed of ring counters. The decoder requires more flip-flops than the binary counter to produce the same number of output states. However, it does not require any binary counter and nor AND gates for decoding each row, column and bank. Hence, the overall transistor count will be reduced. The row address decoder and the column address decoder are initialized as 100...0, the bank address decoder selects the first bank (RB0 = 1). The "1" in the row address decoder is shifted right one bit at each clock pulse. The output state of the row address decoder will return to 100...0 and trigger the column address decoder shifting right every 32 clocks. Similarly, when the output state of the column address decoder is switched from 0...01 to 10...0, the bank address decoder will be triggered to select the next bank. The timing diagram of the sequential address decoder is shown in Fig. 4.

B. Low Power 4-T SAM cell

The leakage current of the memory will be increased with the capacity such that more power will be consumed even if it is in the standby mode. Many schemes, [5]-[8], have been mentioned to improve the standby power consumption for the memory. Most prior schemes reduced the effective data retention current of the inactive or non-selected cells. We choose 4-T memory cells to construct the SAM for saving power and reducing the area. A basic 4-T memory cell is shown in Fig. 5. The feature of the 4-T cells is to decrease the data retention current of inactive cells to nullify the leakage current of the cell access transistors, N1 and N2.

There were two major control schemes to reduce the leakage current of the cell access transistors : negative bulk (NB) bias, and negative word-line (NWL) voltage. Fig. 6 shows the simulation circuits of these two schemes. Fig. 7 shows the simulation results of the mentioned schemes when V_{bulk} and V_{WL} are varied from -1.5V to 0V, given a PVT condition at TT model, VDD = 1.8 V, 25^{o}C. It is found that the leakage current of the NWL scheme is smaller than that of the NB scheme, while will be maintained at the minimum current when $V_{WL} <$ -0.4 V. Besides, for the NB scheme, a triple-well structure is required to isolate the well voltage of the transistor. Hence, the area required by the design rules if the NB scheme is adopted will be increased. Thus, we employ the NWL scheme to minimize the operating leakage current so as to reduce the idle power consumption.

III. Simulation and Implementation

To reveal the power saving advantage of the proposed low power design, three decoder circuits are, respectively, implemented by the same 0.18 μm CMOS process: the binary counter + decoder using the full-customed design flow, the multi-dimensional ring address decoder using the full-customed design flow, and the multi-dimensional ring address decoder using the cell-based design flow. Notably, the cell-based design employs low power cells to make the power comparison fair. The overall characteristics as well as the comparison of these decoders are summarized in Table I. The ring address decoder using the full-customed design flow consumes the least power.

A 2048×1 bit SAM test chip composed of four 512×1 bit SRAM banks is implemented by TSMC (Taiwan Semiconductor Manufacturing Company) 0.18 μm 1P6M CMOS process to verify the power saving and the function of the proposed multi-dimensional ring address decoder. A portion of the output waveform of the proposed decoder is shown in Fig. 8. Fig. 9 shows the architecture of the entire SAM. A sequential address enable signal, SA_EN, is used to select which address is applied to memory cell. Fig. 10 shows the layout of the proposed design. Fig. 11 shows the worst-case post-layout simulation results give by TimeMill at 75^{o}C, SS model, VDD = 1.8 V with D_{out} load = 5 pF. The execution of write 0 and 1 to two adjacent memory cells and then read data from these cells is justified. Notably, the ring counters are triggered at clock negative edges, and the reset signal is active low, while data are accessed at the clock positive edges. The overall design characteristics of the SAM are tabulated in Table II. The longest access time is 5 ns and access average power is 4.11 mW in the R/W mode. The highest operating clock frequency is 100 MHz.

IV. Conclusion

We have proposed a low-power multi-dimensional ring address decoder SAMs for the OFDM demodulator of DVB receivers. The decoder is based upon the ring counter to reduce the total transistor count and the number of transitions per memory access. The leakage current of the cell access transistors is kept very low as long as word-line voltage is below -0.4 V. Hence, the power consumption of memory access can be reduced drastically.

Acknowledgment

The authors would like to express their deepest gratefulness to CIC (Chip Implementation Center) of NAPL (National Applied Research Laboratories), Taiwan, for their thoughtful chip fabrication service. The authors also like to thank "Aim for Top University Plan" project of NSYSU and Ministry of Education, Taiwan, for partially supporting the research.

References

[1] W. Shiue, and C. Chakrabarti, "Memory Design and Exploration for low power, embedded systems," *36th ACM/IEEE Design Automation Conf.,* pp. 140-145, Jun. 1999.

[2] M. Mehendaule, S. Sherlekar, and G. Venkatesh, "Low-power realization of FIR filters on programmable DSP's," *IEEE Trans. Very Large Scale Integration Systems,* vol. 6, no. 4, pp. 546-553, Dec. 1998.

[3] P. K. Lala, and A. Walker, "An on-chip test scheme for SRAMs," *Inter. Workshop on Memory Technology, Design and Testing,* pp. 16-20, Aug. 1994.

[4] C.-C Wang, J.-M Huang, and H.-C Cheng, "A 2K/8K mode small-area FFT processor for OFDM demodulation of DVB-T receivers," *IEEE Trans. on Consumer Electronics,* vol. 5, no. 1, pp.28-32, Feb. 2005.

[5] H. Kawaguchi, Y. Itaka, and T. Sakurai, "Dynamic leakage cut-off scheme for low-voltage SRAM's," *Symp. on VLSI Circuits,* pp. 140-141, June 1998.

[6] C.-C. Wang, T.-H Chen and R. Hu, " A 4-Kb 667-MHz CMOS SRAM using dynamic threshold voltage wordline transistors," in *2003 Southwest Symp. Mixed-Signal Design*, pp. 90-93, Feb. 2003.

[7] C.-C. Wang, P.-M. Lee, and K.-L. Chen, "An SRAM Design using dual threshold voltage transistors and low-power quenchers," *IEEE J. of Solid-State Circuits,* vol. 38, no. 10, pp. 1712-1720, Oct. 2003.
[8] C.-C. Wang, Y.-L. Tseng, H.-Y. Leo, and R. Hu, "A 4-Kb 500-MHz 4-T CMOS SRAM using low-Vthn bitline drivers and high-Vthp latches," *IEEE Trans. on Very Large Scale Integration Systems,* vol. 12, no. 9, pp. 901-909, Sep. 2004.

TABLE I

PERFORMANCE COMPARISON

	Counter +Decoder (full-customed)	Ring Address Decoder (cell-based)	Ring Address Decoder (full-customed)
Technology	1P6M 0.18 μm		
Power supply	1.8 V		
Avg. Power (μm) 20 MHz	83.17	100.1	41.97
Transistor Count	1070	1859	954
Max. Clock Rate (MHz)	300	250	250

TABLE II

CHARACTERISTICS OF THE PROPOSED DESIGN

VDD	1.8 V
Access Time	5 ns
Average Power	4.11 mW (20 MHz) 10.97 mW (100 MHz)
Core area	0.66×0.66 mm^2
Die area	1.018×1.018 mm^2

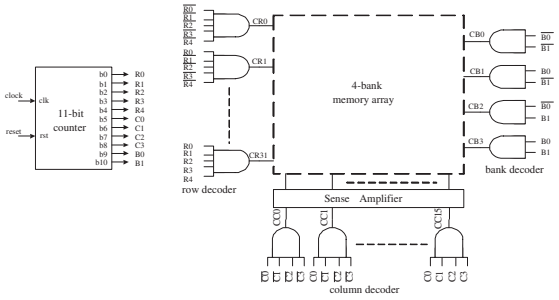


Fig. 1. Block diagram of a typical 2-Kb SAM composed of four 512-b SRAM banks.

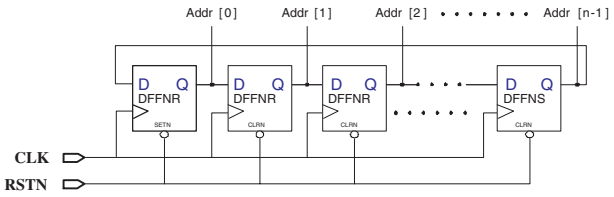


Fig. 2. Basic ring counter circuit

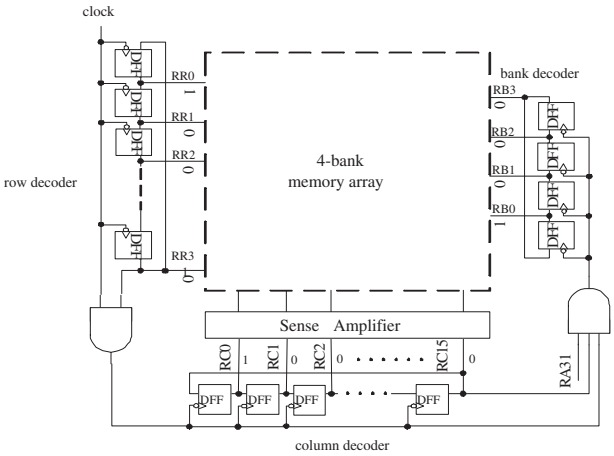


Fig. 3. Block diagram of a 2-Kb SAM with a multi-dimensional ring address generator

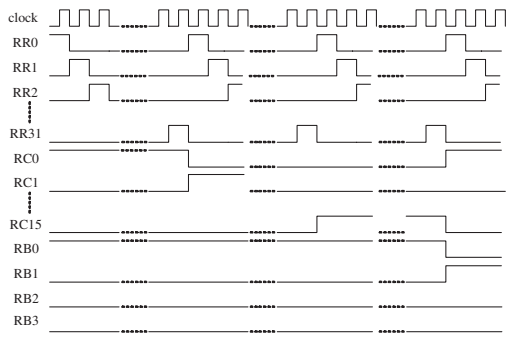


Fig. 4. Timing diagrams of the sequential address decoder

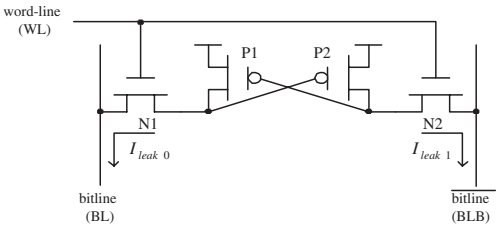
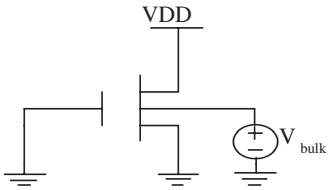
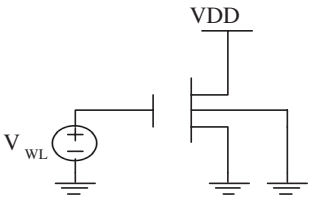


Fig. 5. Basic 4-T memory cell



(a) simulation circuit of the NB scheme



(b) simulation circuit of the NWL scheme

Fig. 6. Simulation circuits of the NB and NWL

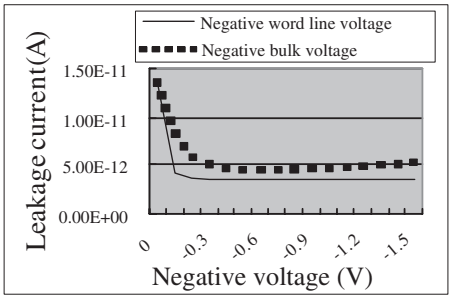


Fig. 7. Comparison of the NB with the NWL scheme for the leakage current

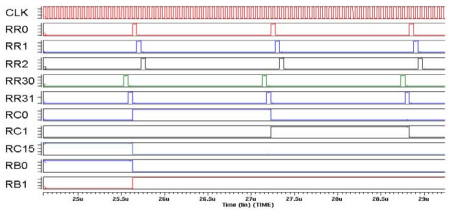


Fig. 8. Output waveform of the ring address decoder

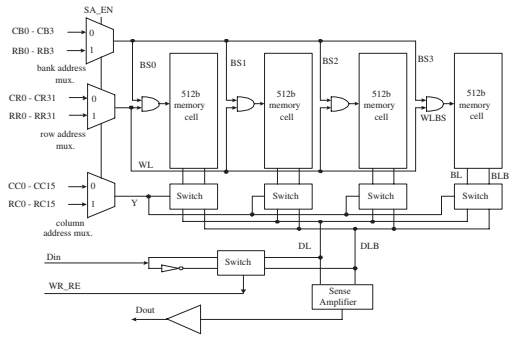


Fig. 9. Architecture of the SAM

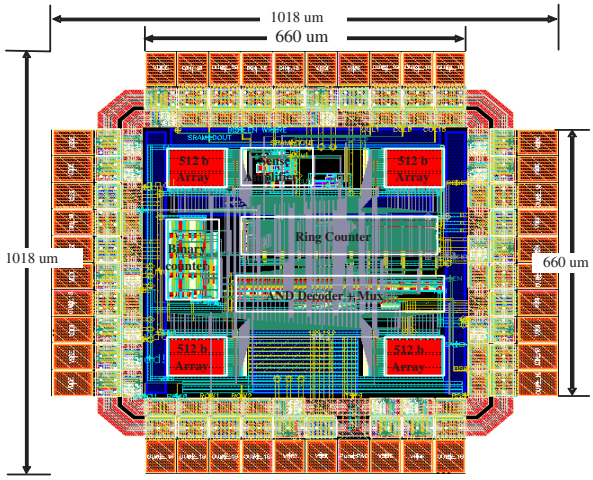


Fig. 10. Layout of the proposed SAM

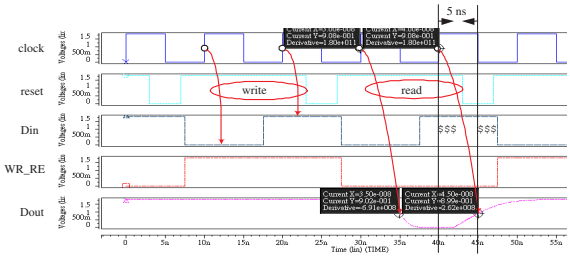


Fig. 11. Worst-case post-layout simulation