An Implantable SOC Chip for Micro-stimulating and Neural Signal Recording

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***Abstract*— An implantable SOC chip for micro-stimulation and neural signal recording is presented. This work possesses a multi-parameter control protocol to provide different stimulation waveforms, for various pain treatments of muscles and stimulating applications. Additionally, the proposed SOC chip supports several transmission rates of RS232, which in turn provides a flexibility to be integrated in a variety of different applications. Moreover, an IA (instrument amplifier) with CMRR of 120 dB and the stopband attenuation of 38 dB/dec is employed, which is capable of sensing very low voltage (1 to 10 μV) neural signal. The proposed design is implemented using TSMC 2P4M 0.35 μm CMOS process.**

***Keywords*—implanltable, wireless, neural stimulation, neural signal recording**

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I. Introduction

The implantable micro-stimulators are widely used in the treatment of the bladder leakage control [1], interrupt of pains, shaking syndromes of Parkinson's disease [2], muscle nerve stimulation [3], and cochlear implants [4]. Moreover, the stimulus frequency, current, and waveform of each application are different. We tend to design an SOC to serve such a demand.

The sensing of the neural signals and the recording thereof allow the use of the sensory signals as either feedback information or observational data to control the implanted devices, which can be a part of a neuroprosthesis. Notably, the neural signals possess a low signal amplitude in the range of 1 to 10 μV, and low frequency in the spectrum between 100 Hz to 7 KHz. Therefore, an IA, which is in charge of faithfully picking up vague neural signals hidden in the background noise floor, plays a critical role in neural signal recording. Important measurements to justify the IA include CMRR (common-mode reject ratio, $>$ 90 dB), stopband attenuation ($>$ 30 dB/dec), and high gain ($>$ 80 dB). The reason why these measurements are so important is to reject the unwanted noise and to amplify the very weak neural signal.

Furthermore, data and power transfer between the implantable unit and the outside world should be achieved without interconnect wires to avoid the infection at the points where the skin is broken. However, the transmission bit rate has a critical limit resulted from the induction of the outside and inside coils. This may cause data congestion when the neural signal is recorded.

This work presents an implantable SOC chip for wireless neural micro-stimulation and neural signal recording. The proposed chip possesses a multi-parameter communication protocol to generate different stimulus currents for various pain treatments of muscles. Moreover, the baseband circuit can support various transmission data rates of the RS232 interface. Therefore, the proposed chip is flexible for applying to various wireless induction devices and the transmission rate can be decided by the user.

II. The Structure of the Implantable SOC

We propose an implantable SOC to carry out the controllable micro-stimulation mission utilizing wireless and non-penetrating transmission to accept external instructions and execute required stimulations. In dual respect, the target SOC chip is also expected to sense the response of the nerves, convert into wireless signals and finally send back to the external monitoring devices. The infrastructure of the entire electrical micro-stimulation system is given in Fig. 1.

A. Power regulator

Since the power of the core circuits on the chip is generated by the induced RF signal, a power regulator is needed to generate a stable system voltage which possesses a ripple less than 10% variation.

B. C-less ASK demodulator

The C-less ASK demodulator is divided into four part: (1) buffered half-wave rectifier, (2) envelope detector, (3) threshold detector, and (4) load driver, as shown in Fig. 2 [5]. Notably, a two-stage OPA (operational amplifier) acts as an unit gain buffer which passes the positive voltage and resists the negative voltage. Thus, it is basically a half-wave rectifier.

C. Stimulation DAC

The 5-bit current steering DACs are employed to supply binary-weighted driving currents to their associative nerves to serve as a stimulus. The polarity signal (P) from the decoder is used to control the switches to select the current direction such that the biphase stimulus can be achieved.

D. Instrumentation amplifier, IA

The structure of the proposed 4-stage IA is shown in Fig. 4 [6]. It is composed of four cascaded stages : a preamplifier, a 2nd-order LPF (low-pass filter), a DSC (differential-to-single converter) with HPF (high-pass filter), and an output buffer with HPF. The first stage, which is the preamplifier, is mainly in charge of reducing the thermal noise effect. The 2nd-order LPF is to increase the DC gain and the stopband attenuation by adding a pole around 7 KHz using the modified low-noise gm-C LPF design in [7]. The DSC with HPF stage is to define a pole at 100 Hz and convert the differential signal into a single-ended signal such that the following ADC can further convert the sensory signal into a binary format for digital

signal processing. The last stage adds another high-pass pole at 100 Hz such that the stopband attenuation can be enhanced.

E. ADC

A charge-redistribution successive approximation ADC (SA ADC) is employed in this work, as shown in Fig. 5. A binary search through all possible quantization level is performed to obtain the final digital value. In order to avoid the drastically increased area of the binary-weighted capacitor array due to the higher resolution of SA ADC, a 6-bit binary-weighted capacitor array and a 4-bit resistor string DAC are combined to construct the 10-bit DAC. Additionally, a four-stage comparator is utilized such that the input voltage difference is amplified stage by stage. Thus, the input equivalent capacitor of the comparator can be reduced so that the matching of the binary-weighted capacitor array is ensured.

F. Packet format

The control command are issued by the external PC. The proposed chip can accept the data packet format which follows the RS232 standard with Baud Rate of 2400, 4800, 7200, 9600, 12800, 14400, 19200, 28800, 38400, 57600, 115200, and 125000 bps (bits per second). The valid packets of the command are listed in Table I. There are a total of 10 bits in each packet. The first bit, "0," is the RS232 start bit and the last bit, "1," is the end bit of RS232. The first two packets are the synchronization packets. The third packet which contains a "0011" string is the start packet. The next three packets are the data packets of the first command, which determines the action by those parameters, explained in Table II. The parameters in the first two data packets trigger the corresponding stimulations, while the third is to execute neural signal recording and impedance measurement.

The packet format provides three operation modes: neural micro-stimulation, neural signal recording, and impedance measurement. When the parameter FUN = 00, the neural stimulation is performed. Several stimulus currents are generated according to the 8 parameters for various muscles neural stimulation applications [8]. Besides, If an extra lower frequence of stimulation needs to be created, the user should choose the "Repeat" function of the GUI. Moreover, the IA and ADC are disabled to reduce the power consumption. When FUN = 01, the neural recording is activated. IA and ADC are enabled such that the neural signal is amplified by IA and digitalized by ADC. Then, the digitalized neural signals are transformed to a serial packet following the RS232 standard, as shown in Table III, for the off-chip LSK modulator. When FUN = 10, the impedance measurement is switched on. DAC generates the required current stimulus and ADC measures the voltage at the same time. Then, the measured data is sent back to PC to be analyzed. Finally, if a control data is received while FUN = 11, the operation mode remains without change.

G. Baseband circuit

The baseband circuit includes a power-on reset circuit, a 2 MHz clock generator, a clock recovery circuit and a packet decoder. Initially, VDD_OUT rises from the ground voltage. The built-in clock starts oscillating. Then, the built-in reset signal (the rising edge) resets the digital baseband circuit. When the synchronization packets are received, the clock recovery circuit counts how many cycles of the 2 MHz built-in clock during each positive edge and negative edge of the synchronization packets. The cycle numbers are recorded and then used to generate the system clock. In order to avoid the jitter accumulation of the 2 MHz clock resulting in errors of the recovered system clock, the clock recovery circuit calibrates the system clock every time that the RS232 signal flips its state. Thus, a 0.19 μs jitter tolerance is possessed for the 2 MHz clock to recover the system clock correctly.

III. Implementation and Measurement

TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 2P4M CMOS process is adopted to carry out the proposed implantable chip design. The layout of the proposed design is shown in Fig. 6, where the digital controller includes the baseband circuit and the digital encoding unit in Fig. 1. The chip core area is 1008 μm $\times$ 3166 μm (1738 μm $\times$ 2436 μm with pads). Fig. 7 is the snapshot of the GUI on the PC host. Fig. 8 shows the simulation results of continuous mode stimulation and neural signal recording. The system clock is recovered after the synchronous package received. The signal "ch3" is selected to perform the continuous mode stimulation which means that channel 3 continues the stimulus until the next command is received. Additionally, the signal "lna_en" and "adc_en" are also activated, and the channel "mux82sel0" is selected to record the neural signal. After ADC converts a sample, the parallel data "adc_out" is transformed to the serial "data_out." This process continues until the command which disables the selected recording channel is received. The characteristics of the proposed chip are tabulated in Table IV.

IV. Conclusion

We present an implantable SOC chip for micro-stimulation and neural signal recording system. A multi-parameter control protocol is proposed to provide differential stimulation waveforms for various pain treatments of muscles and stimulating applications. The protocol also can accept different transmission data rates compliant with RS232 standard such that the proposed chip can be easily integrated with PC-based system.

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TABLE I

THE COMMAND PACKET FORMAT

packet1	0	1	0	1	0	1	0	1	0	1
packet2	0	1	0	1	0	1	0	1	0	1
packet3	0	1	0	1	0	1	0	0	1	1
DATA1_1	0	AD		P	MAG					1
DATA1_2	0	CONT	DUR		INTV			WAVE	PAR	1
DATA1_3	0	FUN			CH			1	0	1
...	...									
END	0	0	0	0	0	0	0	0	0	0

TABLE II

THE PARAMETERS

field	description
AD	selecting channel(s) to be enabled
P	determines the polarity of the stimulating current
MAG	denote the magnitude of the stimulating current
CONT	the continuous mode selection
DUR	the stimulation pulse duration
INTV	select the interval time
WAVE	selects the stimulation waveform to be monophase or biphase
PAR	the parity check bit
FUN	function selection
CH	specifying which IA channel to be selected

TABLE III

THE SENSED DATA PACKET PROTOCOL

Sync1	0	1	0	1	0	1	0	1	0	1
DATA1_1	0	0	1	1	FUN		ADR	B9	B8	1
DATA1_2	0	B7	B6	B5	B4	B3	B2	B1	B0	1

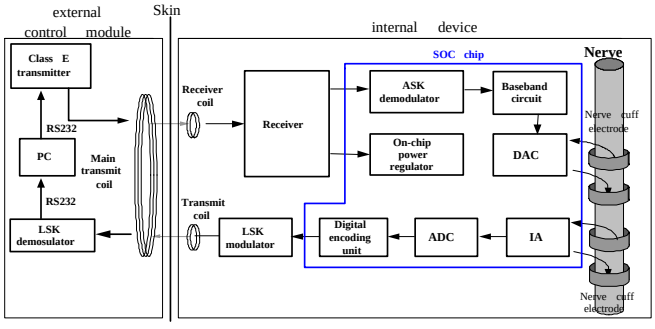

Fig. 1. The building blocks of the implantable system.

TABLE IV

COMPARISON WITH PRIOR DESIGNS

	ours	[9]	[10]
Technology	CMOS 0.35 0.35 μm	BiCMOS	BiCMOS
Area(mm^2)	1.738×3.166	2×8	4×4
IA BW.(Hz)	100∼7K	no	100∼3.1K
IA Gain	80 dB	no	100
IA Stopband attenuation	40 dB/dec	no	N/A
IA CMRR	$>$ 100 dB	no	N/A
ADC Resolution	10 bits	no	8 bits
Channel	4	8	2
Stimulus Freq.(Hz)	20∼10K	500∼8K	no
Stimulus Dur.	100∼2000	N/A	no
Power (mW)	25.52	$<$ 25	90
Function	Neural recording, Micro-stimulation, Impedance measurement	Neural stimulation	Neural signal recording

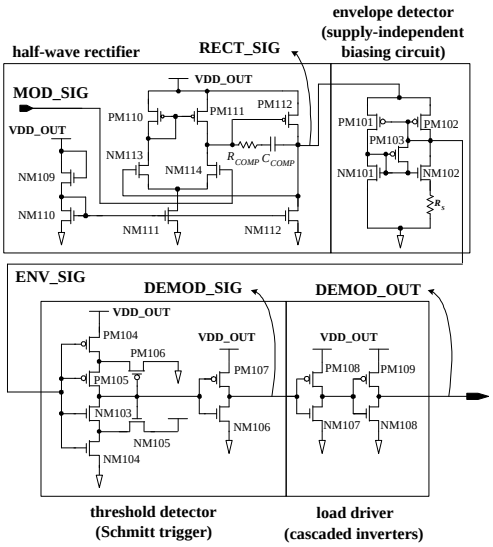

Fig. 2. Schematic of the C-less ASK demodulator.

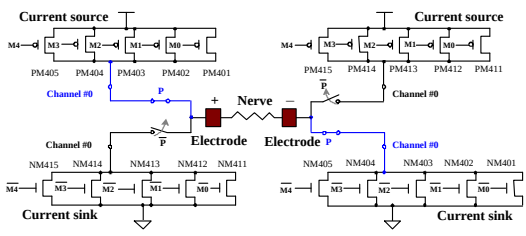

Fig. 3. Schematic of the stimulation DAC.

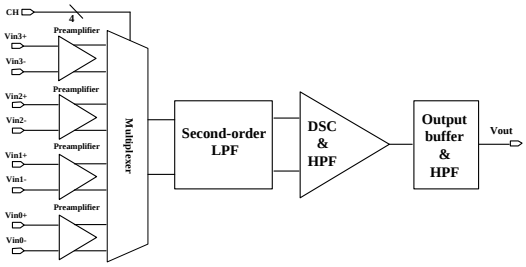

Fig. 4. Schematic of the IA.

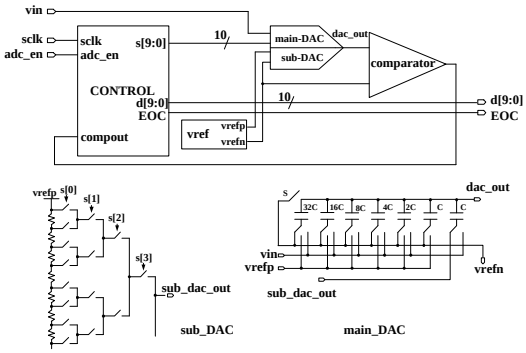

Fig. 5. Structure of the SA ADC.

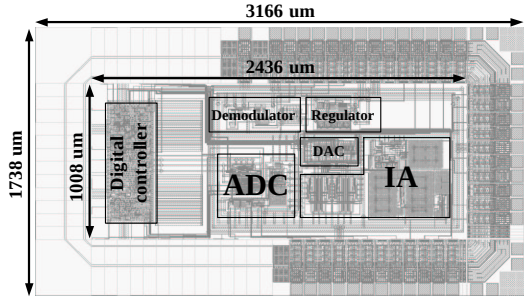

Fig. 6. Layout of the proposed SOC.

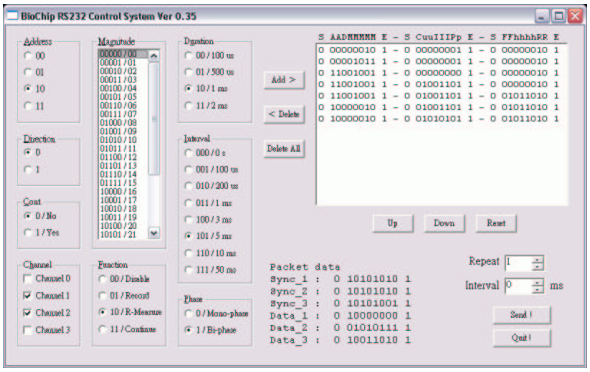

Fig. 7. The PC's GUI for generating the command of RS232 standard.

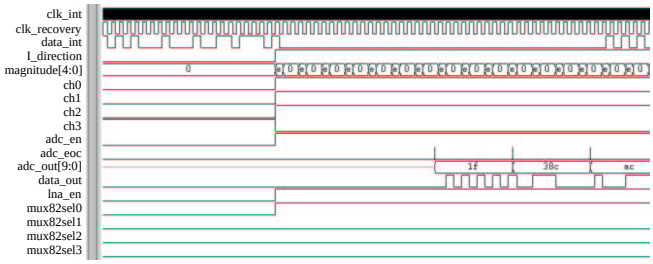

Fig. 8. The simulation results of the baseband circuit.