An All-MOS High Linearity Voltage-to-Frequency Converter Chip with 520 KHz/V Sensitivity[§]

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***Abstract*— An all-MOS linear voltage-to-frequency converter (VFC) chip with 520 KHz/V sensitivity is presented in this paper. This circuit converts an input voltage into frequency by charging and discharging a capacitor. An all-MOS voltage window comparator (VWC) with reduced propagation delay is designed to improve the linearity of traditional VFCs. The propagation delay of the VWC is discussed to resolve the tradeoff between bandwidth and linearity of VFC. The proposed VFC is verified on silicon using TSMC (Taiwan Semiconductor Manufacturing Company) 1P5M 0.25μm process. The measurement results show that the linearity error is less than 1%, and the sensitivity is 520 KHz/V at the input voltage range from 0.1 to 0.8 V.**

Keywords– **voltage-to-frequency converter, sensitivity, linearity, voltage window comparator**

I. Introduction

VFC is a quite popular device due to their low cost and application versatility in variety of electronic control and measurement systems [2]. In measurement systems, the oscillation amplitude, frequency, or duty cycle of the multivibrators provide information on the value of passive or active elements which play roles as sensors of some other factors (mechanical pressure, magnetic field, or temperature) [3]. To maintain the transform accuracy, the variation of the oscillation should be reliable functions of the corresponding change of these sensed values. Thus, the bandwidth, sensitivity, and linearity are the most important measures to judge the quality of VFC. These measures also differentiate the VFC and the VCO (voltage-controlled oscillator). Besides, VFC gives more noise immunity in these measurement systems by converting information into oscillation frequency.

A traditional current steering method to design VFC is converting voltage to current and then into frequency, [6], [3]. Pease showed this idea to design a VFC and used discrete components to verify on PCB board [6]. Filanovsky's design was implemented by using BJTs on breadboard [3]. Filanovsky's experiment results revealed that the current steering method was easily to achieve high bandwidth (100 Hz to 100 KHz), but had a poor linearity (the error is more than 2%). Thus, Trofimenkoff presented a square-rooting VFC based on a clock-controlled one-shot circuit, an integrator, and a filter to provide a 0.02% transformation linearity with full-scale frequency 4 KHz. However, square-rooting VFC attains high linearity at the cost of decreased bandwidth and excess power consumption from 1.024 MHz clock. Besides, the square root relation between the output frequency and the input voltage limits the application range, e.g., for liquid or gas orifice and venturi flow measurement devices [5]. Later, a new Σ-Δ VFC presented by Stork was capable of less than 1% linearity (16 to 18 bits linearity) [2]. Nevertheless, a low jitter clock was required and the bandwidth was reduced to 3.5 KHz in Stork's design. A different method using switched capacitor circuit could achieve maximum operation frequency to be as high as 100 KHz [4]. However, its linearity was drastically dependent on the frequencies of two on-chip clocks.

Thus, we present a VFC which keeps the high bandwidth feature of the traditional VFC but attains a better linearity by using an all-MOS VWC. This circuit is verified on silicon using TSMC 1P5M 0.25 μm process to have linearity better than 1%, 416 KHz bandwidth, and 520 KHz/V sensitivity.

II. All-MOS VFC

The basic theory of the proposed VFC is to track back-and-forth variations of a certain signal in a pre-determined range. Thus, no additional accurate oscillators or PLLs are required. In addition, the low-cost CMOS technology is very suitable to carry out this circuit.

A. Architecture of the proposed VFC

The building blocks of the proposed VFC are shown in Fig. 1. The input voltage VI is converted to current I_{conv} by a V-to-I circuit and then sent into the charge and discharge circuit (CDC). CDC generates a voltage, V_{cap}, whose slope is dependent on I_{conv}. V_{cap} is then tracked by an all-MOS voltage window comparator (all-MOS VWC) in a pre-determined range bounded by two reference voltages VH and VL, where VH is higher than VL. When V_{cap} decreases lower than VL, VWC generates the comparison result, VOUT = 1 (2.5 V), to charge a storage capacitor in the CDC and pull V_{cap} to

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high. On the contrary, if V_{cap} goes higher than VH, the VWC changes its output to be 0 V (VOUT = 0), which results in V_{cap} to be pulled down. In short, V_{cap} varies between VH and VL, and VOUT is the generated oscillation signal whose frequency is controlled by VI.

B. Schematic of the proposed VFC

Fig. 2 shows the schematic of the proposed VFC. OPA, NM21, PM21, and R_T constitute the voltage to current converter (V-to-I converter). According to the virtual ground principle, the minus input node of OPA equals to VI. Hence, the generated current I_{conv} is expressed as

$$I_{conv} = \frac{\text{VI}}{R_T} \tag{1}$$

Notably, the length of all of the MOS transistors are set to be at least 5 times of the feature size to avoid any short-channel effect.

The width of PM21 is M times of that of PM23 such that the mirrored current, I_{cap}, is 1/M times of I_{conv}.

The switch, sw1, which decides the storage capacitor C_T to be charged or discharged, is controlled by the output signal (VOUT) of VWC. The voltage drop of the capacitor, V_{cap}, and two reference voltages, VH and VL are fed into VWC to be compared. While V_{cap} is large than VH, the output signal VOUT = 0 V is provided by VWC to connect sw1 to node b1 such that C_T is discharged. On the contrary, if V_{cap} is less than VL, VWC generates VOUT = 2.5 V to switch sw1 to connect to node a1 resulting in C_T to be charged.

According to the previous description, it is concluded that the ideal relation between the input voltage VI to the output frequency f_{out} could be expressed as follows,

$$f_{out} = \frac{\text{VI}}{2 \cdot C_T \cdot R_T \cdot (\text{VH} - \text{VL}) \cdot M} \tag{2}$$

Obviously, Eqn. (2) is a linear function for f_{out} vs. VI if M, VH, VL, C_T, and R_T are predetermined.

C. Linearity of the proposed VFC

Several non-ideal effects might be considered carefully to ensure the linearity of the proposed circuit. Firstly, in order to avoid the charge injection from the switch sw1, the dummy switches are required to be added. Secondly, although the offset voltage of VWC results in the comparison error, it doesn't affect the linearity seriously due to the error cancellation between two comparisons per cycle. Lastly, the propagation delay (T_{prop}) of VWC is the most important impact to the linearity. The analysis is as follows : the linearity error $(accuracy) = \frac{f_{real} - f_{ideal}}{f_{max}}$, where f_{max} is the maximum operating frequency of VFC, $f_{ideal} = 1/T_{ideal}$ is the ideal output frequency, and $f_{real} = 1/(T_{ideal} + T_{prop})$. In contrast with the varying T_{ideal} resulted form the varying VI, T_{prop} is deemed as a constant value. Therefore, it creates a non-linear term in the transfer function, i.e., Eqn. (2).

To obtain a better behavior in linearity, we compute f_{max} with the corresponding T_{prop} given that the required accuracy error is less than 1% in Fig. 3. Obviously, a higher operation frequency of VFC requires a shorter T_{prop} of VWC. In Fig. 3, there is a turning point at f_{out} = 10 MHz. Thus, we need to design a fast all-MOS VWC without the necessity of using a high-precision clock.

D. Schematic of VWC

Fig. 4 is the schematic of the proposed all-MOS VWC. The two comparators, OPA1 and OPA2, compare the same input voltage VIN (connected to V_{cap}) by two reference voltages, VH and VL, respectively. Their output signals are coupled to the inverter via the switch, sw2. In order to meet the function of VWC for the VFC, the output signal (WOUT, connected to VOUT) of VWC is fed back to sw2 to select which of the outputs of OPA1 or OPA2 is the final comparison result. The switch, sw3, is used to give this VFC an initial state. When INIT = 2.5 V, node d1 is connected to ground due to that sw3 is closed to initialize VOUT = 2.5 V. This causes that C_T begins to be charged and OPA1 is in action simultaneously. Then, VWC is waiting for V_{cap} to be pulled high. The details of OPA1 and OPA2 are shown in Fig. 5 [1]. Referring to Fig. 5, every node, except the output node (VOUT), is a low impedance node due to the diode-connected MOSs such that the comparison of VWC is quite fast.

III. Implementation and Measurement

This circuit is implemented using TSMC 0.25 μm 1P5M CMOS process and measured by using Agilent Infiniium Oscilloscope 600 MHz 4 GSa/s. The die photo is shown in Fig. 6 and the core area is 517.39 $\times$ 595.78 μm^2. The reference voltages, VH and VL, are chosen to be 2 V and 1 V, respectively. Fig. 7 shows that V_{cap} varies correctly back and forth between VH and VL, which is measured to be 1.93 and 0.994 V. Notably, the inaccuracy of these two reference voltages affect the gain of VFC, not the linearity. Referring to Fig. 8, the maximum operating frequency in the linear range is measured to be 416 KHz given VI= 0.8 V. Fig. 9 shows the output frequency versus input voltage is a linear relation, where the linearity error (accuracy) is less than 1%. The measured results compared with several prior works is summarized in Table I. Obviously, the output frequency and the sensitivity of our VFC are higher than that of all of the prior researches, while the linearity meets the requirements for the most measurement systems, i.e., 1%.

IV. Conclusion

We have proposed a high bandwidth all-MOS voltage-to-frequency converter chip in this paper. Not only the sensitivity and the output frequency are enhanced, the linearity error less than 1 % is also better than that of the traditional current steering VFCs. Moreover, the overall manufacturing cost is also reduced, because CMOS process is used to carry out this circuit and no clock control circuit is needed.

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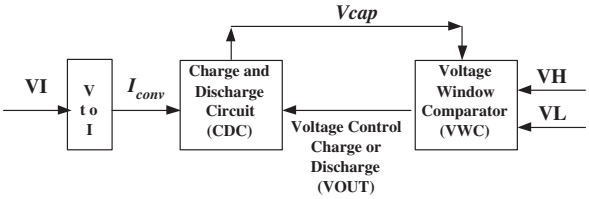

Fig. 1. The building blocks of the proposed VFC.

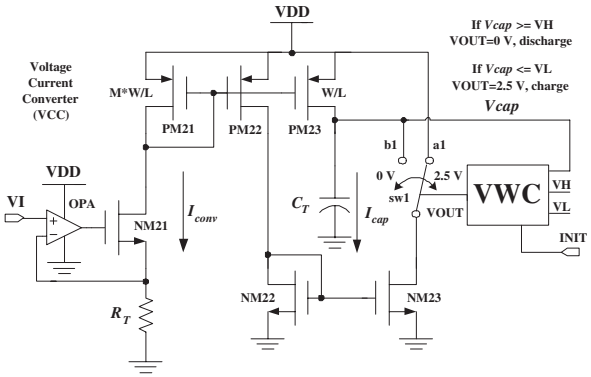

Fig. 2. Schematic of the proposed VFC.

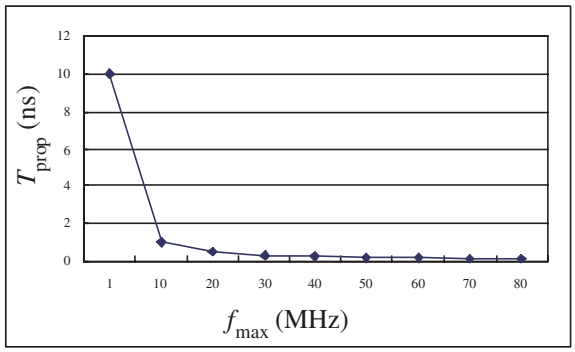

Fig. 3. The propagation delay of VWC and the corresponding max. operation frequency of VFC at condition of 1 % linearity error.

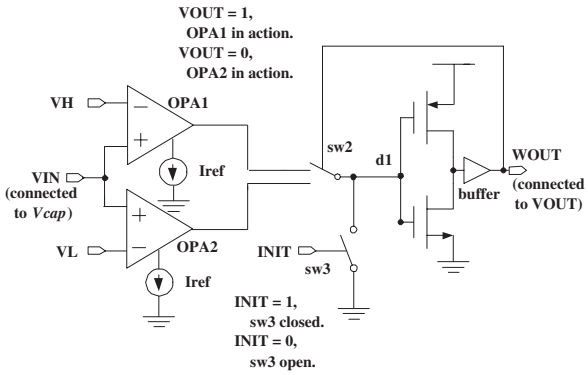

Fig. 4. Schematic of VWC.

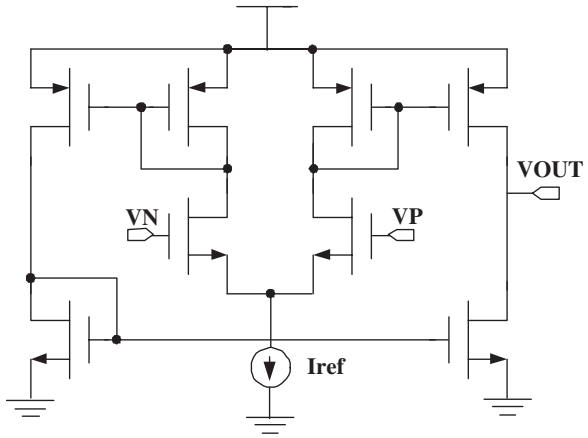

Fig. 5. Schematic of OPA1 and OPA2 in VWC.

	ours	[3]	[5]	[4]	[2]
Technology	CMOS	BiCMOS	CMOS	CMOS	N/A
Implementation	ASIC	Discrete components	Discrete components	Discrete components	Discrete components
Max. f_{out}	416 KHz	100 KHz	8 KHz	100 KHz	3.5 KHz
V_{in}	0 to 0.9 V	0 to 6 V	0.1 to 10 V	0 to 10 V	0 to 5 V
Sensitivity	520 KHz/V	16 KHz/V	0.8 KHz/V	10 KHz/V	0.7 KHz/V
linearity	$< 1\%$	$< 2\%$	0.02% while Max. freq. = 4 KHz	N/A	< 1 % (16 to 18 bits linearity)

TABLE I

COMPARISON TO PRIOR DESIGNS

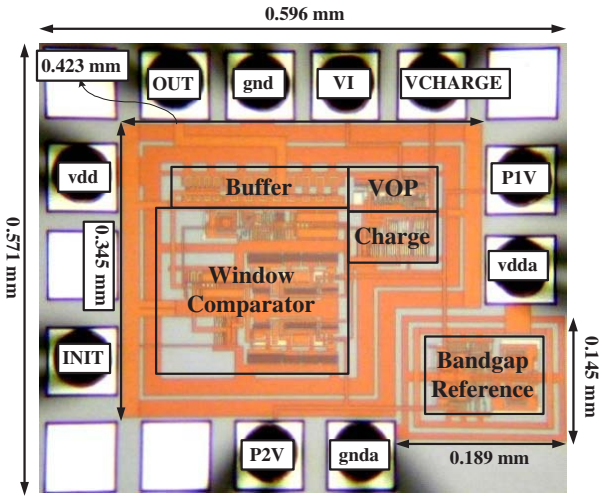

Fig. 6. Die photo of the proposed VFC chip.

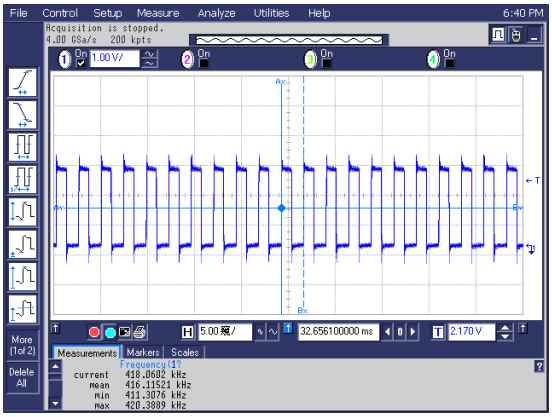

Fig. 8. The output signal while VI = 0.8 V.

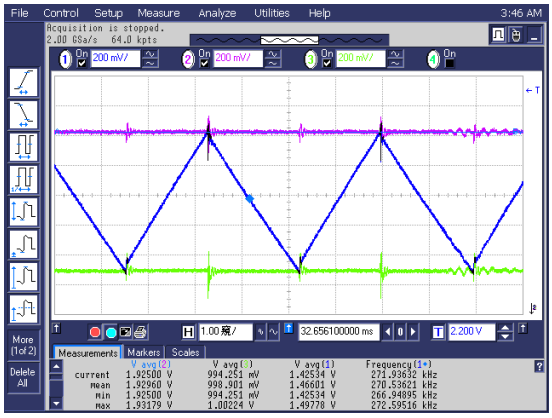

Fig. 7. Measured VH, VL, and V_{cap}.

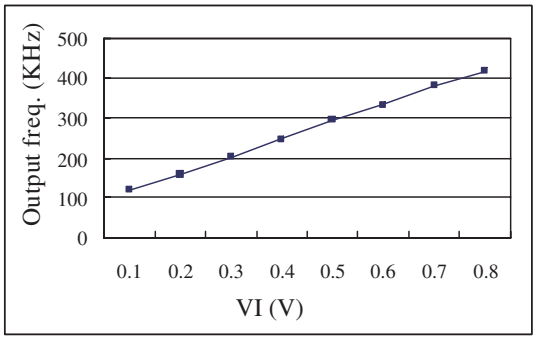

Fig. 9. Frequency of output signal v.s. input voltage VI.