A 140-dB CMRR Low-noise Instrumentation Amplifier for Neural Signal Sensing

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***Abstract*— This paper presents a novel IA (instrumentaion amplifier) design for implantable biomedical devices and systems with a 140-dB CMRR (common-mode rejection ratio). The proposed IA is composed of 3 stages, including a preamplifier, a 2nd-order BPF (band-pass filer), and a DC-level shifter and output buffer stage. A low-noise gm-C amplifier is used in the preamplifier stage so as to reduce the coupled thermal noise which might overwhelm the weak neural signals. The BPF is designed based on an OTA (operational transconductance amplifier) with dual current switches aiming at the low power as well as low noise demands. A source follower is employed to carry out the DC-level shifter and the output buffer, which provides an output signal adequate to drive the following stage, which is usually an ADC (analog to digital converter). Detailed analysis of the proposed circuitry is derived to solidify the proposed architecture. The proposed design is implemented using TSMC 0.35 μm 2P4M CMOS process. The results of post-layout simulations verify the performance of our design. The CMRR is better than 140 dB, and, most important of all, the input noise (RMS) is merely 23.28 dB at all PVT (process, supply voltage, temperature) corners.**

***Keywords*—IA, CMRR, preamplifier, Gm-C, OTA**

I. Introduction

Information provided by implantable biomedical devices is essential to any further detailed neural diagnosis as well as treatment, e.g., implanted wireless chips in [5], [8]. The sensing of the neural signals and the recording thereof allow the sensory signals to be used as either feedback information or observational data to control the implanted devices, which can be a part of a neuroprosthesis. Notably, the neural signals possess low signal amplitude in the range of 10 to 100 μV, and low frequency in the spectrum between 100 Hz to 7 KHz. Therefore, the IA (instrumentation amplifier), which is in charge of faithfully picking up vague neural signals hidden in the background noise floor, plays a critical role in the entire implantable system. Important measurements to justify the IA include CMRR (common-mode reject ratio, $>$ 90 dB), stopband attenuation ($>$ 20 dB/dec), and high gain ($>$ 80 dB). Besides, small area and low power are also considered as major design goals, too. Although several IA or LNA designs have been proposed, e.g., [1], [2], [3], [4], most of these prior works did not meet all of the requirements, particularly the CMRR and the reduction of the RMS input noise. The former implies the capability of common-mode noise rejection, while the latter indicates that of reducing thermal noise generated by the circuitry itself. The reason why CMRR is so important in IA designs is that the electrodes used in the implantable systems to either sense or stimulate the nerves will cause a significant of offset voltage (around several hundreds of mV) and an inherent impedance. The reduction of thermal noise is to ensure the fidelity of the neural noise to be sensed. In this work, a novel IA design composed of 3 stages, including a preamplifier, a BPF, and a DC-level shifter with output buffer, is proposed. Post-layout simulations unveil the impressive performance of the proposed IA design regarding the CMRR and the reduction of RMS input noise.

II. High-CMRR and Low-Noise IA Design

We have proposed an SOC (system-on-chip) design to carry out the mission utilizing wireless and non-penetrating transmission to accept external instructions and execute required stimulations [8]. The entire electrical micro-stimulus system is given in Fig. 1. In dual respect, the SOC chip is also expected to sense the response of the nerves, convert into wireless signals and finally send back to the external monitoring devices. The IA is responsible for picking up the neural signals present at the electrodes surrounding the nerve. It is obvious that the neural signals have very small amplitude while the background noise generated by the tissues, the fluid, or possibly the SOC circuitry itself is relatively large. Meanwhile, the IA must get rid of all of the unwanted noise outside of the neural signal band and amplify the sensory signal large enough to be accepted by the following ADC to convert into meaningful binary signals.

A. 3-Stage IA architecture

The structure of the proposed 3-stage IA is shown in Fig. 2. It is composed of 3 cascaded stages : a preamplifier, a BPF, and a DC-level shifter and output buffer. The respective functionality of these stages are described as follows.

1. preamplifier stage : reduce the coupled thermal noise in the circuitry

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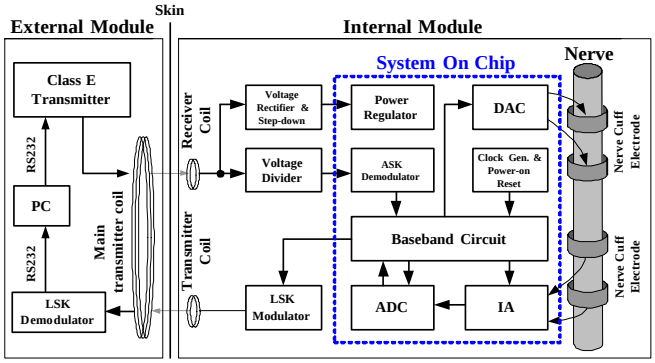

Fig. 1. The implantable micro-stimulation system.

2. BPF stage : filter out the neural signal (100 Hz to 7 KHz) with 20 dB/dec
3. DC-level shifter and the output buffer : provide an output signal with a proper DC offset and large swing to drive the following ADC

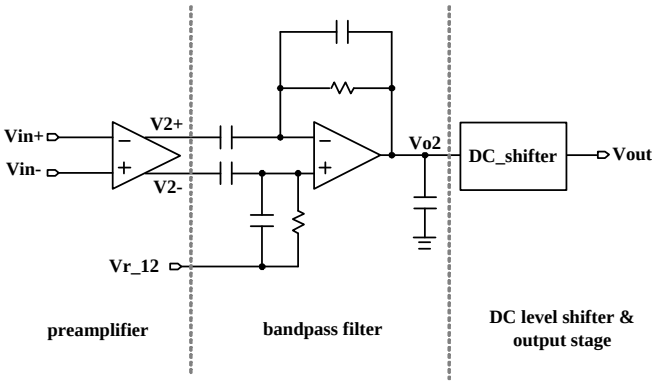

Fig. 2. The proposed IA architecture.

B. Sub-circuit designs

preamplifier : Referring to Fig. 3, a Gm-C amplifier is used to carry out the required low noise function [7]. The gain is proportional to $\frac{gm_1}{gm_2}$. Meanwhile, the thermal noise thereof is anti-proportional to gm_1. Therefore, we increase the width of the transistors for the differential inputs to boost the gain and reduce the thermal noise simultaneously. M5 and M6 are voltage-controlled resistors used to raise the gain and reduce the signal distortion effects. Notably, a transmission gate (TG) is controlled by a sleep signal, namely SW. When the sleep mode is invoked by the system to save power when the IA is no need to operate, SW turns low to shut down TG as well as all of the PMOS-based current sources on top of the amplifier.

band pass filter : The biggest problem encountered in designed a BPF for neural signals is that the required passive elements will be too large to be integrated on silicon owing to the frequency thereof is too low, i.e., 100 Hz to 7 KHz. Therefore, we tend to adopt a 2nd order design based on a

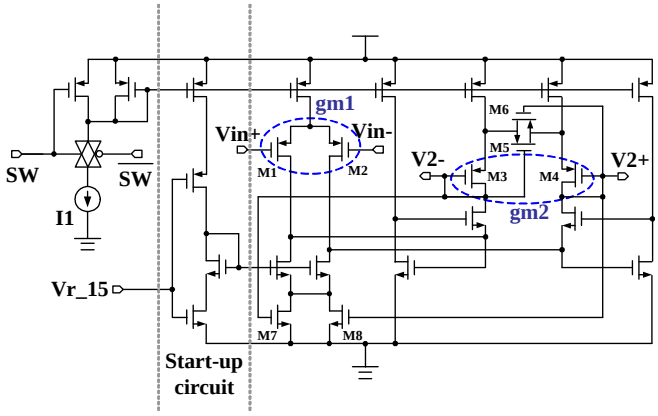

Fig. 3. Schematic of the preamplifier .

OTA, as shown in Fig. 4, to resolve this problem. The two large resistors, R1 and R2 (8 GΩ each), will be implemented by SMD resistors directly on a PCB board where the proposed chip is mounted. Two obvious advantages will be attained by such a scheme : first, the thermal noise inside the chip will be drastically reduced; second, most of the thermal noise generated by these two resistors will be filtered by the parasitic capacitor of the PADs that they are connected to.

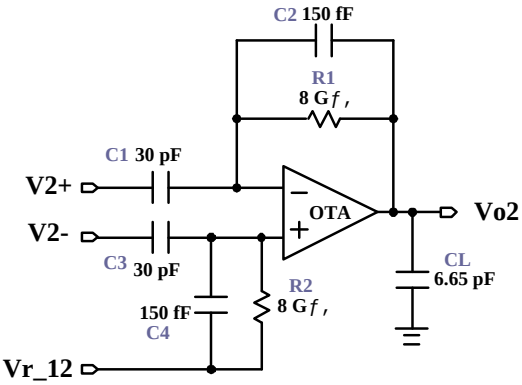

Fig. 4. Schematic of BPF

The schematic of the OTA is revealed in Fig. 5. Notably, after a few simple derivations, the noise of the OTA and the that of the overall BPF can be expressed as follows.

$$\overline{V^2_{\text{ni\_amp}}} = \left(\frac{\text{C1} + \text{C2} + \text{C}_{\text{in}}}{\text{C1}}\right)^2 \times \overline{V^2_{\text{ni}}}, \qquad (1)$$

where $V_{\text{ni\_amp}}$ is the equivalent input noise of the OTA, C_{in} is the the equivalent input capacitance of the OTA, and V_{ni} is the equivalent input noise of the BPF. Therefore, by widening the transistors of the input pair of the OTA, the input capacitance of the OTA as well as the equivalent input noise of the BPF are reduced significantly. Notably, Vr_12 shifts the output, Vo2, to a 1.2 V DC level. $\overline{\text{SW}}$ and SW, respectively, control the current source and the current sink for the mentioned sleep mode operation.

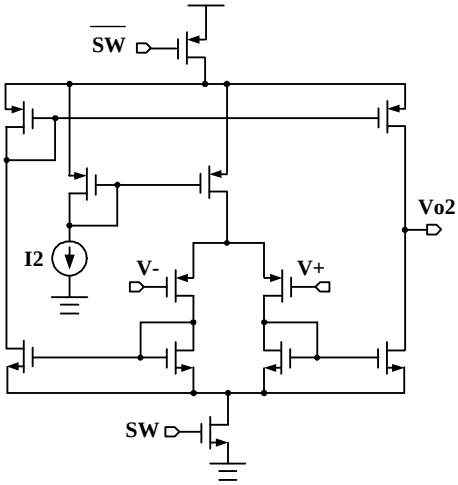

Fig. 5. Schematic of the OTA.

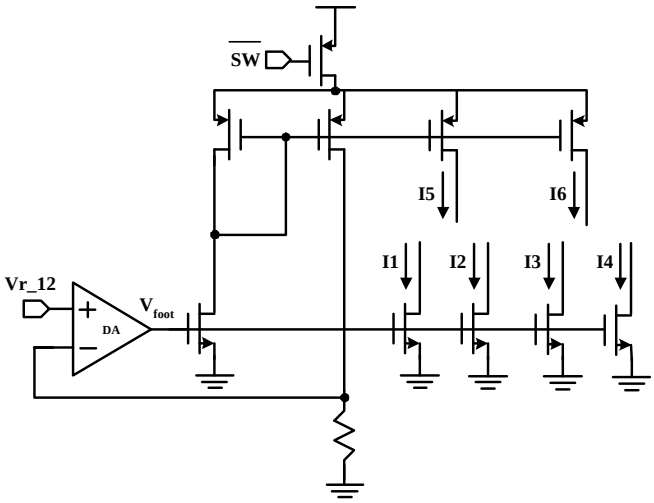

Fig. 7. Bias current generator.

DC-level shifter and the output buffer : A cascaded 2-stage source follower is employed to carry out the DC level shifting and output buffer as the same time, as shown in Fig. 6. The output of the previous BPF, Vo2, is fed to the gate drive of M61. Then, the source of M61 is coupled to the gate of the PMOS M62. By tuning the aspect ratio of M61 and M62, the DC level of Vout is lifted to 1.7 V which is required by the following ADC. The DC current source I5 provides a shielding protection for Vout from the system power supply.

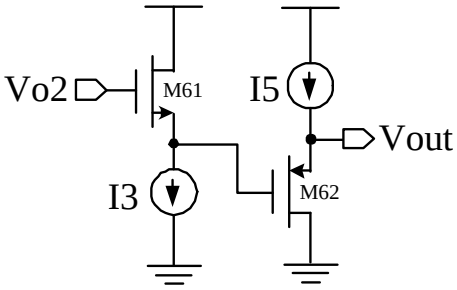

Fig. 6. DC-level shifter and output buffer.

A temperature-insensitive bandgap bias (not shown) is utilized to generate the required reference currents, Vr_12 = 1.2 V. Fig. 7 shows a bias current generator where Vr_12 is fed to the non-inverting input of DA, which is basically a differential amplifier with an NMOS input pair. The bias current generator uses current mirrors to produce all of the required bias currents for other circuits. The DA simply utilizes a feedback loop to achieve self-biasing and generate a stable output voltage reference, V_{foot}. Notably, the required start bias, Vr_15 = 1.5 V in Fig. 3, is similarly generated by a cascaded 2-stage source follower.

III. Simulation and Implementation

TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 2P4M CMOS process is adopted to carry out the proposed IA design. The layout of the proposed design is shown in Fig. 8 and the chip core area is 568 μm $\times$ 289 μm (1374 μm $\times$ 1098 μm with pads). Fig. 9 shows the filter transfer function at several PVT corners which shows that the passband gain is over 77 dB. The CMRR performance is revealed in Fig. 10 where the worst-case PVT corner is still over 140 dB. A performance comparison of the proposed design with several prior LNAs and IAs are summarized in Table I. Though the proposed design consumes more power in the normal mode, mainly due to the number of stages, it still meets the power budget of the IA. On the other hand, the proposed LNA possesses the highest CMRR and DC gain, second best of input noise and PSRR, which is considered as a better IA design alternative.

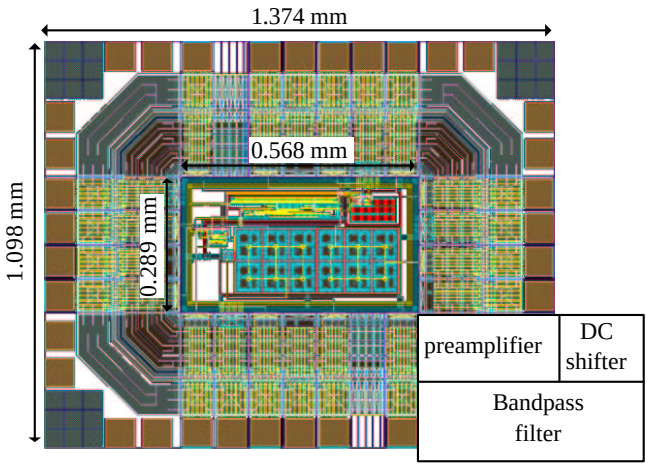

Fig. 8. Layout of the proposed design

IV. Conclusion

We have proposed an IA using a 3-stage architecture to attain high CMRR, high PSRR and low RMS input noise. It is very suitable to be used in SOC-based biomedical

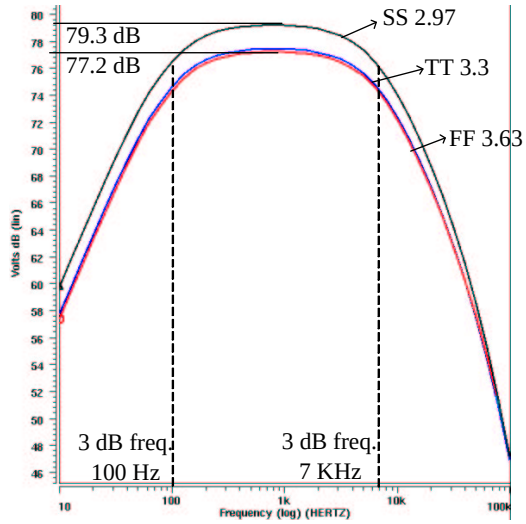

Fig. 9. Frequency response result by simulations

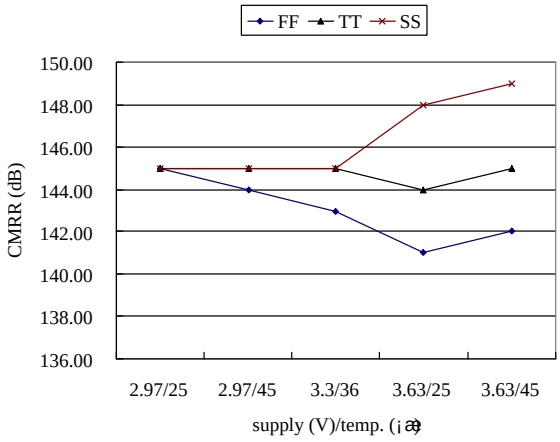

Fig. 10. CMRR performance of the proposed IA

implantable systems to sense and record the response of nerves.

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	[1]	[6]	[2]	[4]	ours
process (μm)	0.8	3	1.5	1.5	0.35
area (mm^2)	0.125	0.082	0.16	0.107	0.151
passband (Hz)	10∼10K	66∼24K	0.025∼7.2K	0.1∼10K	100∼7K
DC gain (dB)	40	38.2	39.5	39.3	77
RMS noise (μV)	9.7	16.6	2.2	7.8	6.852
CMRR (dB)	N/A	N/A	86	N/A	141
PSRR (dB)	N/A	50.5	80	N/A	78.4
power (mW)	0.122	0.092	0/08	0.1148	1.4786

TABLE I

PERFORMANCE COMPARISON OF IAS.

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