10-Bit 30-MS/s Low Power Pipeline ADC for DVB-H Receiver Systems[§]

Chua-Chin Wang,† , Senior Member, IEEE, Jian-Ming Huang, and Tie-Yan Zhang‡

Department of Electrical Engineering
National Sun Yat-Sen University
Kaohsiung, Taiwan 80424
email : ccwang@ee.nsysu.edu.tw

Abstract

This paper presents a 10-bit, 30 MS/s pipeline analog-to-digital converter (ADC) suitable for digital video broadcasting over handheld (DVB-H) systems. The ADC is based on the 1.5-bit-per-stage pipeline architecture. The proposed design is implemented by 0.18 μm CMOS technology. The input range is 2 V peak-to-peak differential, and the post-layout simulation result shows that the spurious-free dynamic range (SFDR) is 62 dBc with a full-scale sinusoidal input at 700 KHz. The maximum power consumption is 37 mW given a 3.3 V power supply. The core area is 0.27 mm^2.

1 Introduction

DVB-H is a new digital terrestrial television (DTTV) standard for handheld devices, particularly for cellular phones. DVB-H is an extension version of DVB-T (digital video broadcasting over terrestrial) standard, and it especially addresses the issues of the power consumption and mobile reception. Video-rate and high performance ADCs are required in the DVB-H receiver to quantize the output from RF tuners. Since the handheld devices, e.g., mobile phones, personal digital assistants (PDA), and portable media players (PMP), are battery operated, the power consumption is the most critical issue for the ADC design.

This paper presents a 10-bit, 30 MS/s, pipeline ADC for DVB-H receivers. According to [1], minimizing the resolution of each pipeline stage leads to the minimization of die area and power consumption. Hence, the proposed ADC adopts the 1.5-bit resolution per stage. Furthermore, we utilize several techniques, including bootstrap circuitry, bottom plate sampling, and dummy switches, to reduce the non-ideality of sample-and-hold (S/H) circuits in the ADC. Therefore, the specification of the operational amplifiers (OP-amps) in the S/H circuits can be relaxed due to the reduction of the non-ideality. Most important of all, the overall power reduction can significantly benefits from such an ADC design.

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† The contact author.

‡ Mr. Zhang is currently a MS student with Institute of Communication Engineering, National Sun Yat-Sen University.

2 Pipeline ADC architecture

The proposed 10-bit pipeline ADC is based on the standard 1.5-bit-per-stage pipeline architecture. Since minimizing the stage resolution leads to the minimization of the power consumption, the stage resolution of the proposed ADC is chosen to be 1.5 bits. The block diagram of the proposed ADC is shown in Fig. 1. The ADC is composed of one sample-and-hold amplifier (SHA), eight stages of the 1.5-bit ADC, and one 2-bit flash ADC. A 1.5-bit ADC, which means the stage resolution is 1.5 bits, which provides 0.5-bit redundancy for later digital correction.

The sub-ADC resolves two bits output by quantizing the input signal. The quantization result of the sub-ADC is converted into an analog magnitude by the sub-DAC. Thus, the residue is obtained by subtracting this magnitude from the input signal. The residue is multiplied by the gain of 2 for the next stage. The residue computation and the precise amplification of the gain of 2 are realized by a multiplying digital-to-analog converter (MDAC) [2]. Since there is no need to produce the residue in the last stage, the 2-bit flash ADC is adopted in the last stage.

2.1 SHA

Fig. 2 shows a simple SHA, where ϕ_S and ϕ_H are two complementary and nonoverlap signals. The linearity of the ADC will be seriously degenerated by the nonideality of SHA. The most important nonideality in the SHA circuit is the charge injection from MOS switches. The charge injection will introduce the nonlinear offset charge into the hold capacitor. For example, the charge injection caused by turning M1 off

can be expressed as follows:

$$Q_{M1} \propto W_1 \cdot L_1 \cdot C_{ox} \cdot (V_{g1} - V_{s1} - V_{TH}), \quad (1)$$

where W_1 and L_1 are the channel width and length of M1, respectively, C_{ox} is the gate oxide capacitance, and V_{TH} is the threshold voltage. Since both the source terminals of M1 and M2 are connected to the input signal, the charge injection caused by M1 and M2 when they are turned off is signal-dependent. On the contrary, the charge injection due to the turning off of M3 and M4 is signal-independent. Although the charge injection introduced by M5 and M6 is signal-dependent, these offset charges introduce no influence while the hold capacitor is sampling the input signal.

The timing diagram of the proposed ADC is shown in the Fig. 3. Fig. 4 shows the SHA of the proposed ADC. The dummy switches MD1 to MD4 are added to alleviate the charge injection by absorbing the charge injected into the capacitor. The size of dummy switches are chosen to be smaller than normal switches. In the proposed design, the size of the dummy switches is one half of that of the normal switches. To further reduce the nonlinearity due to the signal-dependent charge injection, the bootstrap switch [3] is adopted instead of the traditional MOS switch. The schematic of the bootstrap switch is shown in Fig. 5. When ϕ_S is low, the switch M12B is turned off. Boosting circuit provide a high voltage ($> V_{dd}$) to drive M3B such that capacitor C3 can be charged to V_{dd}. When ϕ_S is high, M12B operates in the triode region, and C3 works as a battery across the gate and source of M12B. Hence, the gate voltage of M12B equals to V_{dd} plus V_{in}, which makes the V_{gs12B} become independent of V_{in}. Therefore, the charge injection of the bootstrap switch becomes signal-independent. Since the configuration of the SHA is fully differential, the offset charge due to the signal-independent charge injection can be eliminated. The size of C3 should be large enough to suppress the loading effect caused by parasitic capacitances.

2.2 1.5-bit ADC

The 1.5-bit ADC is composed of an MDAC of a sub-ADC, where the sub-ADC is composed of two compartors. Fig. 6 shows the block diagram of the 1.5-bit ADC. During the *sample* phase, the input signal is sampled by C_S (sample capacitor) and C_F (feedback capacitor). Meanwhile, the input signal is quantized by the sub-ADC to generate a 2-bit digital code, D. Referring to Fig. 3, ϕ_{SA} is the advance version of ϕ_S. When ϕ_{SA} is high, the OP is configured as unity-gain feedback to perform the autozeroing. Besides, ϕ_{SA} is also used to implement the bottom plate sampling [4], which reduces the charge injected into capacitor C_S. During the *hold* phase, C_S is connected to V_{ref+}, V_{ref-}, or V_{cm} according to the digital code, D. Therefore, the relationship between the input and the output of the 1.5-bit ADC can be expressed as following equation :

$$V_{out} = \begin{cases} (1 + \frac{C_S}{C_F})V_{in} - V_{ref}, \text{if } V_{in} > V_{ref}/4 \\ (1 + \frac{C_S}{C_F})V_{in}, \text{if } -V_{ref}/4 \leq V_{in} \leq V_{ref}/4 \\ (1 + \frac{C_S}{C_F})V_{in} + V_{ref}, \text{if } V_{in} < -V_{ref}/4 \end{cases} \quad (2)$$

where $V_{in} = V_{in+} - V_{in-}$, $V_{out} = V_{out+} - V_{out-}$, and $V_{ref} = V_{ref+} - V_{ref-}$. C_S is set to be equal to C_F to attain the inter-stage gain of 2. Since the mismatch of C_S and C_F will directly result in the non-linearity of the ADC, the layout of capacitors should be extremely careful. One of the major advantage of the 1.5 bit ADC is that the resolution of 1.5-bit per stage allows large correction tolerance for comparators. Since only two comparaotrs are required in the sub-ADC, where the tolerance is up to $\pm V_{ref}/4$ [5].

2.3 Dynamic comparator

Since there are a total of 19 comparators in the proposed 10-bit ADC (2 comparators per 1.5-bit ADC, and 3 comparators for the 2-bit flash ADC), the dynamic comparators [6] are adopted to reduce the power consumption. Fig. 7 shows the schematic of the dynamic comaprator. The dynamic comparator only operates at the low-to-high transition of *clk* signal, such that it consumes less power than traditional comparators.

3 Implementation and Simulation

The proposed ADC design is carried out by TSMC (Taiwan Semiconductor Manufacturing Company) 0.18 μm 1P6M CMOS technology to verify the performance. The layout of the proposed prototype on silicon is shown in Fig. 8. Fig. 9 presents the differential nonlinearity (DNL) of the proposed ADC where the maximum is 0.8 LSB. Meanwhile, Fig. 10 depicts the integral nonlinearity (INL) where the maximum is 0.85 LSB. Fig. 11 shows SFDR of 62 dBc with a full-scale sinusoidal input at 700 KHz. The specifications of the proposed prototype are summarized in Table 1. A comparison of the proposed ADC and several prior works is summarized in Table 2. The proposed design possesses less area as well as the acceptable power consumption.

4 Conclusion

A 10-bit, 30 MSample/s pipeline ADC for DVB-H receiver is presented in this paper. By using sev-

Technology	0.18μm CMOS
Power supply	3.3 V
Conversion rate	30 MS/s
Resolution	10 bits
Full-scale input range	2 V p-p differential
DNL	0.8 LSB
INL	0.85 LSB
SFDR	62 dBc
Area	0.27 mm^2
Power consumption	37 mW@30 MS/s

Table 1: Specifications of the proposed ADC

	ours	[5]	[7]	[3]
conversion rate (MS/s)	30	20	30	14.3
power consumption (mW)	37	35	60	36
resolution (bits)	10	10	10	10
chip Area (mm^2)	1.18	10.5	1.36	5.75

Table 2: Comparison

eral techniques, including bootstrap circuitry, bottom plate sampling, and dummy switches, the nonideality of SHA is reduced, such that the specification of OP-amps can be relaxed. Hence, the power consumption of SHA can be significantly reduced. Also, the dynamic comparator is adopted to reduce the power consumption. Therefore, the post-layout simulation result shows that the maximum power consumption is merely 37 mW at a 30 MS/s conversion rate.

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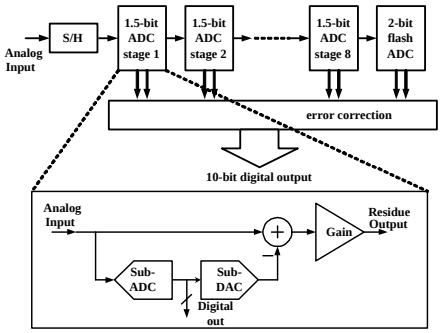

Figure 1: Block diagram of the pipeline ADC

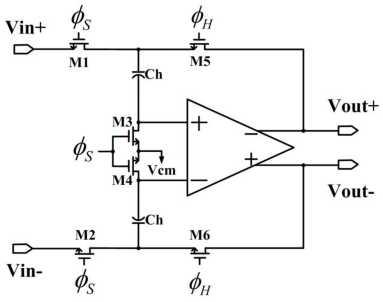

Figure 2: A prior simple SHA

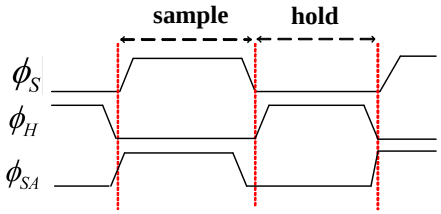

Figure 3: Timing diagram

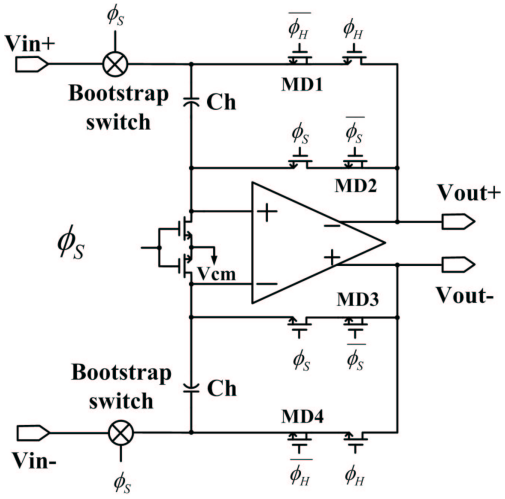

Figure 4: The SHA of the proposed ADC

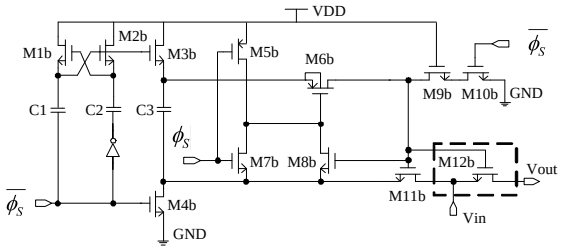

Figure 5: Schematic of bootstrap switch

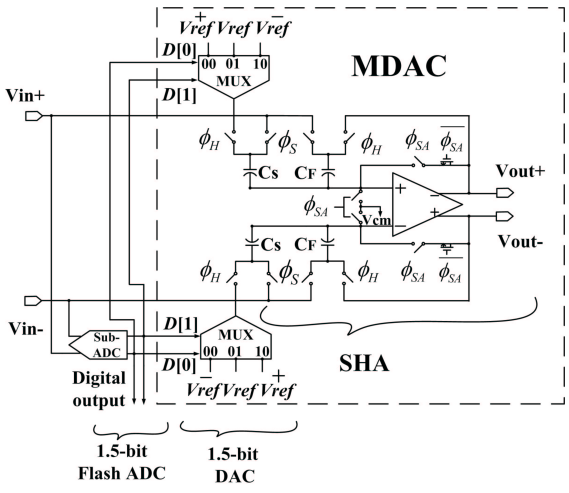

Figure 6: 1.5-bit ADC

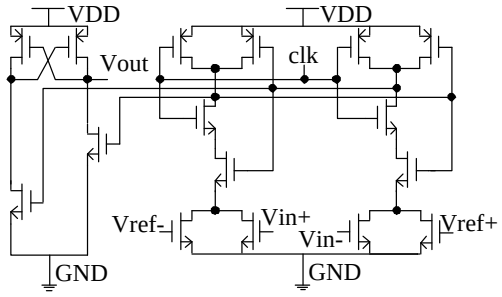

Figure 7: Schematic of the dynamic comparator

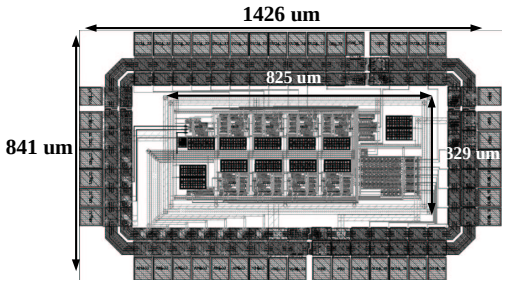

Figure 8: Layout of the proposed ADC

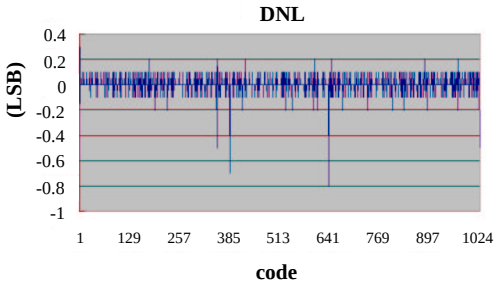

Figure 9: DNL of the proposed ADC

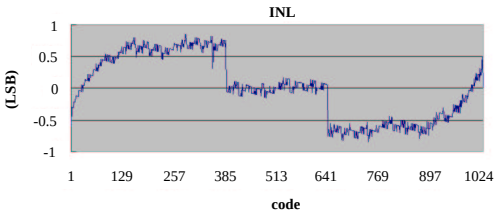

Figure 10: INL of the proposed ADC

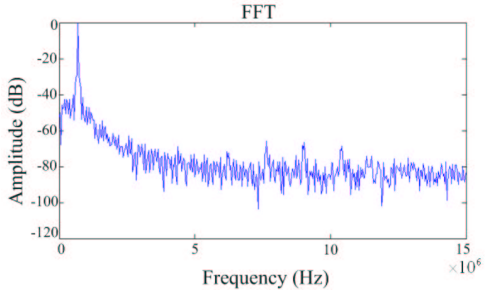

Figure 11: FFT plot of the proposed ADC