A 6.57 mW ZigBee Transceiver for 868/915 MHz Band[§]

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***Abstract*— This paper presents an architecture as well as the circuit implementation of a ZigBee transceiver using 868/915 MHz band, which is compliant to the physical layer of IEEE 802.15.4. Two low-power analog-to-digital converters (ADC) are integrated within the proposed transceiver. The ADC is a 5-bit SA-based (successive approximation) structure. The post-layout simulation shows the packet error rate (PER) is less than 1% given SNR = 5 dB. The overall power consumption is merely 6.57 mW (Tx power = 3.28 mW, Rx power= 3.29 mW).**

I. Introduction

ZigBee is a new wireless standard which targets at a low power, low data rate, wireless short range data transformation. The physical layer and the media access control layer (MAC) of the ZigBee follows the IEEE 802.15.4 wireless personal area network (WPAN) [1]. Meanwhile, its application layer and security layer are defined by the ZigBee Alliance [2]. According to the transmitting frequency, the physical layer of the ZigBee can be distinguished into 2.4 GHz mode and 868/915 MHz mode (868 MHz for North American and 915 MHz for Europe). The data rate and the modulation scheme of ZigBee for these two modes are different. Owing to the low data rate and the simple modulation scheme, the ZigBee using 868/915 MHz band possesses the edge of the cost over the ZigBee using 2.4 GHz band. Therefore, it is extremely suitable for the sensor applications and home automation. The specification of data rate and frequency band for ZigBee protocol are summarized in Table I.

TABLE I
SPECIFICATION OF DATA RATE AND FREQUENCY BAND

Freq. Band	Data Rate	Modulation
868/915 MHz	300/600 Kbps	BPSK

Fig. 1 depicts the structure of the ZigBee physical layer protocol data unit (PPDU) packet. The preamble field, which contains 32 bits "0", is for the packet detection and the synchronization in the receiver. The SFD field denotes the start of the packet data. The frame length field indicates the number of octets of the physical layer service data unit (PSDU). The PSDU conveys the payload of the packet.

Octets : 4	**1**	**1**		**variable**
Preamble	Start of frame delimiter	Frame length (7 bits)	Reserved (1 bit)	PSDU
Synchronization header		PHY header		PHY payload

Fig. 1. PPDU packet structure

The ADC is the most critical interface circuit in general communication systems. Due to the design complexity of the mixed-signal systems, the analog circuits and digital cores are partitioned into two individual parts in these systems. However, the top-down design flow and the system simulation can improve the reliability while designing a mixed-signal system. In this paper, we propose a low-power ZigBee transceiver design using 868/915 MHz, where ADCs are integrated therein. The system simulation are performed to determine the specification of ADCs before the physical design.

II. ZigBee transceiver design

Fig. 2 shows the detailed block diagram of the proposed ZigBee receiver. The RF signal is down-converted to baseband by the RF receiver (Rx) and quantized by the analog-to-digital converters (ADC). These digital signals are sent to the MAC after the digital demodulation performed by the proposed Rx. The PSDU from MAC is modulated by the proposed Tx, and the resultant PPDU packet is transmitted by the RF transmitter. The details of each block are described in the following text.

A. proposed ZigBee Tx

The proposed ZigBee Tx in Fig. 3 is based on [1], and its detailed block diagram is shown in Fig. 3. The PPDU packet is composed of the PSDU from MAC and the header added by the header insertion stage. The differential encoder stage encodes the PPDU packet for error correction. The bit-to-chip stage performs the direct-sequence spread spectrum (DSSS), where each bit of the PPDU packet is mapped

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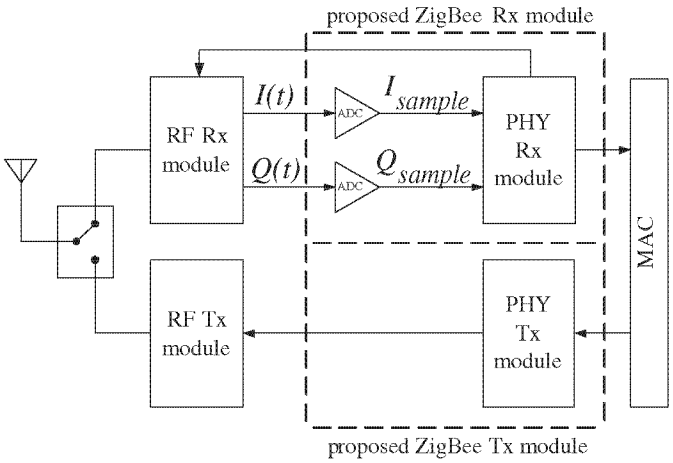

Fig. 2. Block diagram of the ZigBee transceiver for 868/915 MHz band

into a 15-chip pseudo-random noise (PN) sequence ("0" to "111101011001000", and "1" to "000010100110111"). Notably, the binary phase shift keying (BPSK) modulation is adopted in 868/915 MHz mode. The modulated signal goes along with the pulse shaping stage to reduce the inter-symbol interference (ISI) [3], and the resultant signal is transmitter by the RF transmitter.

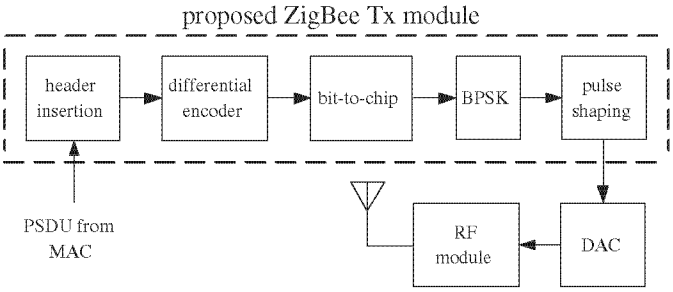

Fig. 3. Detailed block diagram of the proposed ZigBee Tx

B. proposed ZigBee Rx

Fig. 4 shows the block diagram of the ZigBee Rx. The packet detector discriminates whether the incoming signal is data or noise. It enables the following stage if the incoming signal is determined to be data. Each 15-chip PN sequence is sampled to be 60 samples by the ADC. The energy detector is in charge of positioning the chips from the samples. The frequency estimation block computes the frequency offset from samples and corrects the frequency of local oscillator by returning a control signal. The time synchronization indicates the start of each PPDU packet. With the acknowledgement of the start of the packet, the differential decoder proceeds to decode the packet. The confirm SFD stage acquires the length of the PSDU and notifies the MAC layer of receiving the PSDU from the receiver.

1) Packet Detector and Energy Detector: The absolute value of I_{sample} and Q_{sample} are accumulated for certain time

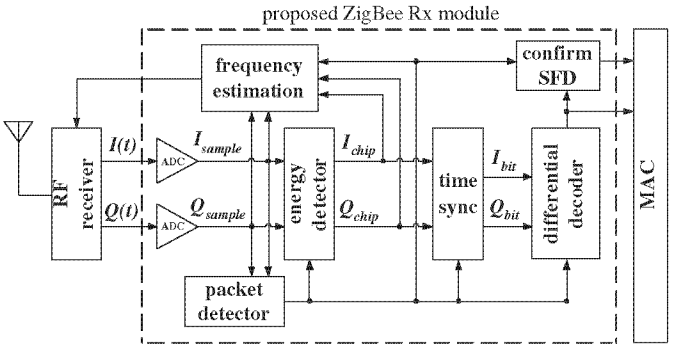

Fig. 4. Detailed block diagram of the proposed ZigBee Rx

interval. If the accumulated value is greater than a predefined threshold, the incoming signal is determined as data. This threshold is derived from detailed system simulations. The energy detector derives the positions of the chips from I_{sample} and Q_{sample}.

2) Frequency Estimation: The frequency estimation consists of two phases, coarse and fine estimation. The frequency estimation stage performs similar operations in these two phases such that the hardware can be reused. The phase angle of a pair of I_{sample} and Q_{sample} can be obtained by mapping the I_{sample} and Q_{sample} to the Cartesian coordinate. A phase rotation is the difference between two adjacent phase angles. In the coarse phase, the frequency estimation stage calculates the average phase rotation of 128 pairs of I_{sample} and Q_{sample}. Then, it corrects the frequency of the local oscillator by returning an 8-bit control signal. In the fine phase, it uses I_{chip} and Q_{chip}, which are derived from I_{sample} and Q_{sample} by the energy detector, to calculate the average phase rotation and send an 8-bit control signal to the local oscillator.

3) Time Synchronization: The time synchronization stage de-spreads the received chips by a matched filter [4] and acquires the preamble of PPDU. The incoming I and Q chips are converted from chips to bits for decoding.

4) Confirm SFD: The confirm SFD stage determines the frame length by acquiring the SFD field of the PPDU packet and acknowledges the MAC layer to receive the PSDU by sending an alarm signal.

C. ADC for ZigBee Rx

Refer to Fig. 2, two ADCs are needed to quantize the in-phase signal, I, and quadrature phase signal, Q. In order to provide sufficient samples for phase error estimation in the demodulator, the sampling rate of the ADC is set to be four times the frequency of the input signal. Hence the sampling rate of the ADC is 2.4 MS/s. The requirement of the ADC resolution is derived from the system simulation illustrated in Fig. 5. According to [1], the packet error rate (PER) should be less than 1% when the signal-to-noise (SNR) ratio is 5 to 6 dB. Referfing to Fig. 5, a 4-bit resolution is sufficient even when the SNR of the input signal is 4 dB. The resolution of the proposed ADC is chosen to be 5-bit to ensure the integrity of the quantization. Hence, the ADC in Fig. 2 is determined

to be a 5-bit, 2.4 MS/s ADC, which is a low speed, and low resolution ADC.

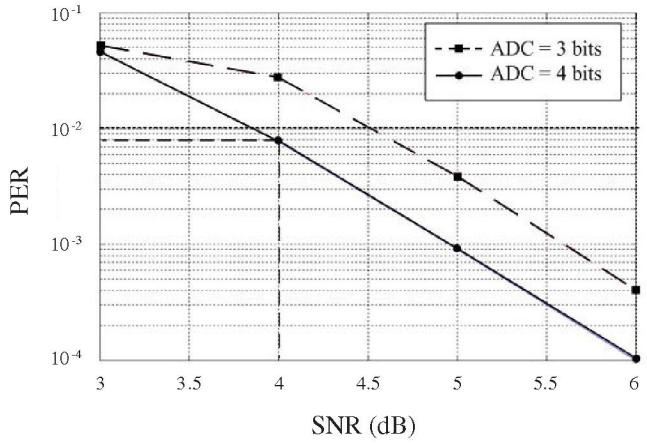

Fig. 5. The resolution requirement of the ADC is derived from system simulation

The architecture of the ADC to meet the requirement of such a low speed, low resolution ADC includes flash ADC, pipeline ADC, and successive approximation ADC. However, the successive approximation ADC [5], [6], [7], is the most power-efficient architecture in the low speed applications. Therefore, we adopt a low-power successive approximation ADC for ZigBee Rx using 868/915 MHz band.

The successive approximation ADC is mainly based on the "binary search" algorithm. The architecture of the proposed successive approximation ADC is illustrated in Fig. 6. The input signal V_{in} is sampled by the sample-and-hold block, and then the sampled signal is subtracted from the output of the digital-to-analog converter (DAC). The comparator determines the polarity of D_{out}. The CONTROL block sends the control signal $en[4:0]$ to the successive approximation latch (SAL) block based upon the output of the of the comparator, C_{out}. Then, the SAL block changes the output of the DAC according to C_{out}. Each bit of the ADC output is obtained in one conversion cycle. Therefore, a complete output of the ADC takes five conversion cycles. After the proposed successive approximation ADC completes the five-bit quantization, the signal EOC is asserted to declare the end of the conversion.

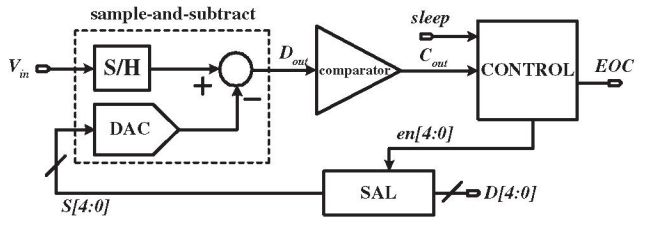

Fig. 6. The architecture of the successive approximation ADC

Fig. 7 shows the sample-and-subtract block, which performs the sample-and-hold and subtraction. The architecture of this block is based on the charge redistribution DAC. The operation of this block in one conversion cycle contains two phases, *sampling* and *subtraction*. In the beginning of the *sampling* phase, the capacitors array are discharged by closing the reset switch. Then, the top plates of the capacitor array connect to the input signal, V_{in}, while the bottom plates still connect to V_{refn}. In the *subtraction* phase, the reset switch opens, and the top plates of capacitors connect to V_{refn} or V_{refp} according to the control signal, $S[k]$ (k=0,1,...,4). If the $S[k]$ is high, the top plate of the capacitor connects to V_{refp}. Otherwise, the top plate connects to V_{refn}. The output of this block, D_{out}, can be expressed as follows :

$$D_{out} = -(V_{in} - V_{refn}) + \sum_{k=0}^{4} S[k] \cdot \frac{V_{ref}}{2^{(5-k)}}, \qquad (1)$$

where V_{ref}=$V_{refp} - V_{refn}$.

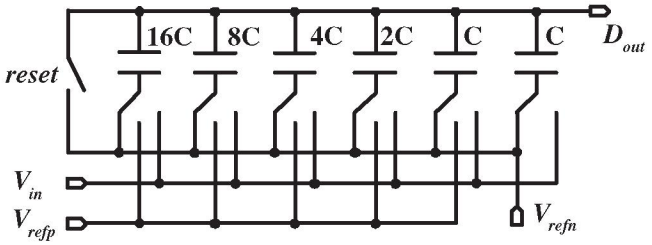

Fig. 7. The architecture of the sample-and-subtract block

III. Simulation and Implementation

The proposed ZigBee transceiver design is carried out by TSMC (Taiwan Semiconductor Manufacturing Company) 0.18 μm CMOS technology to verify the performance. All of the process corners : [0°C, +100°C], and (SS, TT, FF) models, are simulated. The layout of the proposed prototype is shown in Fig. 8. Fig. 9 shows that the PER is less than 1% at SNR of 5 dB when the frequency offset of a symbol (1 symbol = 15 chips), Δf, is +4 ppm $\sim$ -4 ppm. The differential nonlinearity (DNL) and the integral nonlinearity (INL) of the proposed ADC are 0.2 LSB and 0.3 LSB, respectively. Fig. 10 shows the spurious-free dynamic range (SFDR) of 30 dB with a sinusoidal input at 590 KHz. The efficient number of bits (ENOB) is around 4.68 bits, which is sufficiently to meet the requirement of ZigBee applications. The overall power consumption of the proposed ZigBee transceiver is 6.57 mW (Tx power = 3.28 mW, Rx power= 3.29 mW). The specifications of the ADC and proposed ZigBee are summarized in Table II and III, repectively. The comparison between the proposed ZigBee transceiver and the commercial product is summarized in Table IV

IV. Conclusion

In this paper, we propose an architecture as well as circuit implementation of the mixed-signal ZigBee transceiver design. The ADCs are integrated within the proposed transceiver,

TABLE II

SPECIFICATIONS OF THE ADC

Technology	0.18 μm
Power supply	1.8 V
Sample rate	2.4 MHz
Resolution	5 bits
DNL	0.2 LSB
INL	0.3 LSB
SFDR	30 dB
ENOB	4.68 bits
core size	0.028 mm^2
Power consumption	449.6 μW@2.4 MHz

TABLE III

SPECIFICATIONS OF THE PROPOSED ZIGBEE TRANSCEIVER

Technology	0.18 μm
Power supply	1.8 V
Clock rate	2.4 MHz
Power consumption of Tx	3.28 mW
Power consumption of Rx	3.29 mW
core size	2.9 mm^2

TABLE IV

COMPARISON BETWEEN THE COMMERCIAL PRODUCT AND THE PROPOSED DESIGN

Design	Mode	Tx power	Rx power	Power supply
ours	868/915 MHz	3.28 mW	3.29 mW	1.8 V
Atmel - AT86RF210 Z-Link	868/915 MHz	108* mW	26.1* mW	1.8 V

(*NOTE : The power consumption contains the power of RF Tx and RF Rx.)

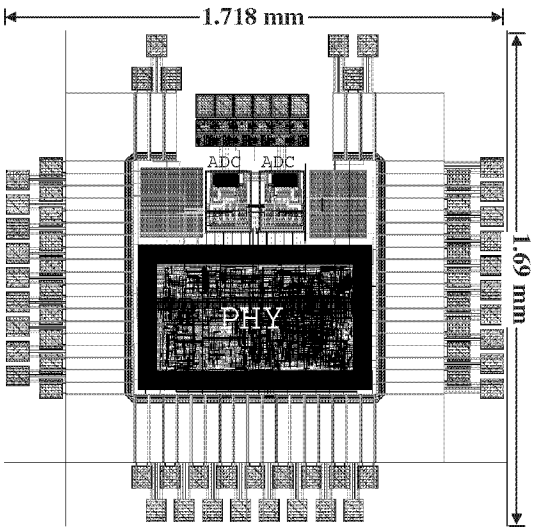

Fig. 8. Layout of the proposed prototype

where the required specification of ADC is derived from system simulation to ensure the validity of mixed-signal integration before circuit-level design. The overall power dissipation is merely 6.56 mW, which is capable of achieving the low power data transmission.

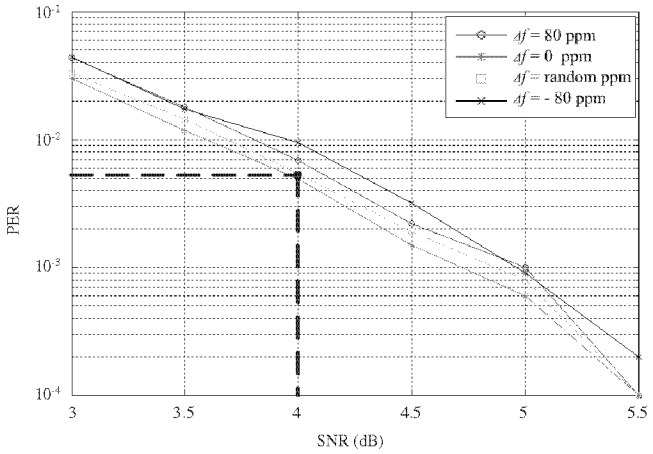

Fig. 9. PER of the proposed ZigBee Rx

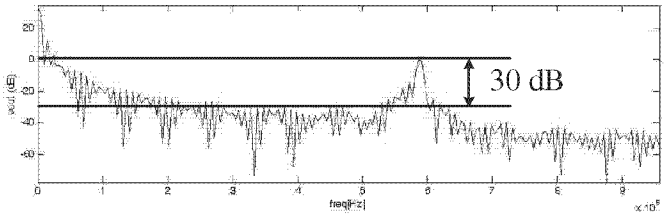

Fig. 10. The spurious-free dynamic range of the ADC

REFERENCES

[1] IEEE Std. 802.15.4: Wireless Medium Access Control (MAC) and Physical Layer (PHY) specifications for Low Rate Wireless Personal Area Networks (LR-WPANs), 2003.

[2] Web site : http://www.ZigBee.org.

[3] H. P. E. Stern, and S. A. Mahmoud, *Communication Systems: Analysis and Design.* Prentice Hall PTR, 2003.

[4] G. J. R. Povey, and P. M. Grant, "Simplified matched filter receiver designs for spread spectrum communication applications," *Electronics and Communication Engineering Journal*, vol. 5, no. 2, pp. 59-64, Apr. 1993.

[5] S. Mortezapour, and E. K. F. Lee, "A 1-V, 8-bit Successive Approximation ADC in Standard CMOS Process," *IEEE Journal of Solid-State Circuits*, Vol. 35, no. 4, pp. 642-646, Apr. 2000.

[6] C. S. Lin, and B. D. Liu, "A New Successive Approximation Architecture for Low-Power Low-Cost CMOS A/D Converter," *IEEE Journal of Solid-State Circuits*, Vol. 38, no. 1, pp. 54-62, Jan. 2003.

[7] J. Sauerbrey, D. Schmitt-Landsiedel, and R. Thewes, "A 0.5-V 1-uW Successive Approximation ADC," *IEEE Journal of Solid-State Circuits*, Vol. 38, no. 7, pp. 1261-1265, Jul. 2003.