A 4-Kb Low Power 4-T SRAM Design with Negative Word-Line Gate Drive[§]

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***Abstract*— The physical implementation of a prototypical 250-MHz CMOS 4-T SRAM is described in this paper. The proposed SRAM cell takes advantage of a negative word-line gate drive to minimize the leakage current of the cell access transistors. As a result, the standby power consumption is drastically reduced. The proposed 4-Kb 4-T SRAM is measured to consume 0.12 mW in the standby mode, and a 3.8 ns access time in the R/W mode. The highest operating clock rate is measured to be 263 MHz.**

I. Introduction

The leakage current of the memory will be increased with the capacity such that more power will be consumed even in the standby mode. Many prior schemes [2]-[5] have been mentioned to improve the standby power consumption of the SRAM. [6]- [8] described a negative word-line scheme to reduce the system supply voltage by lowering the threshold voltage of the cell access transistor for low voltage DRAMs. In this paper, we propose a deterministic negative word-line gate drive method to minimize the operating leakage current and to reduce the idle power consumption. Besides, a current-mode sense amplifier is also employed to nullify the loss of the access speed.

II. Low Power 4-T SRAM Design

According to [1], a unified active power consumption for modern CMOS SRAM is approximately given for a normal read cycle by

$$P = V_{DD} I_{DD}, \quad (1)$$

$$I_{DD} = m i_{act} + m(n-1) i_{hld} + (n+m) C_{DE} V_{INT} f + C_{PT} V_{INT} f + I_{DCP}, \quad (2)$$

where P is the total power dissipation, V_{DD} is an external supply voltage, I_{DD} is a current from V_{DD}, m is the number of memory cells on a word-line, n is the number of the columns of a memory cell array, i_{act} is an effective current of active or selected cells, i_{hld} is an effective data retention current of inactive or non-selected cells, C_{DE} is an output node capacitance of each decoder, V_{INT} is an internal supply voltage, C_{PT} is a total capacitance of CMOS logic and driving circuits in periphery, I_{DCP} is a total static (DC) current of periphery, and f is the operating frequency. To save power by reducing i_{hld} and reduce the cell area, we select 4-T SRAM cells to construct the memory. A basic 4-T SRAM cell is shown in Fig. 1.

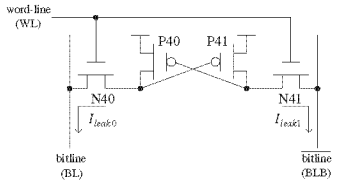

Fig. 1. Basic 4-T SRAM cell

The major goal in this design is to decrease the data retention current of inactive cells, which is i_{hld}, to nullify the leakage current of the cell access transistors, N40 and N41. There were two major control schemes to reduce the leakage current of the cell access transistors : negative bulk (NB) bias, and negative word-line (NWL) voltage.

A. Negative Bulk Scheme

According to [9], we attain the following V_{TH} formulation,

$$V_{TH} = V_{TH0} + \gamma(\sqrt{|\,2\phi_F\,| + V_{SB}} - \sqrt{|\,2\phi_F\,|}), \quad (3)$$

where V_{TH0} denotes the threshold voltage with a zero bulk bias, ϕ_F is electrostatic potential, γ is the body coefficient, and V_{SB} is the bulk bias. Applying a negative bias to the bulk of NMOS or a positive bias to that of PMOS, the V_{TH} will be increased and the leakage current, on the contrary, wll be reduced. Fig. 2 shows the simulation circuit and the results of the NB scheme when V_{bulk} is varied from -1.4 V to 0 V, given TT model, VDD = 1.8 V, 25°C. It is found that the leakage current will be raised when V_{bulk} < -0.7 V, and the minimum leakage current is 4.3736 pA.

B. Negative Word-line Scheme

Fig. 3 shows the simulation circuit and the results of the NWL scheme when V_{WL} is varied from -1.4 V to 0 V, given TT model, VDD = 1.8 V, 25°C. It is found that the leakage current will be reduced and then maintained at the minimum current when V_{WL} < -0.4 V. The minimum leakage current is 3.6 pA.

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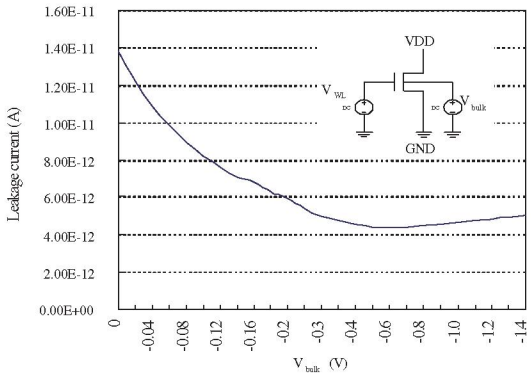

Fig. 2. Simulation circuit and results of the NB scheme

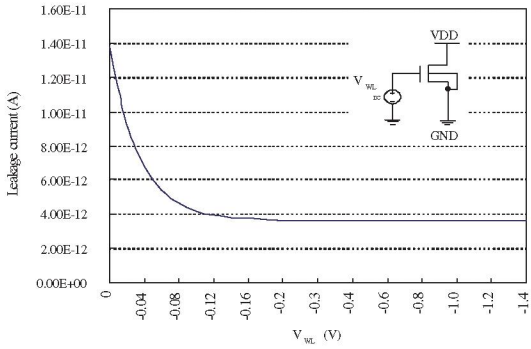

Fig. 3. Simulation circuit and results of the NWL scheme

C. Comparison of the Negative Bulk and the Negative Word-line

The comparison of the mentioned schemes is shown in Fig. 4. The leakage current of the NWL scheme is smaller than that of the NB scheme. Moreover, in order to attain the minimum leakage current, the NB scheme needs a firmly stable bias ≈ -0.7 V, but the NWL scheme only needs keeping the bias below -0.4 V. Besides, for the NB scheme, a triple-well structure is required to isolate the well voltage of the transistor. Hence, the area required by the design rules if the NB scheme is adopted will be increased.

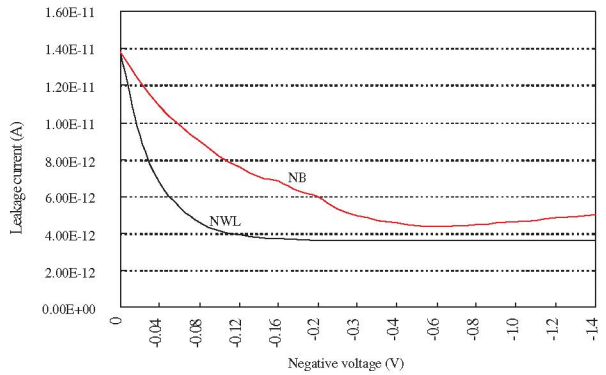

Fig. 4. Comparison of the NB with the NWL scheme for the leakage current

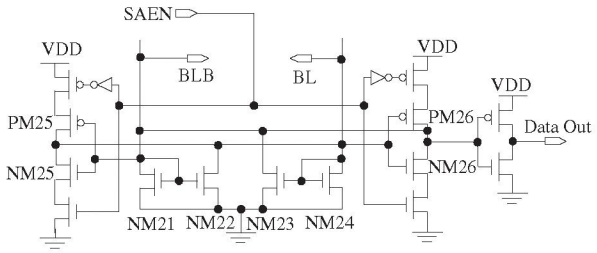

Fig. 5. Sensing amplifier circuit with enable control

Besides the NWL scheme, we use several approaches to maintain operating speed while save power.

(1) The 4-Kb memory array is partitioned into four 1-Kb banks. A predecoder controls the bank enable signals to reduce the accessing memory capacity.
(2) The pulse operation [10] is adopted to shorten the memory access time. Hence, memory cells and sensing amplifier will be closed to avoid any unwanted current when the access operation is finished.
(3) Referring to the sensing amplifier (SA) [11] in Fig. 5, NM21 - NM24 consists the current-mode amplifier stage, while NM25, NM26, PM25, and PM26 are the voltage-mode amplifier stage of the SA. The small input impedance of the current-mode amplifier alleviates the loading effect on the bitlines of SRAM cells such that the sensing speed is enhanced. The voltage-mode amplifier is reponsible for boosting the logic levels to full swing. A sensing amplifier enable signal (SAEN) is used to eliminate unnecessary DC current when the memory in the standby mode or the write operation.

III. Simulation and Implementation

A. Simulation

The proposed design is implemented by TSMC (Taiwan Semiconductor Manufacturing Company) 1P6M 0.18 μm CMOS process. Fig. 6 shows the architecture of the SRAM. The proposed memory also comprises a built-in self test (BIST) circuit as shown in Fig. 7. The post-layout simulations of the chip are tabulated in Table I. The worst-case average power is 0.11 mW in the standby mode. The longest access time is 3.38 ns and access average power is 23.2 mW in R/W mode. The highest operating clock frequency is 250 MHz. Fig. 8 shows the worst-case post-layout simulation result give by TimeMill at 75°C, SS model, VDD = 1.6 V, and D_{out} load is 15 pF. In Fig. 8, we write 0 and 1 to two adjacent memory cells and then read data from these cells. Address latching and data accessing are executed at positive edges of the clock (CLK). WR_RE is the read/write control line of which logic 1 is the write operation, and logic 0 denotes the read operation.

Fig. 9 shows the simulation results of the BIST mode at 25°C, TT model, VDD = 1.8 V. If any fail occurs, the FAIL will be pulled high. The FAIL stays at low to indicate the BIST test is good.

TABLE I

POST-LAYOUT SIMULATION OF THE PROPOSED SRAM

normal mode	clock	250 MHz
	access time	3.38 ns
	VDD	1.8 V
	avg. power	23.20 mW
	max power	130.09 mW
BIST mode	clock	100 MHz
	VDD	1.8 V
	avg. power	11.73 mW
	max power	95.65 mW
standby mode	avg. power	0.11 mW

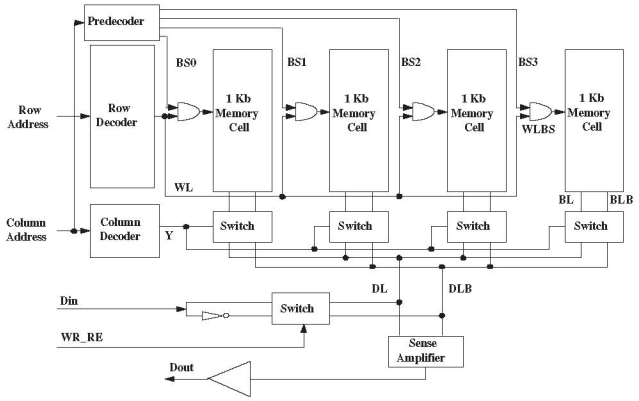

Fig. 6. Architecture of the SRAM

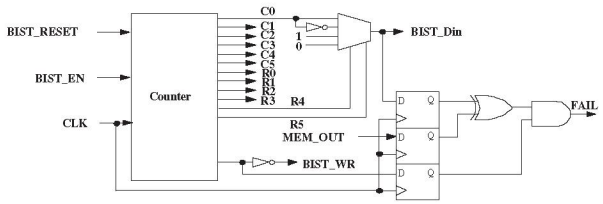

Fig. 7. Built-in self test circuit

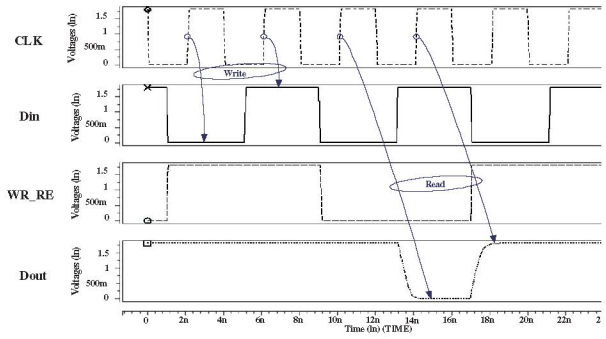

Fig. 8. Worst-case post-layout simulation

B. Implementation & Measurement

Fig. 10 shows the die photo of the proposed SRAM chip. An IMS ATS100 logic master is used to perform chip test and measurement. The maximum operating clock frequency supported by the mentioned instrument is only 100 MHz. The functions of the general (synchronous) mode and BIST mode

Fig. 9. Simulation results of the BIST mode

have been proved by the testing of continuous read/write of row/column addresses. Fig. 11 shows the signal-fetch settings of the general mode and the BIST mode. Fig. 12 shows the measured waveform of read/write operations. In Fig. 12, we write 0,1,0,1,1,0,1,0, continuous 0 and continuous 1 to 4 rows and 1 to 4 columns, i.e., 16 adjacent memory cells. Then, read data from these cells. Notably, Fig. 11 shows the output data fetch delay is 3.80 ns, which indicates the highest operation speed of the proposed design is 263 MHz. Fig. 13 shows that the power consumption of the proposed chip is a function of the clock rate. The curve (1) is the average power consumption for the word-line voltage = 0 V, while the curve (2) is the average power consumption for the word-line voltage = -0.7 V. Notably, the power consumption in the standby mode is 0.55 mW for 0 V word-line voltage, while the power consumption in the standby mode is 0.12 mW for -0.7 V word-line voltage. Table II summarizes the physical measurement results.

A power consumption and power-delay product comparison with prior works is shown in Table III. It is obvious that the proposed design possesses the smallest power consumption and power-delay product.

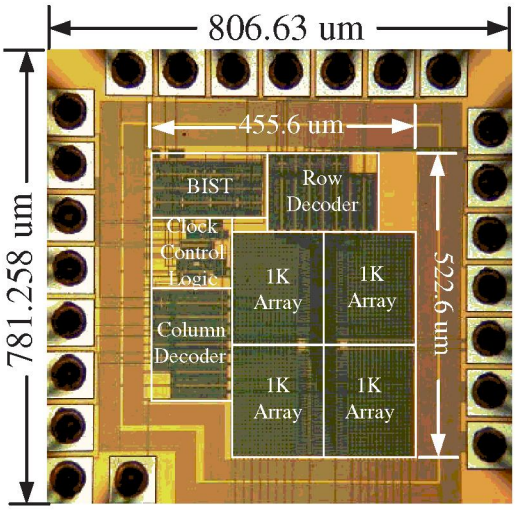

Fig. 10. Die photo of the proposed SRAM

TABLE III

COMPARISON OF POWER-DELAY PRODUCT

	[4]	[5]	Proposed
CMOS Process	1P6M 0.18 μm		
Power	152 mW (500 MHz)	182 mW (667 MHz)	23.2 mW (250 MHz)
Power/(bit*MHz) (nW/MHz)	74.22	66.62	22.66
Access Delay (ns)	2.49	2.2	3.38
Power*Delay/(bit*MHz) (ns*nW/MHz)	184.8	146.56	76.58

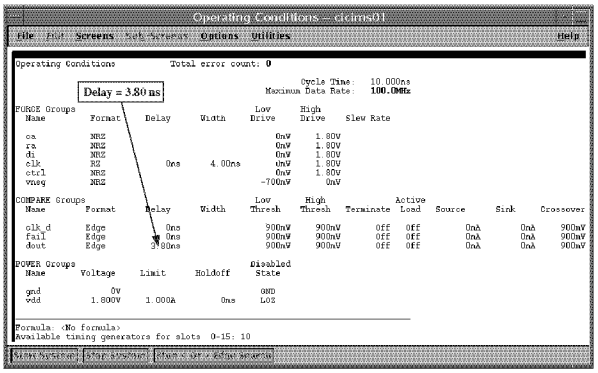

Fig. 11. General R/W mode operation and the signal-fetch conditions

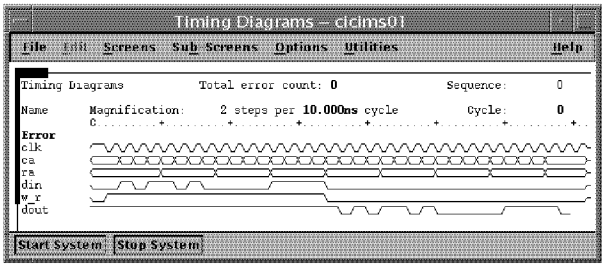

Fig. 12. Measured waveform of the read/write operation

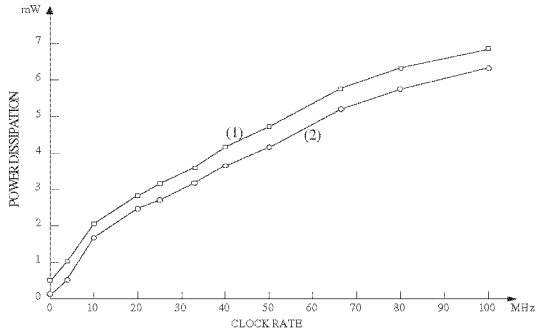

Fig. 13. Power consumption of the proposed SRAM as a function of the clock rate

TABLE II

PHYSICAL MEASURING RESULTS

Max. Freq.	100 MHz ‡
Avg. Power	6.24 mW (100 MHz, 1.8 V)
Access Time	3.8 ns
Standby Power	0.12 mW

‡ : Limited by the measurement instrument (IMS ATS100).

IV. CONCLUSION

We have revealed a 4-Kb 4-T CMOS SRAM by using the NWL scheme to achieve low power dissipation. The proposed design does not need any special CMOS process, e.g., multiple-well layers. The leakage current of the cell access transistors is kept minimum as long as word-line voltage is below -0.4 V. Hence, the power consumption of the inactive cells in the standby mode is drastically reduced.

V. ACKNOWLEDGMENT

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