LOW-POWER 5-BIT 2.4 MS/S SUCCESSIVE APPROXIMATION ADC FOR ZIGBEE RECEIVER USING 868/915 MHZ BAND[§]

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ABSTRACT

This paper presents a 5-bit, 2.4 MS/s, low power analog-to-digital converter for ZigBee receiver using 868/915 MHz band. The converter uses successive approximation architecture. By using 0.18 μm CMOS technology, the post-layout simulation shows the worst-case power consumption is merely 449.6 μW. The converter achieves the maximum differential nonlinearity of 0.2 LSB, the maximum integral nonlinearity of 0.3 LSB, and area of 0.028 mm^2.

1 Introduction

ZigBee is a wireless standard which targets at a low power, low data rate, wireless data transformation. The physical layer and the media access control layer (MAC) of the ZigBee follows the IEEE 802.15.4 wireless personal area network (WPAN) [1]. Meanwhile, its application layer and security layer are defined by the ZigBee Alliance [2]. According to the transmitting frequency, the physical layer of the ZigBee can be distinguish into 2.4 GHz mode and 868/915 MHz mode (868 MHz for North American and 915 MHz for Europe). The data rate and the modulation scheme of ZigBee for these two modes are different. Owing to the low data rate and the simple modulation scheme, the ZigBee using 868/915 MHz band possesses the edge of the cost over the ZigBee using 2.4 GHz band, such that it is extremely suitable for the sensor application and home automation. The specification of data rate and frequency band are summarized in Table 1.

Fig. 1 shows a general block diagram of the ZigBee receiver (Rx), which requires two analog-to-digital converter (ADC) to quantize the in-phase signal, I, and quadrature phase signal, Q. In order to provide sufficient samples for phase error estimation in the demodulator, the sampling rate of the ADC is set to be four times the frequency of the input signal, hence the sampling rate of the ADC is 2.4 MS/s. The requirement of the ADC resolution is derived from the system simulation illustrated in Fig. 2. According to [1], the packet error rate (PER) should be less than 1% when the signal-to-noise (SNR) ratio is 5 to 6 dB. Refer to Fig. 2, a 4-bit resolution is sufficient even when the SNR of the input signal is 4 dB. The resolution of the proposed ADC is chosen to be 5-bit to ensure the integrity of the quantization. Hence, the ADC in Fig. 1 is determined to be a 5-bit, 2.4 MS/s ADC, which is a low speed, and low resolution ADC.

Freq. Band	Data Rate	Modulation
868/915 MHz	300/600 Kbps	BPSK

Table 1: Specification of data rate and frequency band

The architecture of the ADC satisfied the requirement of such a low speed, low resolution ADC includes flash ADC, pipeline ADC, and successive approximation ADC, however the successive approximation ADC [3], [4], [5], is a most power-efficient architecture in the low speed application. This paper presents a low power successive approximation ADC design, which meets the requirement for ZigBee Rx using 868/915 MHz band.

2 Successive Approximation ADC for ZigBee Rx

The successive approximation ADC is mainly based on the "binary search" algorithm. The architecture of the proposed successive approximation ADC is illustrated in the Fig. 3. The input signal V_{in} is sampled by the sample-and-hold block, and the sampled signal is subtracted from the output of the digital-to-analog converter (DAC). The comparator determines the polarity of D_{out}. The CONTROL block processes the

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result of the comparison, C_{out} and sends the control signal $en[4:0]$ to the successive approximation latch (SAL) block, hence the SAL block change the output of the DAC according to C_{out}. Each bit of the ADC output is obtained in one conversion period, therefore a complete output of the ADC takes five conversion periods. After the proposed successive approximation ADC completes the five bits quantization, the signal EOC is asserted to declare the end of the conversion.

2.1 CONTROL and SAL

Fig. 4 shows the block diagram of the CONTROL block and SAL block. The CONTROL block contains three subblock. In the ZigBee applications, the Rx spends most of its time dozing, hence the ADC should be able to be turn off when there is no input signal. The function of SAL and subblocks of CONTROL are explained as follows :

Reload: The Reload block resets the ADC after the end of the conversion and turn off the ADC when the signal, *sleep*, is asserted.

D_ctrl: The D_ctrl resets the switched-capacitors of the DAC at the end of every conversion period by sending the signal, *reset*, to the DAC. It also generates the clock signal, *clk*, for the comparator and the SHIFT block.

SHIFT: This block is a shift register which generates the control signals, $en[4:0]$, to trigger the SAL.

SAL: The SAL block generates the control signal, $S[4:0]$, to change the output voltage of the DAC and produces the ADC output, $D[4:0]$, every five conversion periods.

2.2 Sample-and-Subtract

Fig. 5 shows the sample-and-subtract block, which performs the sample-and-hold and subtraction. The architecture of this block is based on the charge redistribution DAC. The operation of this block in one conversion period contains two phase, *sampling* and *subtraction*. In the beginning of the *sampling* phase, the capacitors array are discharged by closing the reset switch. Then, the top plates of the capacitor array connect to the input signal, V_{in}, while the bottom plates still connect to V_{refn}. In the *subtraction* phase, the reset switch open, and the top plates of capacitors connect to V_{refn} or V_{refp} according to the control signal, $S[k]$ (k=0,1,...,4). If the $S[k]$ is high, the top plate of the capacitor connects to V_{refp}. Otherwise, the top plate connects to V_{refn}. The output of this block, D_{out}, can be expressed as follows :

$$D_{out} = -(V_{in} - V_{refn}) + \sum_{k=0}^{4} S[k] \cdot \frac{V_{ref}}{2^{(5-k)}}, \qquad (1)$$

where V_{ref}=$V_{refp} - V_{refn}$.

2.3 Dynamic Comparator

Fig. 6 shows the schematic of the comparator, which is a dynamic comparator. In the low-to-high transition of the *clk* signal, the NMOS transistor M1 turns on, and the input signal, D_{out} and V_{refn}, are compared to each other. The result of the comparison, C_{out}, are stored in the latch which is composed of M4, M5, M8, and M9. By contrast, in the high-to-low transition of *clk*, M1 turns off, and C_{out} would be high. The output of comparator would be meaningful only if the *clk* is high. In the dynamic comparator, the DC path only exits at the transition of *clk* signal, such that the dynamic comparator consumes less power than traditional comparators.

3 Simulation Results

The proposed ADC design is carried out by TSMC (Taiwan Semiconductor Manufacturing Company) 0.18 μm CMOS technology to verify the performance. All of the process corner : [0^{o}C, +100^{o}C], and (SS, TT, FF) models, are simulated. The layout of the proposed prototype is shown in Fig. 7. Fig. 8 presents the differential nonlinearity (DNL) of the proposed ADC where the maximum is 0.2 LSB. Meanwhile, Fig. 9 depicts the integral nonlinearity (INL) where the maximum is 0.3 LSB. Fig. 10 shows the spurious-free dynamic range (SFDR) of 30 dB with a sinusoidal input at 590 KHz. The efficient number of bit(ENOB) is around 4.68 bits. The worst-case power consumption is merely 449.6 μW given a 1.8 V power supply. The specifications of the proposed prototype are summarized in Table 2.

Technology	0.18 μm
Power supply	1.8 V
Sample rate	2.4 MHz
Resolution	5 bits
DNL	0.2 LSB
INL	0.3 LSB
SFDR	30 dB
ENOB	4.68 bits
core size	0.028 mm^2
Power consumption	449.6 μW@2.4 MHz

Table 2: Specifications of the proposed ADC

4 Conclusion

This paper presents a ADC design for the ZigBee Rx. The specification of the ADC is derived from the system simulation to meet the requirement of the ZigBee application. The post-layout simulation reveals the power consumption is merely 449.6 μW, such that the proposed ADC is sufficiently suitable for the ZigBee Rx.

References

[1] IEEE Std 802.15.4: Wireless Medium Access Control (MAC) and Physical Layer (PHY) specifications for Low Rate Wireless Personal Area Networks (LR-WPANs), 2003.

[2] Web site : http://www.ZigBee.org.

[3] S. Mortezapour, and E. K. F. Lee, "A 1-V, 8-bit Successive Approximation ADC in Standard CMOS Process," IEEE Journal of Solid-State Circuits, VOL. 35, pp. 642-646, Apr. 2000.

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[5] J. Sauerbrey, D. Schmitt-Landsiedel, and R. Thewes, "A 0.5-V 1-uW Successive Approximation ADC," IEEE Journal of Solid-State Circuits, VOL. 38, pp. 1261-1265, Jul. 2003.

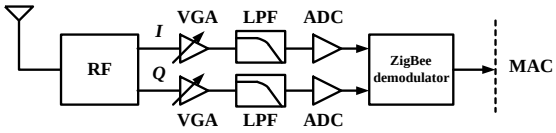

Figure 1: Block diagram of the ZigBee Rx

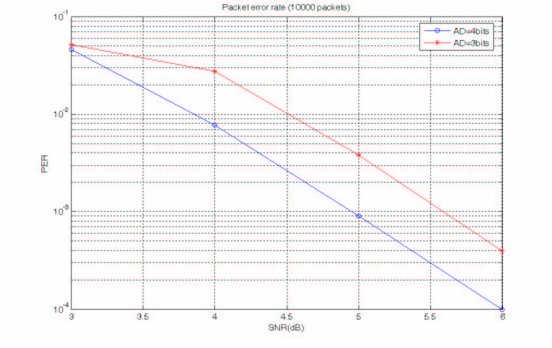

Figure 2: System simulation of the ADC resolution

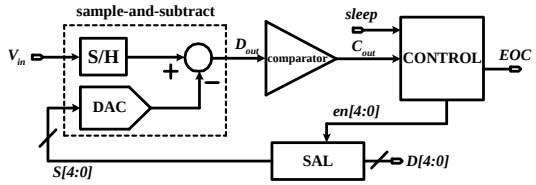

Figure 3: The architecture of the proposed successive approximation ADC

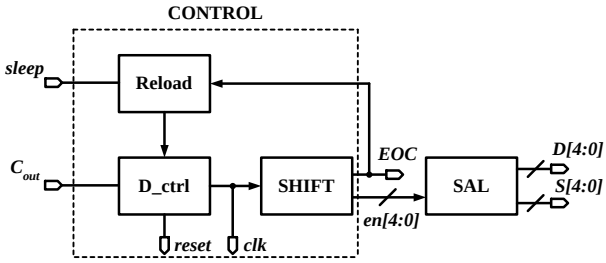

Figure 4: The block diagram of the CONTROL block and SAL block

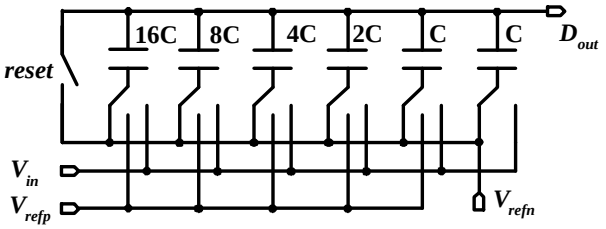

Figure 5: The schematic of the sample-and-subtract block

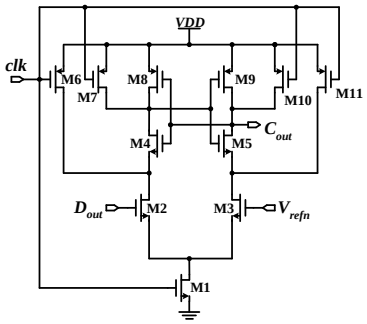

Figure 6: The schematic of the dynamic comparator

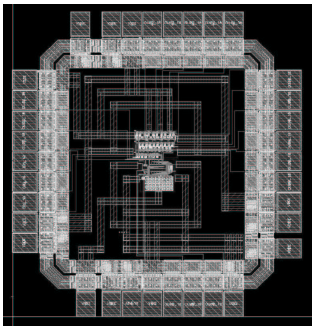

Figure 7: The layout of the proposed ADC

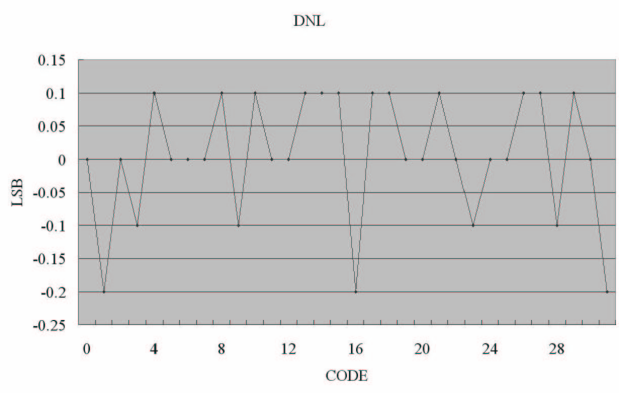

Figure 8: DNL

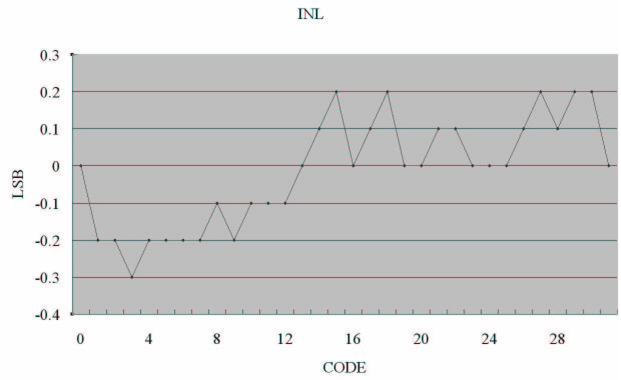

Figure 9: INL

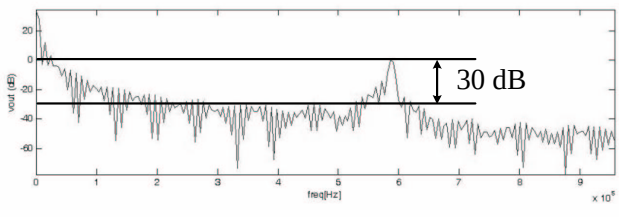

Figure 10: SFDR