10-bit 80 Msps ADC Using Closed-loop MDACs for DVB-T Receivers

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Abstract — The proposed ADC is the bridge connecting an AGC output and an OFDM demodulator. The ADC has four parallel channels. Each channel has nine 1.5-bit stages, one 2-bit flash ADC, and an error correction circuit. The ENOB is better than 9 bits. The INL is smaller than 2.8 LSB, and the DNL is smaller than 2.1 LSB. The power consumption is 432 mW at 80 MHz sample rate.

***Key Words* — DVB-T, ADC, MDAC**

I. INTRODUCTION

The main progress of TV broadcasting in these years is the transaction from NTSC TV broadcasting to Digital TV broadcasting, such as DVB, ATSC, HDTV etc. In Taiwan and Europe, DVB-T is the official standard for Digital TV broadcasting. The proposed ADC is designed for baseband mixed-signal processing of DVB-T receivers. The DVB-T receiver receives the TV signal by an antenna, and down-converts the signal by an RF frond-end. The ADC converts the down-converted TV signal into quantized digital signals sent to the OFDM demodulator in the baseband module. Certain DVB-T receivers down-convert the TV signal to 4.5 MHz by double down-conversion. Those designs need an extra mixer and an anti-aliasing filter. We choose another approach which only down-coverts the TV signal to 36 MHz [1]. Although this design needs a high resolution ADC, it saves the mixer and the anti-aliasing filter which are hard to be integrated in an SOC due to large passive elements.

Many ADC designs have been proposed in the literature. Primary ADC architectures are full flash, two step flash, folding, successive approximation, and pipeline. In order to satisfy the Nyquist rate, the sample frequency should be better than 72 MHz if the input frequency of the ADC is 36 MHz. In order to keep enough design margin, the ADC is designed to have a 80 MHz sample rate. The resolution of the ADC should be 8-10 bits [1]. The pipeline ADC architecture is a better option for DVB-T receivers regarding the power, area, and throughput trade off.

II. PARALLEL PIPELINE ADC

The operational amplifiers designed for high-speed high-resolution applications generally occupy large die area and consume large power. If the bandwidth of the operational amplifiers is reduced, both the die size and the power consumption are reduced, either. Hence, the parallel pipeline architecture [2] is chosen.

The proposed ADC is composed of four 10-bit 20 Msps ADC channels [3] as shown in Fig. 1. The clocks of the 10-bit 20 MHz pipeline ADC channels are $\phi_1 \sim \phi_4$, respectively. The CLK (80 MHz) is down-converted to four 20 MHz clocks ($\phi_1 \sim \phi_4$) by a four-phase clock circuit, which has two div2, one div2-dummy, and a multi-phase generator as shown in Fig. 2. The detailed circuits of div2 and div2-dummy are shown in Fig. 3. Two div2 circuits down-convert f_{CLK} to $\frac{1}{4} f_{CLK}$. The delay difference between the two inputs of the multi-phase generator are reduced by the div2-dummy. The glitches of $\phi_1 \sim \phi_4$ are reduced, too. The multi-phase generator detailed in Fig. 4 generates $\phi_1 \sim \phi_4$ with 90^o phase difference by two inverters and a XOR gate. The maximum jitter tolerance of the sampling clock is shown as Eqn. (1) [4].

$$\Delta Ts \le \frac{1}{2^N} \times \frac{1}{\pi \cdot fs} \tag{1}$$

where ΔTs is the jitter, N is the resolution, and fs is the sampling frequency. The maximum jitter tolerance in each channel must be less than 15.56 ps.

As shown in Fig. 5, a single 10-bit 20 Msps ADC channel contains a S/H circuit, nine 1.5-bit ADC stages, a 2-bit flash ADC, and an error correction circuit. The 1.5-bit ADC stages, S/H circuit, and error correction circuit are detailed as follows.

A. S/H circuit

The S/H circuit is based on a switch capacitor circuit as shown in Fig. 6. During the sample period, SW_S is ON, SW_f is OFF, and C_S is charged by V_{in}. During the hold period, SW_S is OFF, SW_f is ON, and the charge stored in C_S is transferred to C_f. Finally, V_{out} equals $V_{in} \times \frac{C_S}{C_f}$. Because each channel is operated at 20 Msps, the bandwidth of the S/H operational amplifier should be 120 MHz, which is six times of the sample rate of the single channel [8]. As shown in Eqn. (2), the DC gain of the operational amplifier must be better than 61.96 dB provided that the resolution of the ADC is 10-bit.

$$\begin{aligned} \text{SNR} &= 6.02 \times \text{resolution} + 1.76 \\ &= 6.02 \times 10 + 1.76 \\ &= 61.76 \end{aligned} \tag{2}$$

In order to satisfy the setup time of each stage in the pipeline ADC, the operational amplifiers should charge the capacitors (2 pF) in the S/H circuit from 1 V to 2 V in 10 ns. Hence, the slew rate should be at least 1 V/0.01 μs which is equal to 100 V/μs.

The characteristics of the operational amplifier, which are required for satisfying above design constraints and keeping design margins in each channel, are summarized in Table I.

B. 1.5-bit ADC stage

Each 1.5-bit ADC stage contains a 2-bit flash ADC and a multiplying digital to analog converter (MDAC) as shown in Fig. 7. The set of the 2-bit flash ADC output is {00, 01,10}. Since each stage is calibrated by its next stage, the ADC stage is named as 1.5-bit ADC stage. The offset errors and gain errors induced by the operational amplifiers and the switches are partially calibrated by the error correction circuit.

A traditional MDAC is shown in Fig. 8(a). During the sample period, the V_i from prior stage charges C_{M11} and C_{M12} in this stage. During the subtract period, V_{i+1} is decided by C_{M11}, C_{M12}, and D as shown in Eqn. (3).

$$V_{i+1} = (1+\frac{C_{M11}}{C_{M12}})\, V_i + D \times V_{ref}, \quad (3)$$

where D = -1, 0 or +1, when $\{SEL_1, SEL_0\}=\{11, 01,00\}$, respectively, as shown in Fig. 8. Let C_{M11} equal to C_{M12}, the relations among V_i , V_{i+1}, and D are tabulated in Table II. During the sample period, the operational amplifier has an open loop, but a closed loop during the subtract period. The voltage of the virtual ground during the sample period is different from the voltage during the subtract period. Hence, V_{i+1} is distorted so that the resolution is worsen. This problem is resolved by a modified MDAC is shown in Fig. 8(b). No matter in the sample period or the subtract period, the modified MDAC contains a closed loop. The virtual ground voltage is kept the same all the time.

C. Error correction circuit

Each output of the 1.5-bit ADC stage is stored by a D Flip-Flop as shown in Fig. 5. As soon as the 2-bit ADC at the last stage generates its outputs, the stored outputs of each stage are summed up as shown in Fig. 9. The error correction circuit reduces the distortions resulted from gain errors and offset errors.

III. Simulation & Implementation

A slow ramp signal is fed into the Analog IN while stimulating INL and DNL. The data from Digital OUT are analyzed by C programs. Fig. 10 is the simulation result of DNL. The maximum DNL is less than 2.1 LSB (least significant bit). Fig. 11 is the simulation result of INL. The maximum INL is less than 2.8 LSB. A 36 MHz signal is feed into the Analog IN while simulating SFDR. The data from Digital OUT are analyzed with DFT (discrete-time Fourier transform) by MATLAB. The spectrum performance of the SFDR result is found to be 56 dB is shown in Fig. 12. The ENOB is (SFDR-1.76)/6.02 which equals to 9.01 bits. The proposed ADC is implemented by TSMC 0.35 μm CMOS process. The die area of the proposed ADC is 3400×3100 μm^2 as shown in Fig. 13. The function of the proposed ADC is proved at PVT corners which are from 0^oC to 60^oC with 10 % VDD variations. The performance of the proposed ADC is tabulated in Table III. Table IV tabulates the performance of the proposed design with several prior ADCs. Compared with the performance of [5], which was designed for DVB-T receivers, the proposed ADC satisfy the demands of DVB-T receivers. The performance of [6] is obviously better than the other design because of using advanced 0.18 μm process. The proposed design consumes less power at the same operation frequency when compared with [7] given the same condition.

VI. Conclusion

This paper presents a 10-bit 80 Msps ADC for DVB-T receiver. The parallel pipeline architecture reduces the bandwidth requirement of the operational amplifiers. The power and the die size of the operational amplifiers are then effectively reduced. The distortion induced by the virtual ground variation is resolved by the modified MDAC circuit.

Acknowledgement

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Table I: The implementation characteristics of the operational amplifiers in the pipeline stages

Load capacitance	2 pF
Unity bandwidth	170 MHz
DC gain	68 dB
Phase margin	70^o
Slew rate	158 V/μs

Table II: The mapping among V_i, V_{i+1}, D, SEL_1, and SEL_0

V_i	V_{i+1}	D	SEL_1SEL_0
$V_i < -\frac{1}{4} V_{ref}$	$V_{i+1}=2 V_i + V_{ref}$	+1	00
$-\frac{1}{4} V_{ref} < V_i < -\frac{1}{4} V_{ref}$	$V_{i+1}=2 V_i$	0	01
$\frac{1}{4} V_{ref} < V_i$	$V_{i+1}=2 V_i - V_{ref}$	-1	11

Table III: The specification of the proposed ADC

Power consumption	432 mW @ 80 Msps
Die area	3400× 3100 μm^2
Power supply range	3.3 V ± 10 %
Temperature	0 ^oC ~ 60 ^oC
Max. operation frequency	80 MHz
INL	< 2.8 LSB
DNL	< 2.1 LSB
SFDR	56 dB
ENOB	9.01 bits

Table III: Performance comparisons

	[5]	[6]	[7]	ours
Sample frequency	25 MHz	80 MHz	25 MHz	80 MHz
Resolution	10 bits	10 bits	10 bits	10 bits
Process	0.35 μm	0.18μm	0.35 μm	0.35 μm
DNL	1.53 LSB	0.66 LSB	0.7 LSB	2.1 LSB
INL	3.03 LSB	0.76 LSB	1.1 LSB	2.8 LSB
ENOB	8.98 bits	9.1 bits	9 bits	9.01 bits
Supply voltage	2.8 V	1.8 V	3.3 V	3.3 V
Power consumption	27 mW	80 mW	195 mW	432 mW

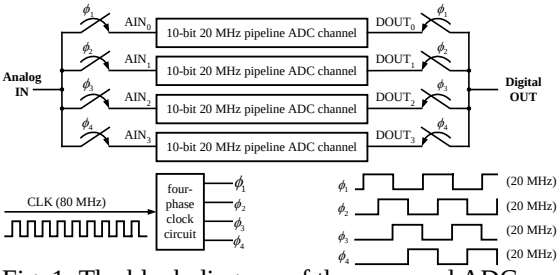


Fig. 1: The block diagram of the proposed ADC

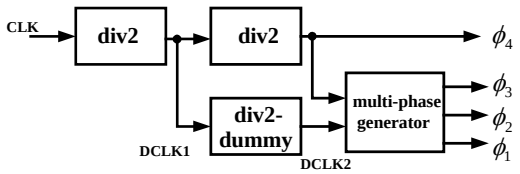


Fig. 2: four-phase clock circuit

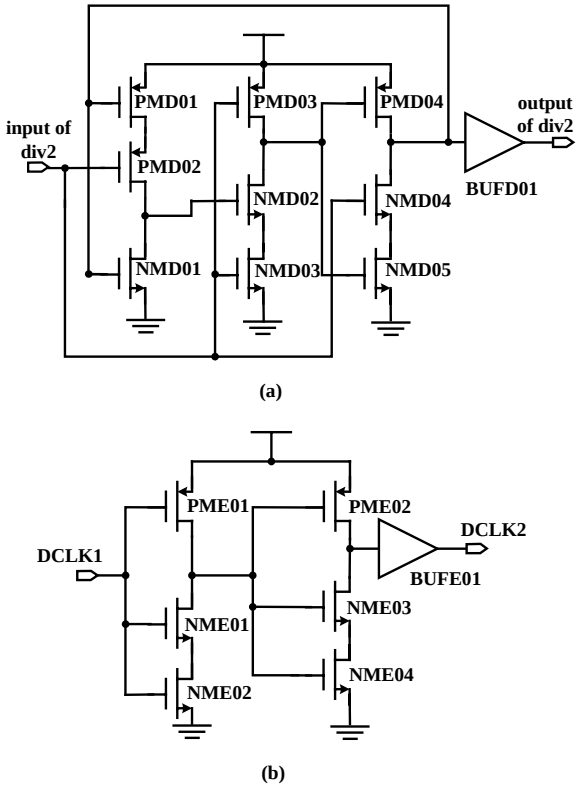


Fig. 3: (a) div2 circuit (b) div2-dummy circuit

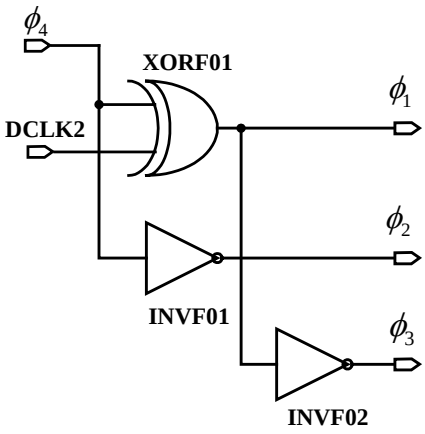


Fig. 4: multi-phase generator

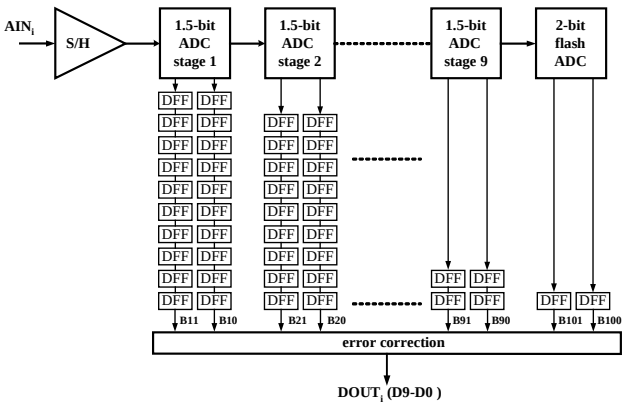


Fig. 5: The block diagram of a single ADC channel

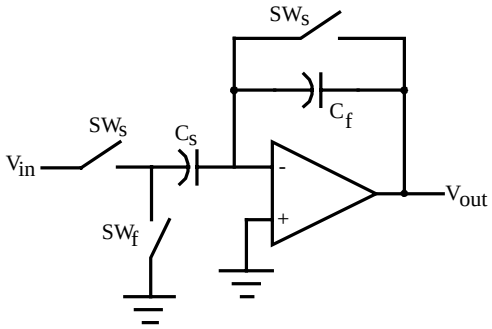


Fig. 6: S/H circuit

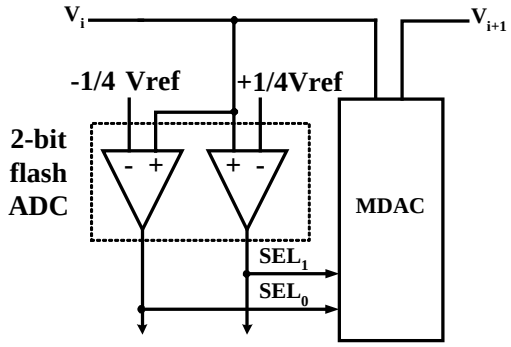
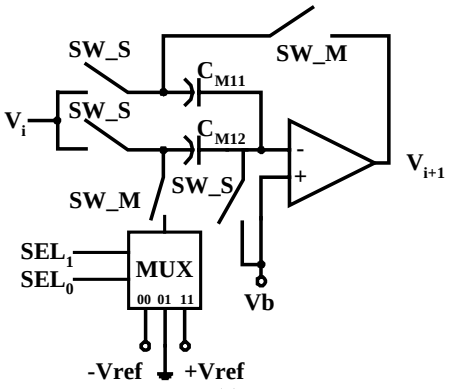
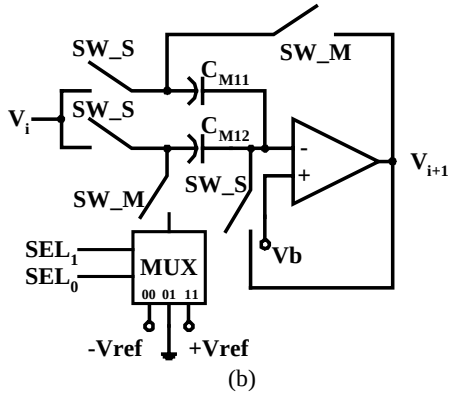


Fig. 7: 1.5-bit ADC stage



(a)



(b)

Fig.8: (a) Traditional MDAC (b) Modified MDAC

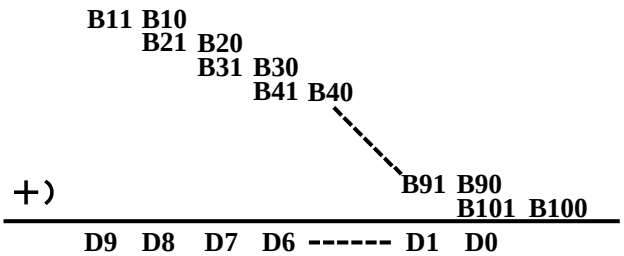


Fig. 9: error correction operation

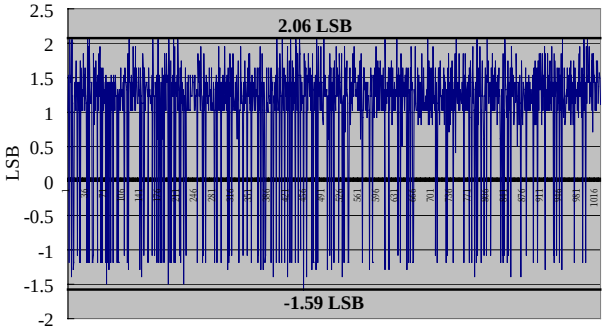


Fig. 10: DNL of the proposed ADC

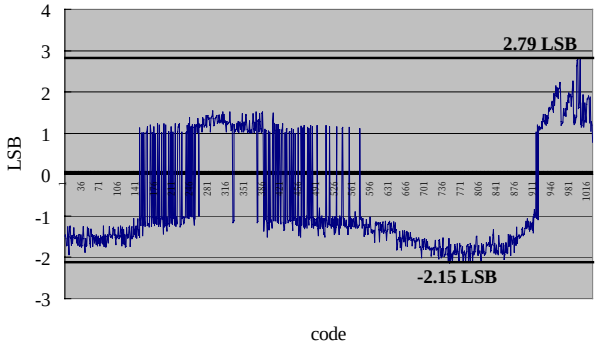


Fig. 11: INL of the proposed ADC

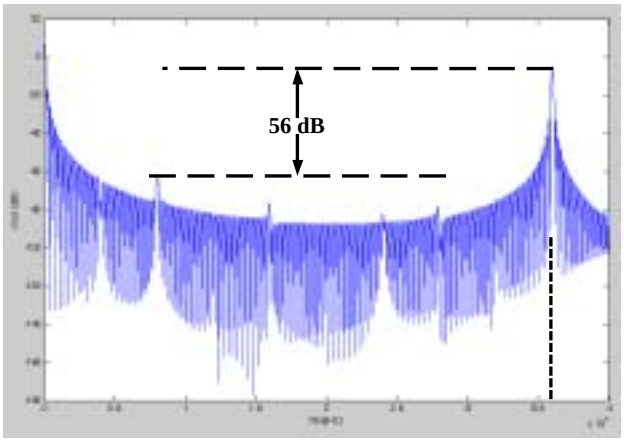


Fig. 12: SFDR of the proposed ADC

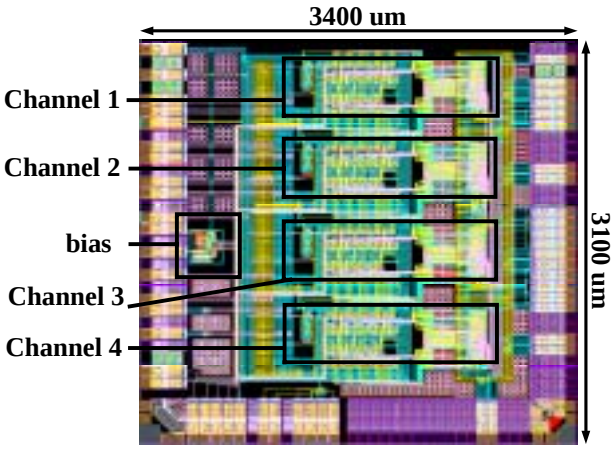


Fig. 13: Layout of the proposed ADC