LOW POWER CMOS OUTPUT CELL DESIGN WITH SPIKE FILTERING FOR BASEBAND DIGITAL SIGNAL PROCESSING[§]

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ABSTRACT

A novel power-saving and small-area digital output cell is proposed in this work. The new cell drastically reduces the output power consumption by filtering pre-defined spikes, which have been considered as one of the major power dissipation sources of the whole chip, with little sacrifice of speed or delay. The duration of the spikes to be removed can be pre-defined either dynamically by digital selection signals or permanently by fuses to be burned. The maximum operating clock is 200 MHz given a 10 pF off-chip load according to measurements on silicon. Not only the proposed design removes hostile spikes to baseband DSP modules, it also reduces unwanted power dissipation caused by the spikes.

Keywords : baseband DSP, spike filtering, delay cells, buffering, off-chip load

1. INTRODUCTION

A critical circuit in the digital transmission of chips via longs wires in a communication baseband DSP module on PCBs is the output cells which are responsible for voltage level shifting and load driving [5]. Any noisy spike might cause the output cells to drive the long wires which might cause false transmission and power waste. Buffer circuits are widely employed in the presence of large capacitive loads, e.g., the off-chip wires. Besides the typical tappered buffer design which is expected to drive the large load by a series of inverters within a reasonably optimal amount of delay [6], another serious issue for the output cell design is that the power consumption of these cells and buffers occupies a significant portion of entire power dissipation of the chip. Prior CMOS I/O cells utilized very large area to accommodate large driving transistors as well as large passive elements [2], [7]. The price to pay is the significant power dissipation. What worse is that random noisy voltage spikes, which could be either positive or negative, will turn on the current sink or the current source of an output cell, respectively, to waste more power. By contrast, most of the prior I/O cell researches regarding the removal of noisy spikes were focused on the protection of the input cells, e.g., ESD protection, [1], [3], [4], [5]. In this paper, we tend to propose a novel output cell design to resolve the dilemma. Spike filters are proposed to be inserted between the output driver and the core circuit including the tappered buffers such that the unwanted random noisy voltage spikes will be removed. The duration of the spikes to be filtered can be determined by digitally controlled switches or fuses. The proposed output cell is implemented by CMOS 0.35 μm 2P4M process. The power reduction is almost 28% up to 200 MHz data rate by measurement on silicon.

2. SPIKE-FILTERING OUTPUT CELL

A typical output cell with a predriver is shown in Fig. 1. The predriver, when enabled, supplies the gate drive to the driver composed of a pair of huge PMOS and NMOS transistors to steer a large current to or from the long wire. This traditional design can not directly be voltage scaled so as to achieve the power saving by $P = f \cdot C \cdot V^2$, where f is the switching frequency, C is the load, and V is the supplied voltage. The reason is obvious : if the supplied voltage of the driver is shifted form VDD to $\frac{1}{2}$VDD, the drain current of M11 becomes

$$I_D = \frac{\beta}{2}(V_{SG} + V_{thp})^2 \left[1 + \lambda(V_{SD} - V_{SD,sat})\right] \quad (1)$$

where V_{SG} is the voltage drop between the source and the gate of M11, V_{SD} is that between the source

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and the drain of M11. The decrease of V_{SD} caused by the shrinkage of the supplied voltage results in the decrease of I_D. Thus, the driving capability as well as the speed is deteriorated.

What worse is any noisy voltage spike appearing at the output of the predriver will cause the driver to be turned on. For instance, a negative voltage spike present at the gate drive of M11 turns on the current source to charge the capacitive load. The power loss caused by such a spike is $\frac{1}{2}C_{\text{load}}\text{VDD}^2$. Similarly, a positive spike turns on the M12 to cause the same amount of power loss.

2.1. Digital-controlled spike filters

The essence of noisy spikes is mainly high frequency signals. Hence, low pass filters composed of delay buffers are considered to remove these unwanted high frequency spikes. Meanwhile, positive noisy spikes only turns on the pull down MOS of the output driver, while negative ones turns on the pull up MOS. Thus, we need two separate filters to be inserted between the output driver and the predriver. Fig. 2 shows the architecture of the proposed output cell.

Positive Spike Filter (PSF) : The details of the PSF in Fig. 2 is revealed in Fig. 3. Each delay cell is responsible for a unit delay, say 1 ns. Digital selection signals, D1, D2, ..., Dn, determine the status of pass-transistor-based switches, $PS_1, \ldots, PS_n$, respectively. For instance, if 3 of the n switches are opened, all of the spikes with duration less than 3 ns will be filtered.

Negative Spike Filter (NSF) : By contrast, the schematic of the NSF is given in Fig. 4. The only difference of NSF from PSF is that the AND gate is replaced with an OR gate.

2.2. Fuse-based spike filters

It is well known that the MOS-based switches possess on-resistance as well as parasitic capacitance, which might distort the signals fed into the gate drive of the output buffer. An alternative to avoid such a problem is to replace all of the switches with fuses. Hence, the schematics of the PSF and the NSF become those shown in Fig. 5. The advantage of the fuse switches is low resistance and small capacitance. However, the price to pay is the loss of flexibility once if some of the fuses are burned.

3. SIMULATION AND IMPLEMENTATION

The proposed output cell is implemented by TSMC 0.35 μm 2P4M CMOS technology to verify the performance. Notably, all of the process corners : [0^oC, $+75^o$C], (SS, SF, TT, FS, FF) models, and VDD$\pm$10%, are simulated.

Periodic Spikes Simulation : Fig. 6 is a 200 MHz testing data with noisy spikes. The spike duration set to be removed is 450 ps. The post-layout simulation results of the proposed design are given in Fig. 7 showing that all of the unwanted noisy spikes are filtered at all of the PVT corners.

Random Spikes Simulation : By using the random number generator functions provided by HSPICE S/W, a series of random pulses shown in Fig. 8 is used as the testing data. Fig. 9 and Fig. 10 are the simulation results of traditional output cell and the proposed design with a predefined 450 ps duration filter setting. All of the pre-defined noisy spikes are fully filtered.

We also run a series of Monte Carlo simulation by HSPICE to attain the power reduction performance compared the proposed design with the traditional output cell without spike filtering. The number of sweeps is 30. Fig. 11 shows that the average power reduction between 1 MHz to 200 MHz data rate is almost 28% given coupled periodic high-frequency ($\geq$ 200 MHz) noise spikes. Meanwhile, in the same figure, the average power reduction is shown to be 6% given 10 MHz testing data with a low-frequency 4 MHz bandwidth random noise. Fig. 12 shows the die photo of the proposed design, while Fig. 13 is the waveform of the measurement on silicon. Notably, all of the noisy spikes are removed. Table 1 summarizes the characteristics of the proposed output cell.

4. CONCLUSION

We propose a novel output cell taking advantage of noise spike filters to reduce unwanted power dissipation. Two alternatives to define the duration of the spike duration are revealed. The sacrifice in terms of delay is proved to be obscure. Thorough post-layout simulations and measurement on silicon justify the superiority of our design.

5. REFERENCES

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VDD	3.3±10%
max. power	140 mW@200 MHz
die area	1.31×1.31 mm^2
core cell area	119.5×305 μm^2
(including SF and driver)	
temp. range	0∼75^{o}C
max. data rate	200 MHz
max. C_{load}	10 pF
V_{IH}	> +0.8 V
V_{IL}	< -0.8 V

Table 1: characteristics of the proposed output cell

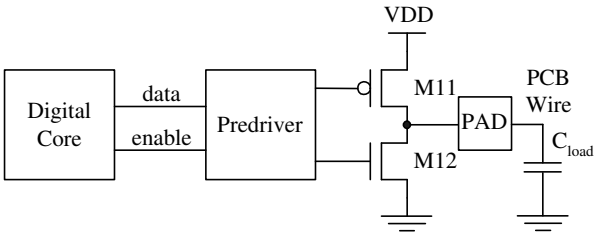

Figure 1: Traditional I/O cells

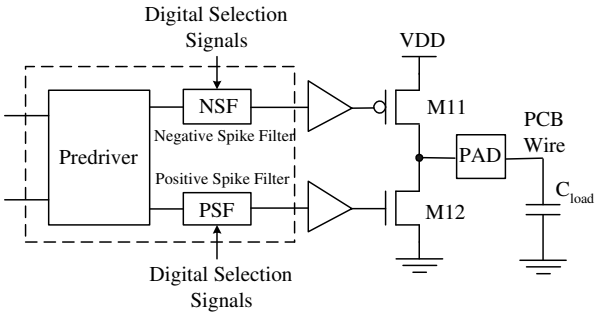

Figure 2: Trasmitter of the proposed I/O cell

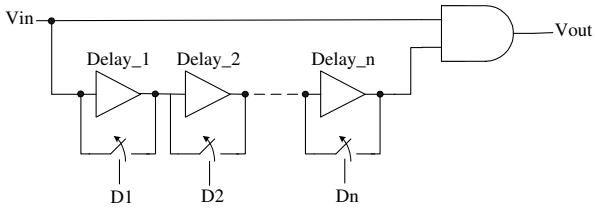

Figure 3: Positive spike filter (PSF)

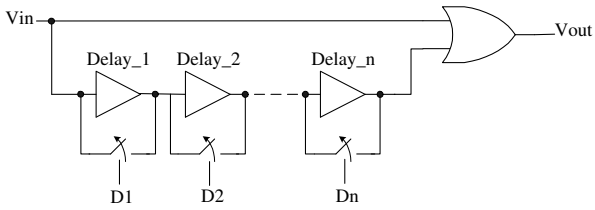

Figure 4: Negative spike filter (NSF)

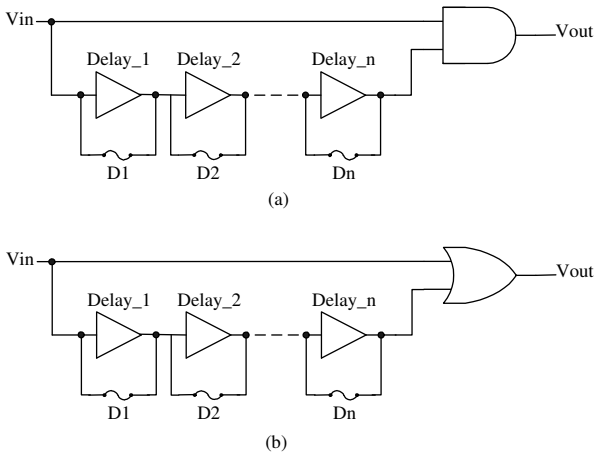

Figure 5: Fuse-based NSF and PSF

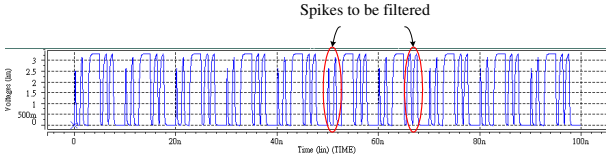

Figure 6: Test signal with periodic spikes

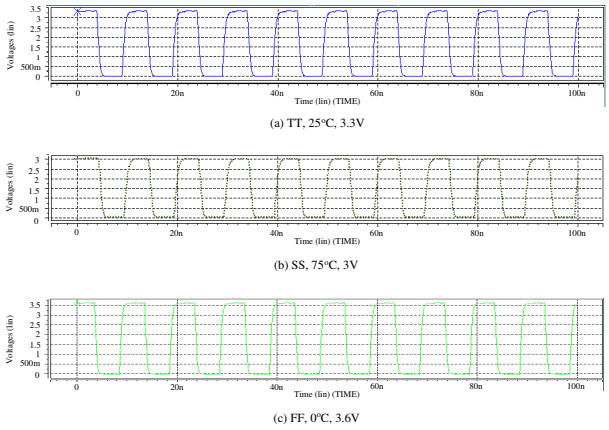

Figure 7: Simulation waveforms given different PVT conditions

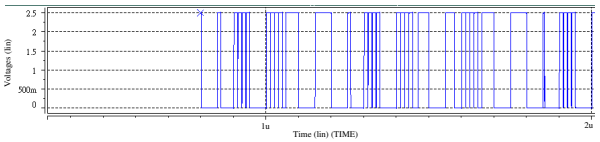

Figure 8: Test signal with random spikes

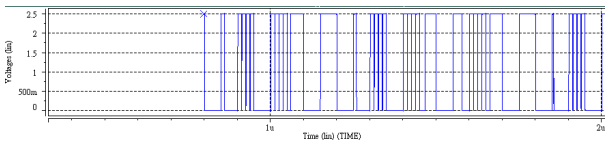

Figure 9: Simulation waveforms of the traditional output cells

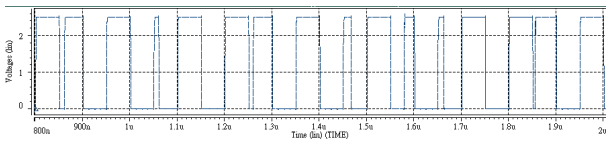

Figure 10: Simulation waveforms of the proposed output cells

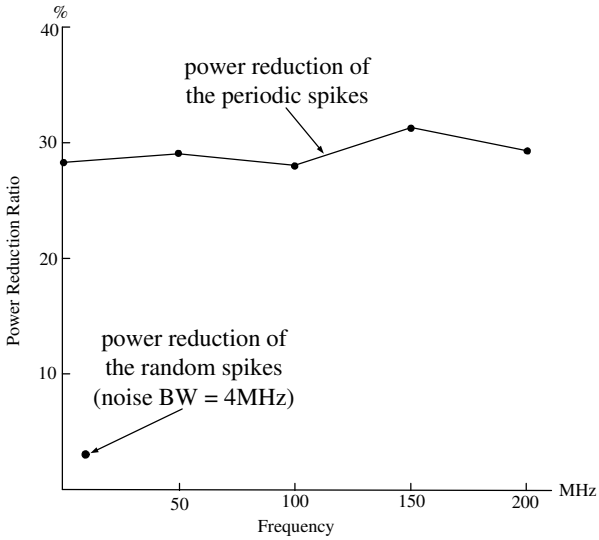

Figure 11: Average power reduction ratio

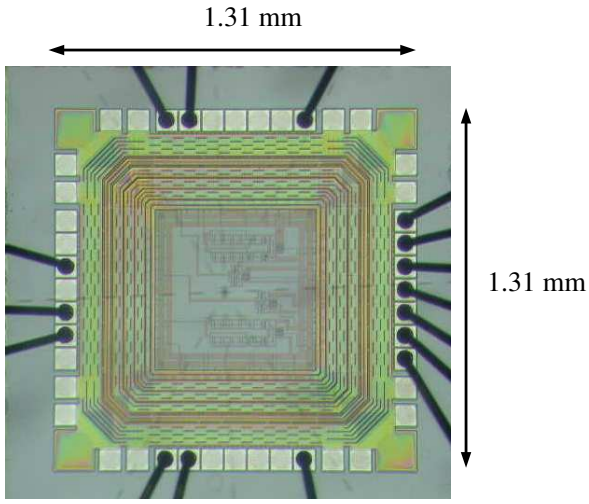

Figure 12: Die photo of the test chip

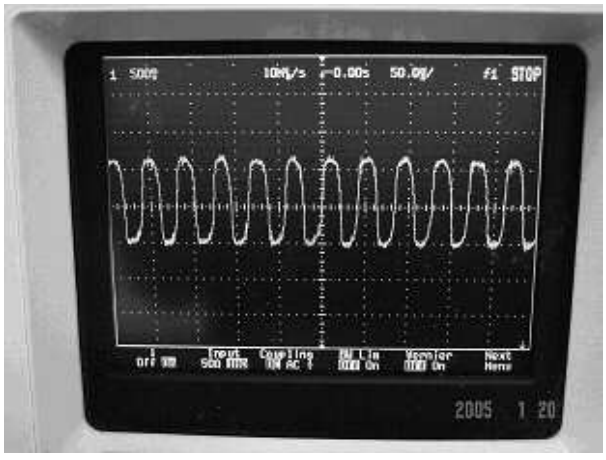

Figure 13: Measurement of the test chip O/P