DUAL-OPA COIL DRIVER FOR HEAT DISSIPATION OF SOC'S[§]

Chua-Chin Wang† , Senior Member, IEEE, Tzung-Je Lee, and Kuan-Wen Fang

Department of Electrical Engineering
National Sun Yat-Sen University
Kaohsiung, Taiwan 80424
email : ccwang@ee.nsysu.edu.tw

ABSTRACT

A coil driver consisting of dual operational amplifiers (OPAs) implemented on a chip for driving heat-sinking fans or micro motors is presented in this paper. The two OPAs employ the modified class AB push-pull output stage to generate an output current which lags the output voltage by 90^o when an inductive load is to be driven. This design is implemented by using a 1P6M 0.18μm CMOS process. Moreover, the isolation technique for pnp type BJT is utilized such that this circuit is able to be integrated in an SOC (system-on-a-chip) or SOP (system-on-a-package). Therefore, the direct control of a heat-sinking fan or motor can be directly driven by the SOC itself without using any extra circuitry or chip. The simulation result verifies that the proposed circuit works correctly at all PVT corners. The worst output current is found to be 20.9 mA at the corner, [VDD = 2.97 V, temp. = 0^oC, SS model].

Keywords : coil driver, SOC, class AB, push-pull, motor, heat-sinking

1 Introduction

Due to the rapid advancing of modern technology, motors become basic devices in a variety of common applications, especially for the heat-sink fans or micro motors. Massive number of discrete elements are required on a PCB to drive the motors or fans to resolve the heat problem, e.g., power BJT, MOS, and large passive R, C elements. Not only they consume a great portion of power, they also occupy a very large area on the PCB. With the development of sub-micro technologies and SOC, we tend to explore the feasibility of driving the heat-sinking fans by the SOC itself. In order to drive these fans or micro-motors, we need a coil driver implemented on the SOC to supply the required current for the equivalent inductive load. Lots of piror works, which utilized the big sized BJT to provide large output currents, can not be easily integrated to drive the micro motors on silicon. Thus, we design the dual OPAs for the coil driver to be used in SOC designs. Besides, the output amplifiers of the coil driver in a lot of prior researches were based on the class AB push-pull complementary output stage, [1], [2], [3], [4], which could not generate the output current and output voltage which are 90^o out of phase at the presence of an inductive load. Hence, we utilize a modified output stage in the dual OPAs to resolve this difficulty [6].

[§] This research was partially supported by National Science Council under grant NHRI-EX93-9319EI and NSC 92-2218-E-110-001.

†the contact author.

2 The Coil Driver for SOCs

The basic requirement of the coil driver for SOC is using two modified OPAs with a switching class AB push-pull complementary output stage, which produces the output current having 90^o out of phase with the output voltage for the inductive load. The second requirement is the magnitude of the output current should be at least in the range of 10 $\sim$ 100 mA to drive a fan like [7].

2.1 Traditional OPA

Fig. 1 shows the traditional OPA with the class AB push-pull complementary output stage [5]. The diode D13, the resistor R11, and the transistor Q14 constitute a current source to bias transistors Q11 and Q13 in the class AB output stage. A composite pnp Darlington pair is composed of Q11 and Q12, as shown in Fig. 2, which turns into a push-pull output stage with transistor Q13. The two diodes, D11 and D12, are used to supply the required base-emitter voltage and emitter-base voltage for the transistor Q13 and the pnp Darlington pair comprising Q11 and Q12, respectively.

When the OPA operates in the negative feedback configuration with an inductive load, the input signal V_{ip1} is amplified by the differential input stage to drive the emitter follower, Q15, such that the voltages V_{a1} and V_{b1} are in phase with V_{ip1} and V_{out1}. Therefore, Q13 is turned on at the positive half-cycle of V_{out1}. However, the output current would change its direction from I_{OB1} to I_{OA1} in this half-cycle resulting in I_{OB1} to pass through Q11 and Q12 which are turned off if an inductive load is connected, as in the phase A in Fig. 3. Similarly, I_{OA1} would flow through Q13 while Q13 is off because V_{out1} is in its negative half-cycle, as in the phase C shown in Fig. 3. The exact 90^o phase lag between the output voltage and the output current is not feasible by this circuit.

2.2 The coil driver

In order to resolve this problem, we present a coil driver which would change the current direction appropreiately for the inductive load. Referring to Fig. 4, the coil driver is composed of two negative feedback operational amplifiers OPA3 and OPA4 which possess a modified push-pull output stage. The input signals, V_{a3} and V_{b3}, where V_{b3} is the inversion of V_{a3}, are applied to the positive nodes of OPA3 and OPA4, respectively. The negative nodes of OPA3 and OPA4 receive a reference voltage via the negative feedback resistor networks composed of R33∼R36. V_{REF} is fed into these two resistor networks to provide the required reference voltage. A control signal V_{c3}, which determines whether the positive half cycle (V_{c3}=1) or the negative half cycle (V_{c3}=0) of V_{a3} is served, is fed into OPA3 and OPA4 to control switches in OPA3 and OPA4. Thus, OPA3 and OPA4 work in a complementary manner and generate the output currents, I_{OA3} and I_{OD3}, or I_{OB3} and I_{OC3}, respectively. Notably, the inductive load L is connected between V_{op3} and V_{on3}.

2.3 The modified OPAs

Fig. 5 shows the schematic of OPA3 and OPA4 in Fig. 4. We adopt the OPA using a modified push-pull output stage for an inductive load [6]. Referring to Fig. 5, Q41-Q44 and I_{dc4} constitute an input differential stage. The emitter follower Q45 and the common-emitter amplifier Q46 are used to generate a signal V_{a2} with an appropriate DC voltage level and a voltage swing range for the push-pull pair Q24 and Q25. The two switches S1 and S2, and the transistors Q21, Q22, QD21, and QD22, constitue the first switching circuit to change the output current direction when the output signal is in its positive half cycle. Moreover, QD21, and QD22 are treated as the diodes with a turn-on voltage equal to the emitter-base forward voltages of Q21, and Q22, respectively. On the other hand, transistors Q23 and QD23, and the switch S3 form the second switching circuit which operates during negative half cycle.

The OPA operates in four modes in respective four phases in Fig. 3, to supply different combinations of output voltage and current to the inductive load. The operation is described as follows:

Phase A : When the output voltage is at the positive half cycle, S1 and S2 are turned on by the signal V_{c3} such that the first switching circuit is in action. The signal V_{a2} is designed to turn on the transistor Q22 resulting in Q25 to be turned on when V_{a2} is smaller than V_{b2}. Thus, the output current I_{OB2} is generated.

Phase B : Once the signal V_{a2} is higher than the voltage V_{b2} which is $V_{out2} + |V_{BE}|$, the first switching circuit is turned off. Simutaneously, Q24 is turned on because V_{a2} is larger than $V_{out2} + |V_{BE}|$. Thus, the output current I_{OA2} is generated.

Phase C : If the output volatge is at its negative half cycle, S1 and S2 are turned off and S3 is turned on by the control signal V_{c3}. Therefore, the second switching circuit is active and the first switching circuit is deactivated. Initially, Q24 is still turned on because V_{a2} is large enough to maintain the output current I_{OA2}.

Phase D : When V_{out2} reaches its negative peak value, the signal V_{a2} drops such that Q24 is off and the current through QD23 is decreased. It results in that the current I_{dc3} is applied to the base current of the transistor Q23. Then, the Darlington pair is turned on and the output current change to be I_{OB2}.

The above operation ensures that there is a 90^o phase difference between the output voltage and the output current which is adequate to drive an inductive load.

3 Implementation and Simulation

To apply to SOC applications and facilitate the reduction of the cost as well as the area, this circuit is implemented by using TSMC 0.18 μm 1P6M CMOS process. However, because only two models of BJT are available in the mentioned process, the design becomes very difficult to carry out on silicon. Moreover, the collector of the pnp type BJT in the CMOS process would be connected to the P-substrate inherently such that it is not so straight forward to be integrated, as shown in Fig. 6. However, the deep NWELL (DNW) is available in the mentioned process. Thus, we propose to utilize NWELL and DNW to isolate the collector of pnp type BJT and the P-substrate ground, as shown in Fig. 7, to resolve the integration problem.

The layout of the proposed design is shown in Fig. 8 and the core area is 1074.2 × 1341.5 μm^2. A 2 KHz input signal are applied to V_{a3} and the load inductor is set to be 1.5 mH to reduce the simulation time. Referring to simulation results in Fig. 9, the output voltage V_{op3} leads 90^o phase to I_{o3}. Moreover, V_{op3}, V_{on3} and V_{a3} vary between 0.894 V and 1.735 V because R33∼R36 are chosen to be the same. Besides, I_{o3} is from -48.8 mA to 48.8 mA which is adequate to drive the fan like [7]. The output current I_{o3} has at lowest 20.9 mA amplitude at the worst case of [VDD=2.97 V, temp,=0°C, SS model], as shown in Fig. 10. The specifications of this design are summarized in Table 1.

4 Conclusion

We have presented dual OPAs for a coil driver to drive micro motors in this paper. This design is implemented by using TSMC 0.18 μm 1P6M CMOS process and the isolation techique for the inegration of pnp type BJT such that it is able to be feasible for SOC designs. This circuit is verified by using HSPICE simulator at all PVT corners. The output current is simulated to be 20.9 mA in the worst case.

References

[1] Rohm Co. Ltd., "6CH power driver for CD-ROM, DVD-ROM," Data Sheet: BD7902CFS.

[2] Allegro, "Dual full-bridge motor driver," Data Sheet: 2916, 1994.

[3] A. Ruha, T. Ruotsalainen, J.-P. Tervaluoto, and J. Kauppinen, "Electronic circuit for a switching power

amplifier and method for switching the output stage of a switching power amplifier," United States Patent No. 6819177, Nov. 16, 2004.

[4] J. Bales, "A low-power, high-speed, current-feedback, op-amp with a novel class AB high current output stage," *Inter. J. of Solid-State Circuits*, vol. 32, no. 9, pp. 1470-1474, Sept. 1997.

[5] P. R. Gray, and R. G. Meyer, *Analysis and design of analog integrated circuits,* Published by John Wiley & Sons, Feb. 2001.

[6] Rohm Co. Ltd., "Coil load driving circuit." Taiwan Patent No. 336310, July 1998.

[7] SUNON, "KDE0502PEV3-8." Data Sheet: Sunon DC Fan & Blower, 2004.

Output voltage	$0.894 \sim 1.735$ V
Output current	> 20.9 mA
Inductive load	1.5 mH
Power consumption	< 190.8 mW @ [3.63 V, 50^oC, FF] $I_{o3} = 61.3mA$

Table 1: Specifications of the proposed coil driver.

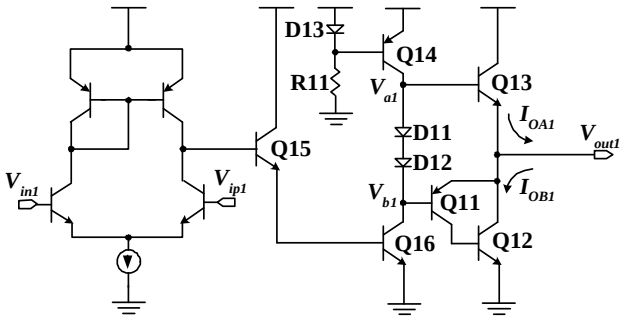

Figure 1: OPA with traditional class-AB push-pull output stage.

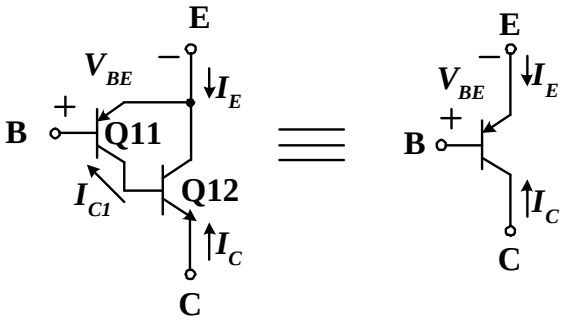

Figure 2: The Darlington pair and its equvalent pnp transistor.

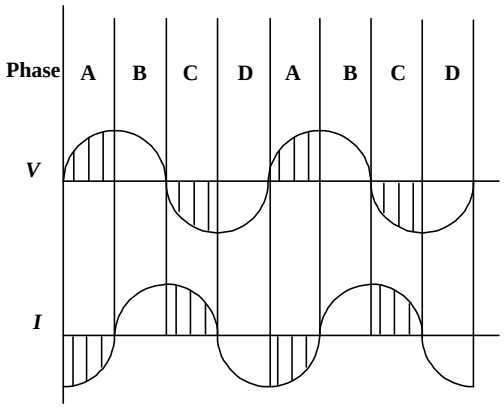

Figure 3: Voltage and the associated current for the inductive load.

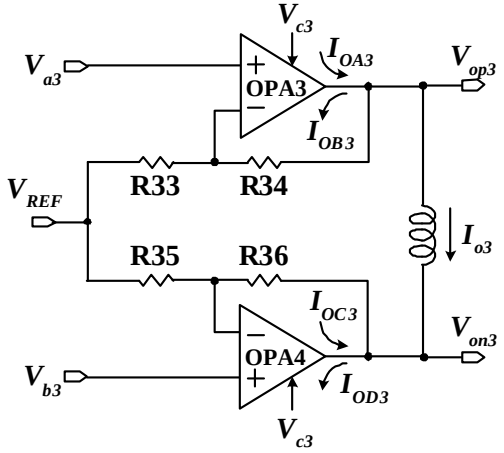

Figure 4: Schematic of the coil driver.

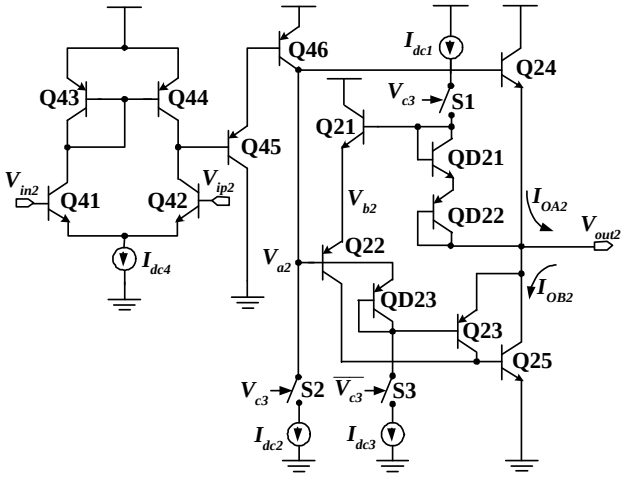

Figure 5: The modified OPA.

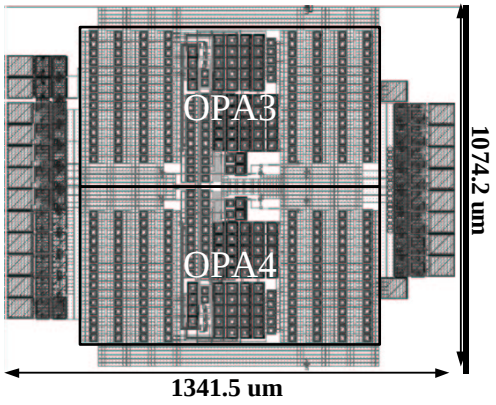

Figure 8: Layout of the proposed design.

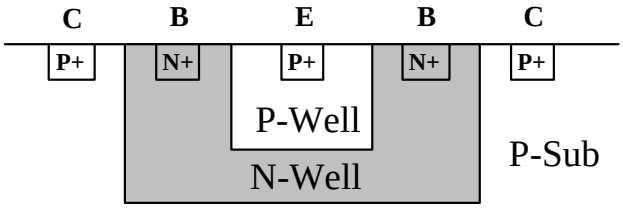

Figure 6: Cross-section view of original pnp type BJT.

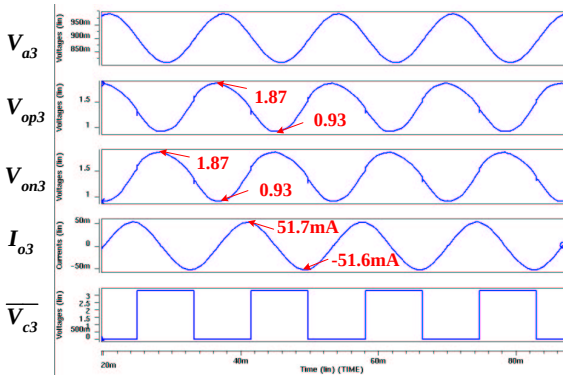

Figure 9: Simulation of V_{a3}, V_{op3}, V_{on3}, I_{o3}, and V_{c3}.

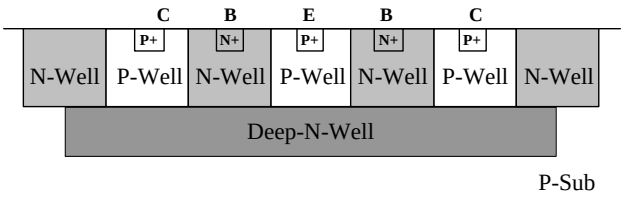

Figure 7: Cross-section view of the isolated pnp type BJT.

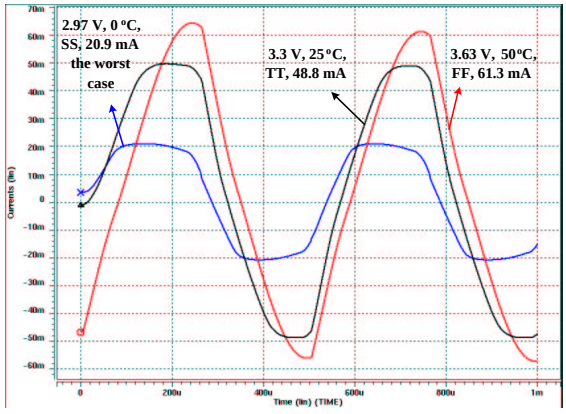

Figure 10: The output current I_{o3} in the worst PVT corner.