LOW-POWER BUS DRIVER DESIGN BASED ON A CHARGE RECYCLE TECHNIQUE[§]

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ABSTRACT

This paper presents a differential low swing bus driver based on a charge recycle technique. The differential low swing signaling has long been adopted to achieve low power and robust data transmission, while the charge recycle technique has been widely utilized to reduce the power consumption. We, thus, propose to recycle the charges on the long lines for differential low swing signaling, e.g., LVDS, to reduce the power dissipation. The simulation results have shown that the reduction of 13.6% power consumption and 43% power-delay product is achieved, as compared with these circuits without using the charge recycle technique.

1 Introduction

As the growing demand for portable and hand-held devices, power consumption of bus and bus drivers becomes a critical issue in the low power design since the bus involves long interconnections with large fan-out and passive parasitics. The power consumption mainly results from charging and discharging of large capacitive loads. Most of the prior low power driver design were based on two different techniques, low swing signaling and charge recycling.

The driver circuits based on the reduce swing signaling reduce the signal swing on the loads to reduce the power consumption [1], [2], [3]. What benefits from the low swing signaling is not only the reduced power but also the the gain of the speed. To ensure the signal integrity over the buses in the applications of extreme low swing, the differential solutions [4], [5], [6] are more attractive than single-ended counterpart, even though they come with the penalty of duplicated power. We enhance the differential scheme in the proposed design with the charge recycle technique to further reduce the power dissipation .

The charge recycle technique is based on the concept of reusing the discharging current. The discharging charge is stored during the discharging phase. In the next charging phase, the load is charged by the stored charge instead of the power supply. According to [7], the power saving is achieved by using a large capacitor tank to gather the charge, which is assumed to be dumped by the load in the discharging phase. This scheme is impractical to be implemented since the significant power saving comes from the large capacitor tank. [8] and [9] proposed similar schemes, but both of them were using conventional full swing drivers. [10] proposed a novel charge recycling bus by cascading several low swing drivers. One capacitor is needed between every two drivers. The stored charge of the upper driver became the power supply of the lower driver. This scheme needs extra capacitors and voltage level guard circuits to keep capacitors in a proper voltage level.

Although the differential scheme is more immune to noise, it suffers from the duplicated power consumption compared to the single-ended scheme. In this paper, we present a low power bus driver design, which combines differential low swing signaling with the charge recycle technique, to achieve a robust and low power data transmission.

2 Recycling Technique of Differential Signaling

2.1 Differential low swing circuit

The differential low swing driver circuit is presented in Fig. 1. M0, M1, M2, and M3, M4, M5 are two NMOS-only push-pull pairs. To clarify the circuit operation, symbols "0" and "1" denote logical low high levels, respectively, while V_{low} and V_{high} denote low swing low high levels, respectively. Assume that in a stable state where IN = "0", while OUT_1 =

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V_{low} and $OUT_2 = V_{high}$. M0 is on, and M3 is off in this stable state.

Case 1 When the input IN goes high, M1 will be turned on, and then load capacitance C_1 is charged by V_{dd}. When C_1 is charged to V_{high}, the output of the inverter INV1 goes to "0" and make M0 turn off. Therefore, OUT_1 remains at V_{high}. On the other hand, M5 is turned on when IN goes high, and C_2 is discharged to make $OUT_2 = V_{low}$.

Case 2 When the input IN goes low, M1 will be turned off, and M2 is turned off. The load capacitance C_1 is discharged to ground via M2. On the other hand, M4 is turned on, and C_2 is charged by the power supply until the voltage level of OUT_2 reaches V_{high}.

Given that $V_{dd} = 1.8$ V, V_{high} is around 0.5 V and V_{low} is 0 V. In order to make inverters INV1 and INV2 in the Fig. 1 switch at V_{high}, the medium threshold voltage NMOS is used. The schematic and transfer curve of the INV1 and INV2 are shown in Fig. 2 and Fig. 3, respectively.

2.2 Drivers with charge recycling

Fig. 4 shows the schematic of the proposed differential low swing driver circuit with charge recycling technique. During the "1" to "0" transition of the input signal, M8 is turned on temporarily such that the charge in C_1 is redistributed between C_1 and C_2. Hence, part of the charge form C_1 is reused to charge C_2. During the "0" to "1" transition, both the M6 and M7 would be turned on for a transience due to the propagation delay of the inverter such that the charge in C_2 is redistributed between C_1 and C_2.

2.3 Power saving analysis

Regarding the power saving attained from the the charge recycle technique, we first consider the power dissipated by the driver circuit without adopting the charge recycle technique, which is shown in Eqn. (1).

$$P_{load} = V_{dd} \cdot V_s \cdot (C_1 + C_2) \cdot f, \quad (1)$$

where V_{dd} is the supply voltage, f is input signal frequency, and V_s is the voltage swing on the load capacitance C_1 and C_2 ($V_s = V_{high}$ - V_{low}).

As for the circuit based on the charge recycle technique in Fig. 4, the differential outputs are coupled via the pass transistors. During the signal transition, the pass transistors are turned on temporarily to proceed charge sharing, which makes a significant ratio of the stored charge reused, where the ratio is determined by the load capacitances. The power dissipation of the circuit in Fig. 4 can be represented as follows :

$$\begin{aligned} P_i &= V_{dd} \cdot C_i \cdot (V_s - \frac{C_j}{C_i + C_j} \cdot V_s) \cdot f \\ &= V_{dd} \cdot V_s (\frac{{C_i}^2}{C_i + C_j}) \cdot f, \end{aligned} \quad (2)$$

where C_i and C_j are the charging capacitance and the discharging capacitance ineach cycle, respectively. That is, C_i and C_j could be C_1 and C_2 or vice versa. Then, the power saving of the driver circuit based on the charge recycle technique is as follows :

$$\text{power saving ratio} = 1 - \frac{P_1 + P_2}{P_{load}} = \frac{2C_1C_2}{(C_1 + C_2)^2} \quad (3)$$

When $C_1 = C_2$, the theoretic maximum of the power saving is 50%. Such a figure is impossible to achieve due to the additional power dissipation consumed by the additional control circuitry, e.g., those pass transistors.

3 Simulation Results

In order to evaluate the performance of the proposed design, simulations were carried out by TSMC 0.18 μm 1P6M CMOS technology with a nominal supply voltage 1.8 V. All of the process corner : [0°C, +100°C], (SS, TT, FF) models, and V_{dd}±10%, are simulated. The proposed differential low swing driver based on the charge recycle (Fig. 4) is compared with the original driver without charge recycle (Fig. 1).

Fig. 5 demonstrates the comparison of the power consumption. It shows the driver based on the charge recycle technique consumes less power than the original driver. Fig. 6 shows the percentage of the power saving where the maximum is 13.6% at load = 3 pF. Fig. 7 shows the average delay of the both drivers. Fig. 8 depicts the power-delay product, which shows the superior performance of the driver based on the charge recycle technique. Fig. 9 shows the improvement of power-delay product, where the maximum is 43% when the load capacitance is 2.7 pF.

4 Conclusion

We have proposed a differential low swing driver based on the charge recycle technique. The maximum power saving is up to 13.6% and the maximum improvement of the power-delay product is up to 43%. Simulation results manifests the charge recycle technique can dramatically improve the differential low swing signaling by reducing both the delay time and the power consumption.

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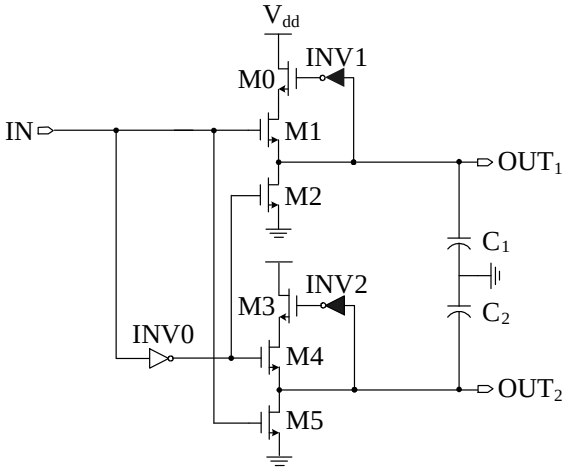

Figure 1: Differential low swing driver

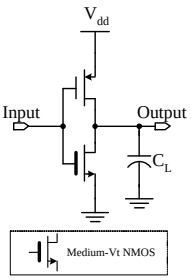

Figure 2: Schematic of the inverter INV1 and INV2

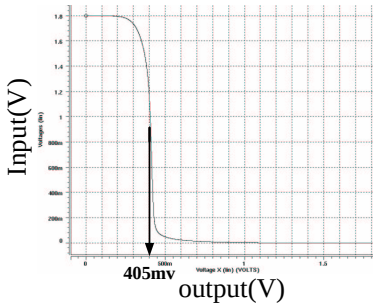

Figure 3: Transfer curve of the inverter INV1 and INV2

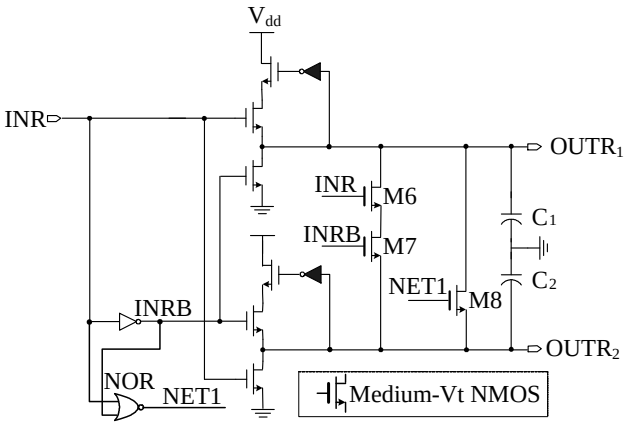

Figure 4: Proposed differential low swing driver based on charge recycle technique

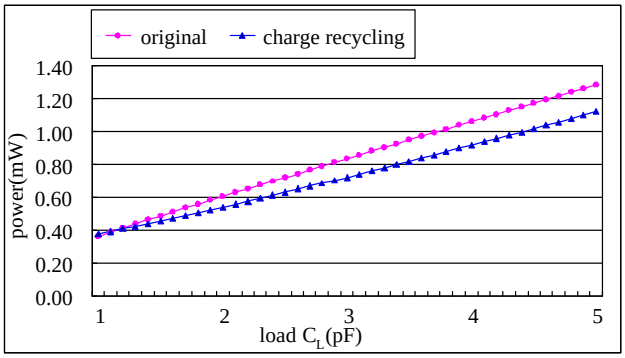

Figure 5: Comparison of the power consumption

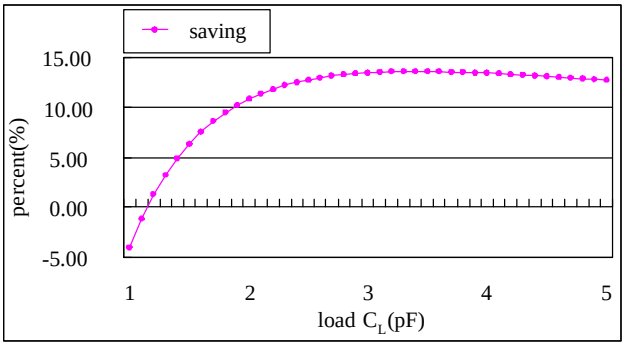

Figure 6: Power saving ratio

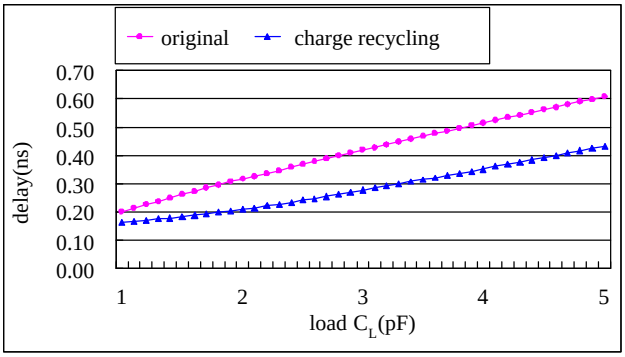

Figure 7: Comparison of the delay

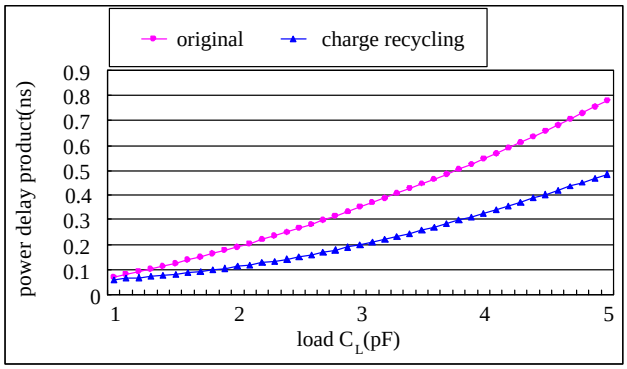

Figure 8: Comparison of the power delay product

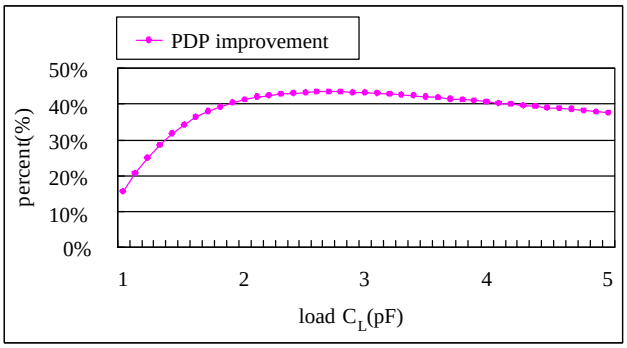

Figure 9: Improvement of the power-delay product