Wideband 70dB CMOS Digital Variable Gain Amplifier Design for DVB-T Receiver's AGC[§]

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***Abstract*— This paper presents a novel VGA (variable gain amplifier) design which is applied in the AGC (automatic gain control) loop of DVB-T receivers. A total of three tunable gain stages are cascaded to provide a 70 dB dynamic range. Each gain stage is based on a DVGA (digital variable gain amplifier) which is composed of a plurality of GBs (gain block) and a fully differential degeneration amplifier (FDDA). The GBs are digitally controlled current mirrors which are used to determine the gain of the DVGA. A CMFB (common-mode feedback) circuitry is used to stabilize the FDDA. The bandwidth of the proposed design verified by HSPICE post-layout simulations is better than 95 MHz at every PVT corner which is sufficient for the DVB-T IF mixed-signal processing.**

I. Introduction

The AGC (automatic gain control) plays critical roles in many applications, e.g., hearing aids, hard disk drives, and particularly portable communication systems. As long as a receiver is required in a wireless system, the signal strength will likely depend on the distance between the receiver and the transmitter which will cause the processing difficulty of the following signal processing units in the receiver [1]. The task of the AGC loop is to adjust the gain depending on the receiving path automatically such that the strength of the signal collected by the signal processing units in baseband modules appear to be close to a constant level no matter what the distance between the receiver and the transmitter is. It is particularly critical in the wireless DVB-T receiver to ensure the correctness of the OFDM demodulation therein. Notably, DVB-T has been deemed as one of the most outstanding standards for the next-generation digital TV [2], [3]. The AGC is responsible for the stable signal level for the following ADC (analog-to-digital converter) as well as the OFDM demodulator. Hence, two important requirements for the AGC in the DVB-T receivers besides the gain step are decibel linearity and the bandwidth. Besides, one long ignored problem in the design of AGC is the peaky current overshoot occurring at the change of the gain, which in turn causes power waste and hazards. A novel digital VGA based on a g_m-boosting DVGA (digital VGA) is proposed in this work. A current-selecting gain control approach is also presented to suppress the overshoot when the gain is adjusted. The proposed digital VGA which is implemented by 0.35 μm 2P4M CMOS technology possesses 70 dB dynamic tuning range with a 0.3 dB gain error and 95 MHz bandwidth.

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II. Wideband Digital VGA Design

If AGC designs are classified by feedback signals provided by baseband DSP units, there are two types : analog-controlled loop and digital-controlled loop, as shown in Fig. 1. Notably, the former needs a DAC to convert the digital feedback signals from the DSP into analog signals. Hence, the digital-controlled loop obviously has the edge. However, the digital VGA in the prior digital-controlled loop-based AGCs encounters different design problems. CDN (current division network) proposed in [1] possesses low bandwidth ($\leq$ 18 MHz). By contrast, though the DDP (degeneration differential pair) approach in [4] resolved the bandwidth difficulty, it requires a lot of resistors to attain the gain-tuning effect which in turn consumes large chip area and produces thermal noise problems.

A. VGA in the AGC Loop

Since it is highly difficult to use a single VGA to realize a very wide dynamic range of gain tuning, we propose to utilize 3 stages of individual DVGAs to attain the required 70 dB range, wide bandwidth, and decibel linearity. As shown in Fig. 2, the range of the first DVGA is 0 to 30 dB with a 10-dB gain step; the second stage is aimed at 0 to 10 dB range with a 2-dB gain step; and the last stage is -30 to 0 dB with a 10-dB gain step. The ratio of the range to the gain step in each stage determines the number of gain blocks required therein. Meanwhile, the gain block which will be disclosed later is composed of digital-controlled current source and switches. If the number of gain blocks in a single VGA is increased, the decibel linearity will be likely to be decreased. After detailed simulations, a ratio of 3 to 5 is a better option to determine the number of gain blocks in each stage.

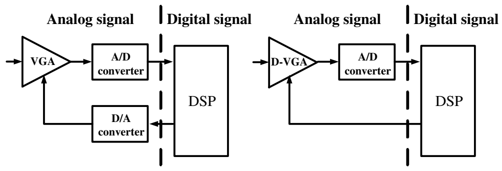

Fig. 1. Two types of AGC loops

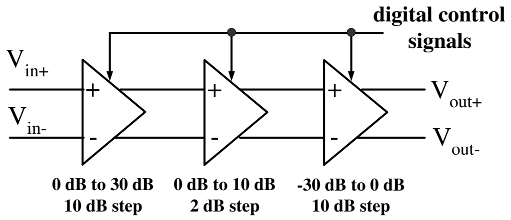

Fig. 2. Architecture of the proposed DVGA

B. Schematic of DVGA

Referring to Fig. 3, the schematic of the proposed DVGA is revealed, where V_{in+} and V_{in-} are differential inputs, V_{o+} and V_{o-} are a pair of differential outputs, and D_i and $\overline{\mathrm{D}}_i$, $i = 1 \ldots N$, are digital control signals. The input stage of the DVGA is a fully differential degeneration amplifier. The gain blocks controlled by D_i and $\overline{\mathrm{D}}_i$, $i = 1 \ldots N$, are used to change the summation currents, I_{o+} and I_{o-}, such that the overall gain can be adjusted by the digital signals. Besides, a CMFB (common mode feedback) is employed to stabilize the common-mode voltage of the amplifier.

1) Gain analysis: Fig. 4 is the simplified schematic of the FDDA. The transconductance and the gain of the amplifier is summarized as follows.

$$g_{m\text{diff}} = \frac{g_{m_1}}{1 + g_{m_1} \cdot \frac{R_d}{2}}, \tag{1}$$

$$A_v = \frac{R_L}{\frac{R_d}{2} + \frac{1}{g_{m_1}}}, \tag{2}$$

where g_{m_1} is the transconductance of M_01 and M_02. Obviously, the voltage gain is increased with g_{m_1}. It implies that a g_m-boosting circuit will be helpful in this regard. Hence, a g_m-boosting circuit in Fig. 5 is proposed to increase the gain. The boosted transconductance is derived to be $g_m = g_{m_1} \cdot (1 + g_{m_3} R_{AL})$, where g_{m_3} is the transconductance of M_03, and R_{AL} is the equivalent impedance looking into the current sink, I_b. The overall fully differential degeneration amplifier with the g_m-boosting circuit is given in Fig. 6. Thus, the gain is enhanced to be

$$A_v = F \cdot \frac{R_L}{\frac{R_d}{2}}, \tag{3}$$

where F is the current ratio of I_7 to I_3.

2) Gain tuning control: According to Eqn. (3), the gain can be adjusted by two parameters : the resistance ratio and

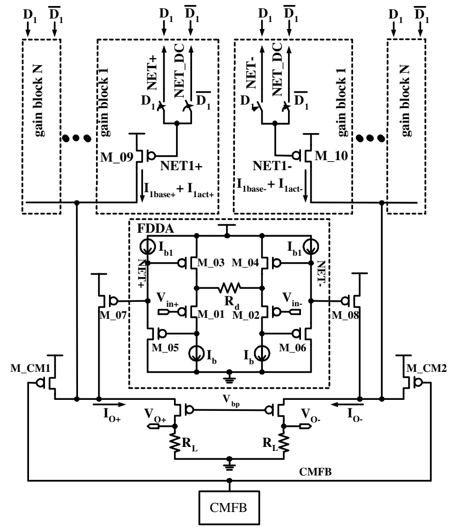

Fig. 3. Proposed DVGA with current selecting

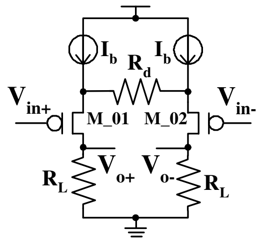

Fig. 4. Simplified schematic of the DVGA

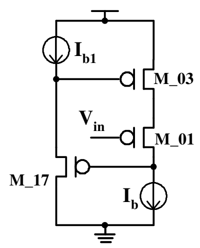

Fig. 5. g_m-boosting circuit

the current mirror gain. However, since the resistors will cause large chip area consumption and unwanted thermal heat problem, we tend to use the variation of current mirror gain to achieve the gain tuning function. In other words, different current sources in the gain blocks as shown in Fig. 3 provide a variety of current ratio compared to I_3. The digital control signals, D_i and $\overline{\mathrm{D}}_i$, $i = 1 \ldots N$, are used to determine the ON/OFF of the current source in each gain block such that the overall gain can be adjusted.

However, owing to the fact that $V_o = I_o \cdot R_L$, where V_o is V_{o+} or V_{o-}, I_o is I_{o+} or I_{o-}, a current spike is generated when the states of MOS-based switches in gain blocks are flipped provided that the gain adjustment is proceeded. An example is illustrated in Fig. 7. Such an overshoot might

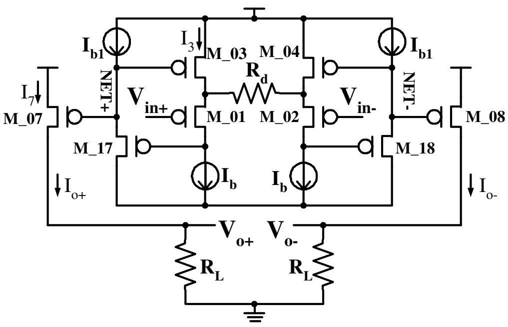

Fig. 6. Fully differential degeneration amplifier with the g_m-boosting circuit

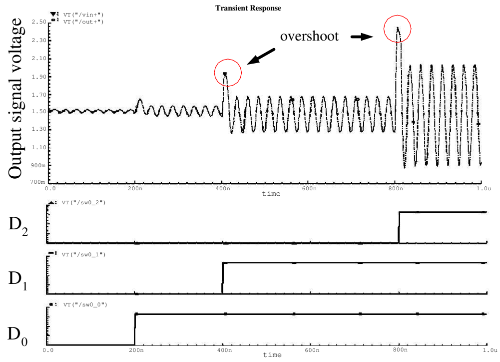

Fig. 7. Overshoot syndrome at the gain tuning

cause gain error besides power waste. Hence, we propose to divide the generated current in each gain block into two partitions : I_{base} and I_{act}. The corresponding gate drives to generate the I_{base} and I_{act} are V_{base} and V_{act}, respectively. If a gain block is not chosen, the gate drive is switched to V_{base} such that a smaller I_{base} is fed to the output current. By contrast, when it is selected, the gate drive is switched to V_{act} such that a bigger I_{act} is supplied. In short, every gain block will supply its own I_{base} regardless of being activated. Fig. 8 shows the cancellation of the overshoot by this modification.

3) CMFB: A CMFB is required to stabilize the common mode voltage of the fully differential degeneration amplifier. The average of I_{o+} and I_{o-} is mirrored to input of the CMFB in Fig. 9, where V_{oCM} denotes the common mode voltage. Thus, the following derivation can be concluded.

$$\begin{aligned} I_{o+} + I_{o-} &= [\frac{V_{oCM}}{R_L} + i_{act+}] + [\frac{V_{oCM}}{R_L} - i_{act-}] \\ &= 2 \cdot \frac{V_{oCM}}{R_L} \\ \frac{I_{o+} + I_{o-}}{2} &= \frac{V_{oCM}}{R_L}, \end{aligned} \tag{4}$$

where i_{act+} and i_{act-} represents the total current supplied by all of the gain blocks. Then, by the feedback loop in Fig. 9, the V_{ref} can be determined.

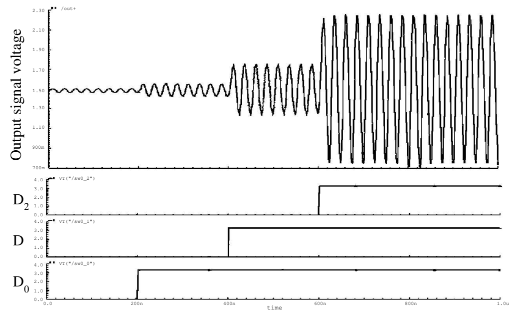

Fig. 8. Cancellation of overshoot

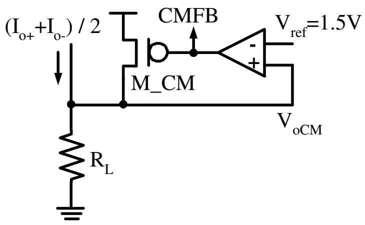

Fig. 9. CMFB circuitry

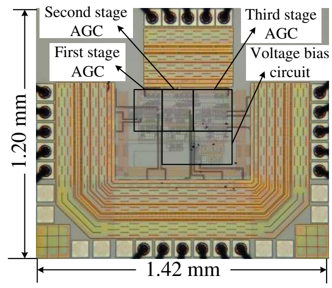

Fig. 10. Die photo of the proposed design

$$V_{oCM} = \left(\frac{I_{o+} + I_{o-}}{2} + I_{CM} \right) \cdot R_L = V_{\text{ref}}, \tag{5}$$

where I_{CM} is the current via PMOS M_CM. By mirroring the I_{CM} to the branches of M_CM1 and M_CM2 in Fig. 3, the common voltage is fixed to be V_{ref}.

Undoubfully, the V_{ref} plays a critical role in the success of the entire design. We utilize a step-down regulator to reject the noise coupled in power supplies to a bandgap bias.

III. Simulation and Implementation

TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 2P4M CMOS process was adopted to carry out the proposed design. Fig. 10 shows the die photo of the proposed design. The worst-case (FF model, VDD = 3.63 V, 0^{o}C) post-layout simulations of the bandwidth and the gain error are revealed, respectively, in Fig. 11 and Fig. 12, given all of the PVT corners. The maximum dynamic gain range at $f_{3\text{ dB}}$ = 95 MHz is [-30, +40] dB. The gain

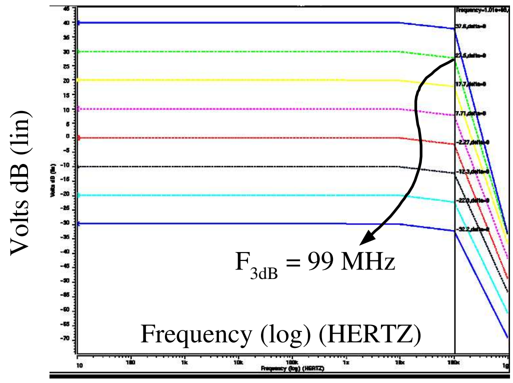

Fig. 11. Gain response by post-layout simulations

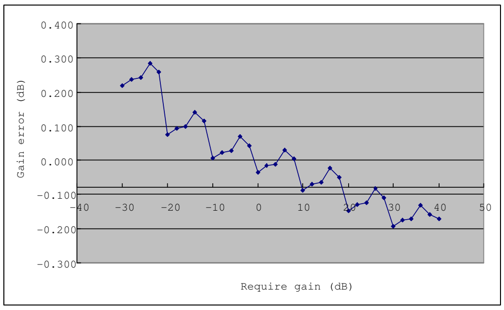

Fig. 12. Gain error by post-layout simulations

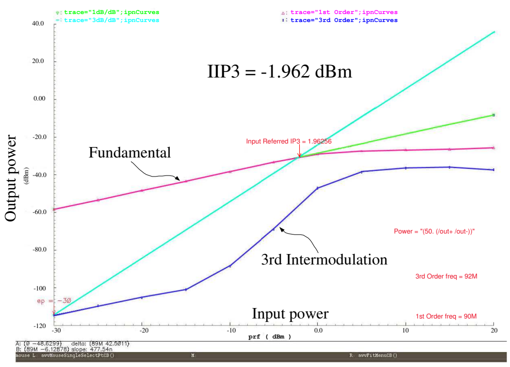

Fig. 13. IIP3 plot

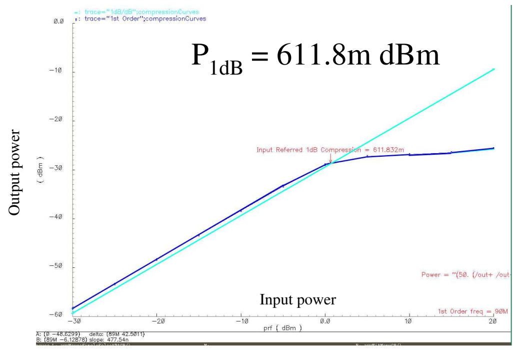

Fig. 14. P_{1dB} plot

TABLE I

CHARACTERISTICS OF THE PROPOSED DESIGN

Bandwidth	95 MHz
Dynamic range	70 dB
Gain step	2 dB
Gain accuracy	< 0.3 dB
IIP3	-1.962 dBm
P1dB	0.611 dBm
Power	32.7 mW@95 MHz
Core area	0.65×0.44 mm^2
Die area	1.42×1.20 mm^2

TABLE II

COMPARISON WITH PRIOR DESIGNS

	[4]	[1]	ours
CMOS Process	0.6 μm	1.2 μm	0.35 μm
Max. Freq.	110 MHz	18 MHz	95 MHz
Dynamic range	70 dB	60 dB	70 dB
Gain step	2 dB	0.55 dB	2 dB
Gain error	0.3 dB	0.5 dB	0.3 dB
# of Res.	$O(n)$	$O(1)$	$O(1)$
Overshoot	large	small	small

error is no more than 0.3 dB. The IIP3 and P_{1dB} plots are shown in Fig. 13 and Fig. 14, respectively to justify the decibel linearity of the proposed design. The overall design characteristics of the proposed DVGA are tabulated in Table I. Meanwhile, the comparison of the proposed design with several prior designs is summarized in Table II. It is obvious that the proposed design preserves the wide bandwidth with small area and gain transition overshoot.

IV. CONCLUSION

We have proposed a novel digital AGC based on a DVGA (digital variable gain amplifier) composed of a plurality of GBs (gain block) and a fully differential degeneration amplifier. The gain tuning required by DVB-T receivers can be carried out by digital signals selecting proper GBs. The post-layout simulations justify the advantages of the proposed design in terms of small area, small overshoot without any loss of bandwidth, gain step and gain error. Besides, the decibel linearity is also verified.

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