AN 80 MHZ PLL CHIP WITH SUPPLY NOISE REJECTION USING SEPARATE REGULATORS[§]

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Abstrate–**An 80MHz PLL using separate regulators to reject the supply noise is presented in this paper. The jitter of the proposed PLL is proven on silicon to be less sensitive to the supply noise. The separate regulators are designed according to the proper selection of the frequency bandwidth for the regulators. The proposed PLL is fabricated using TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 2P4M CMOS process. The consideration of the regulator's bandwidth selection is discussed. Simulation results and physical measurements are matched. The p2p jitter is measured to be 174 ps when the PLL is operating at 80 MHz.**

I. INTRODUCTION

Most mixed-signal circuits need a PLL to generate a stable clock for ADC, DAC or digital circuits. The jitter of the PLL is considered as a critical factor for the correct data transformation in these applications. Many prior efforts to discuss the reasons as well as the rejection methods of the PLL jitter have been announced, [1], [7], [8]. The main source causing the PLL jitter is the supply noise and the substrate noise [1]. Several prior works proposed a variety of methods to reduce the supply noise in order to suppress the jitter. The most widely used method for reducing the PLL jitter is to employ a differential voltage controlled oscillator (VCO) with good noise rejection. Thus, Maneatis proposed the self-biased techniques to achieve a low jitter, and fixed damping factor PLL [7]. However, this method can not alleviate the problem of coupling the power supply noise directly to the VCO output node through parasitics. Other approaches attemping to isolate the VCO from the noisy power supply were also proposed. For instance, Kim's charge pump boosting technique suggested to leave a headroom for supply noise rejection [8]. An extra clock, however, is needed in Kim's method such that the power consumption increases and new noise sources appear. We propose to use separate regulated power supplies for the charge pump and the VCO, respectively, in this paper. The physical measurements on silicon verifies that the p2p jitter is merely 174 ps which is far less than that of the prior works.

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II. PLL USING SEPARATE REGULATORS

Since the charge pump (CP) is also a supply-noise-sensitive component in the PLL architecture, the noise rejection for the charge pump is also important for any low jitter PLL design. If a single regulator is used for CP and VCO, the area cost of the regulator will be very severe due to the stability demand of CP. Hence, we propose a two-regulator strategy (REG1 and REG2) for CP and VCO, respectively, as shown in Fig. 1. Besides, because the loop filter (LF) composed of RS, CS, and CP is an LPF (low-pass filter), the supply noise over the PLL bandwidth coupling to CP will be filtered [2]. On the contrary, the high-frequency supply noise coupling to VCO which is not filtered by LF will cause the PLL unlocked. Thus, we use the separarte regulators, an HPF (high-pass filter) -based REG1 and an LPF-based REG2, to isolate the supply noise from the CP and VCO, respectively.

Submodules of the proposed PLL

Regulators (REG1, REG2): To reduce the supply noise, the bandgap bias must be insensitive to the supply voltage. Referring to Fig. 2, the output voltage $VBGAP$ of the bandgap bias is indenpendent to VDD based on the following equation.

$$VBGAP = V_{EB,PQ101} + (V_T \ln n)(1 + \frac{R101}{R102}), \quad (1)$$

where $V_{EB,PQ101}$ is the emitter-base voltage of PQ101, V_T is the thermal voltage, and n is the emitter area ratio of PQ101 to PQ102. As mentioned in the previous section, REG1 and REG2 should reduce the low-frequency and high-frequency noise, respectively. The HPF-based regulator REG1, as shown in Fig. 3, is basically a step-down regulator. By contrast, the LPF-based REG2 is given in Fig. 4. Notably, the MOS resistor PM401 and the MOS capacitor NM401 are used to replace traditional R-C LPF configuration to reduce the area overhead.

PFD: The deadzone is the most important parameter in PFD due to that it is the major source of the PLL phase error. The deadzone introduces the phase jitter when the control voltage is, VCTRL, within the deadzone. A lot of different PFDs have been proposed to resolve the problem of long delay, limited operationg frequency, or long deadzone, [6], [3]. The most extensive PFDs are the dynamic PFDs which attain the advantages of high speed and zero deadzone. The PFD shown in Fig. 5 is used in the proposed PLL. The node EXT and INT refer to the signal CLK_IN and CLK_OUT, respectively. The two-stage structure carries out the precharge function such that high speed is achieved. The feedback control signal for PM602 and NM601 for UP (similarly, PM605 and NM605 for DN) makes the zero deadzone possible. Moreover, the drawback of a short-circuit current from VDD to GND is eliminated because PM602 and NM601 for UP (similarly, PM605 and NM605 for DN) do not turn on at the same time [3].

CP: REG1 is in charge of the noise rejection for CP. Besides, the switching speed of CP is another important source for the PLL jitter. Thus, a switch is placed in the source of the mirrored MOS transistors for the speed considration in Fig. 6 [4], where PM801 (NM803) is the switch of current, PM803 (NM801) is the mirrored current source, PM802 and PM806 (NM802 and NM806) are for the charge injection reduction, PM804 and NM804 (PM805 and NM805) consist of a dummy delay element for eliminating the skew of the control signal, and UPB and DNB are the inversions of UP and DN, respectively. Notably, the output current of the bias generator for CP shown in Fig. 7 is independent of the supply voltage.

VCO: The current-starved inverters are the basic cells for VCO design [5]. The serious problem of supply noise coupling in the current-starved VCO is resolved by REG2. Besides, the output buffer is added to maintain the gain of VCO when the large capacitive load is present.

III. SIMULATION AND MEASUREMENT

TSMC 0.35 μm 2P4M CMOS process is adopted to carry out the proposed PLL design. The die photo of the proposed LDO regulator is shown in Fig. 11 where the core area is 705 μm $\times$ 732 μm. The total area including the PADs is 1.118 mm $\times$ 1.462 mm. In order to guarantee the functionality of the power regulators addressed in section 2, the guard ring to reject the substrate noise from PLL to regulators must be added between the REG1, REG2 and the PLL.

The simulation is based on HSPICE simulator. Fig. 9 shows the post-layout simulation of pick-to-pick jitter as 174.83 ps in the worst case (FF, 25^{o}C, 3.3). The measurement environment of the PLL chip is built on a PCB board. The quartz oscillator for the reference clock is HO-12B of HOSONIC ELECTRONIC CO., LTD. The power supplier is GW GPC-3030D. Agilent Infiniium Oscilloscope, 600 MHz, 4GSa/s is employed in recording the PLL jitter of the chip. The measured jitter is 173.543 ps when PLL operates at 80 MHz as shown in Fig. 10. The rise time and fall time are 3.1142 ns and 2.7747 ns, respectively. The equivalent load capacitance of the probe is 8 pF. Obviously, the measurement meets what the simulation expected. A performance comparison of the proposed design on chip with several prior PLLs are summarized in Table 1. Our design indeed possessses the edge of low jitter.

IV. CONCLUSION

We have proposed a PLL with two regulators to isolate the supply noise for CP and VCO, respectively. The proposed PLL is implemented on TSMC 0.35 μm 2P4M CMOS process. The measurement results reveal that PLL jitter is 173.543 ps operating at 80 MHz and justify that the design works correctly.

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	ours	Maneat's[7]	Kim's[8]
CMOS process	0.35 μm	0.5μm	0.8 μm
P2P jitter	174 ps	262 ps	270 ps
chip area (mm^2)	1.63	1.18	N/A
max. freq.	80 MHz	400 MHz	592 MHz

Table 1: Summarized performance of the proposed PLL.

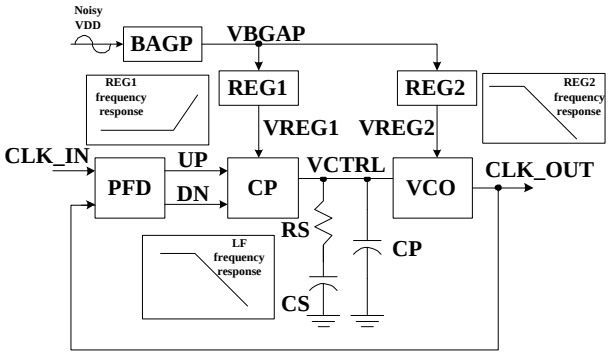

Fig. 1: The block diagram of the proposed PLL.

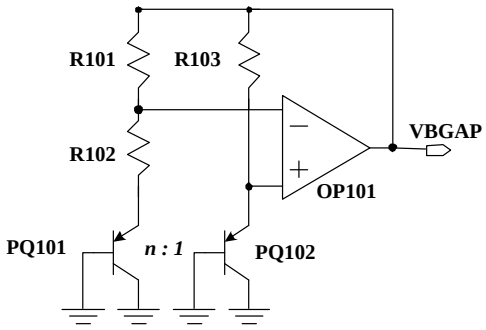

Fig. 2: The bandgap bias.

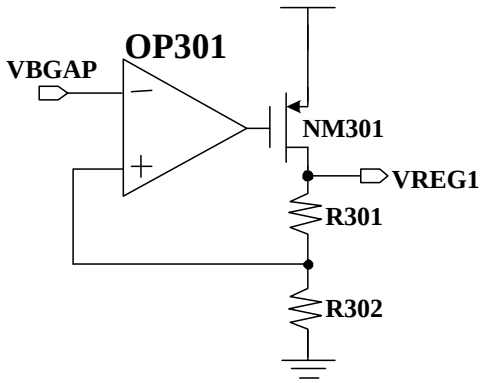

Fig. 3: Schematic of REG1.

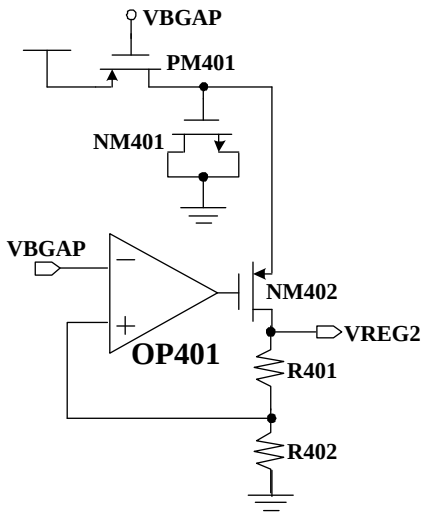

Fig. 4: Schematic of REG2.

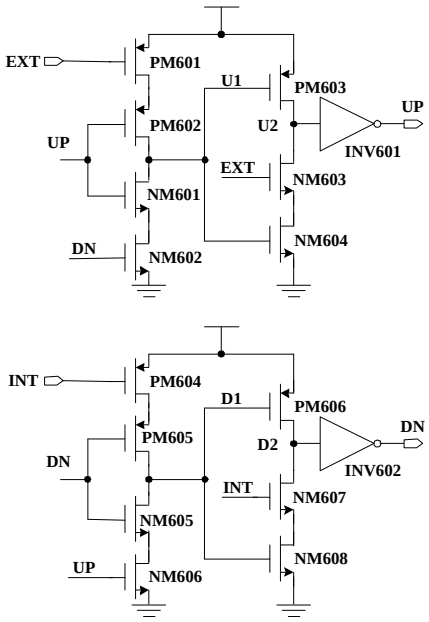

Fig. 5: The zero deadzone PFD.

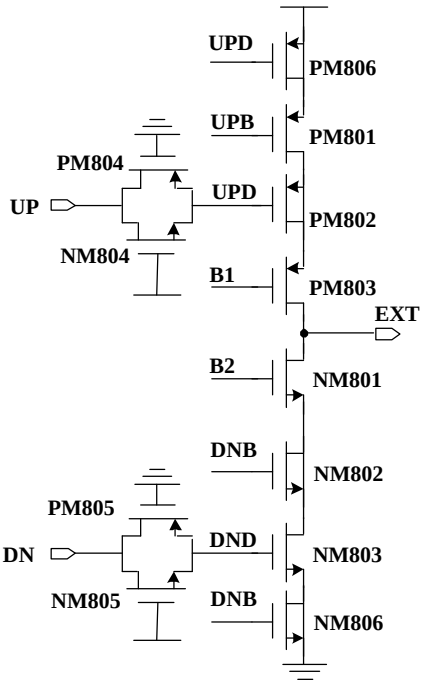

Fig. 6: Schematic of the charge pump.

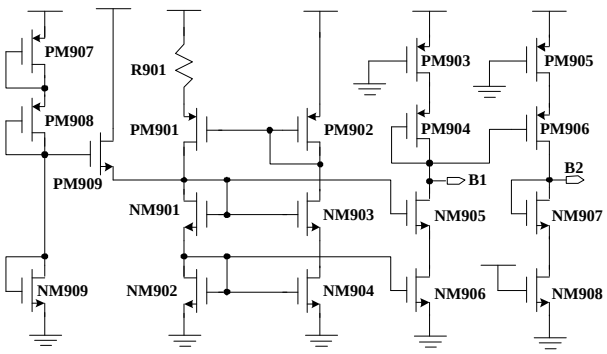

Fig. 7: The bias circuit of CP.

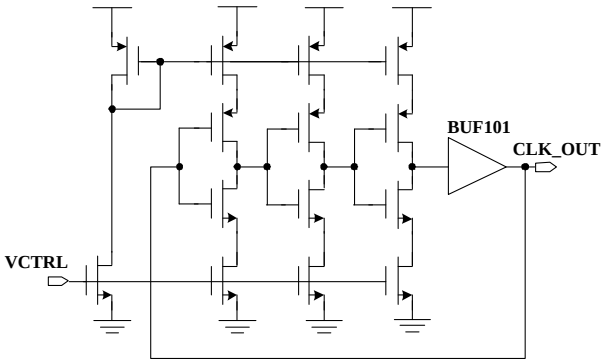

Fig. 8: The current-starved VCO.

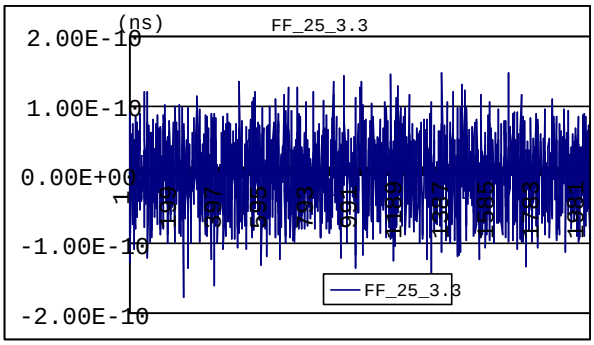

Fig. 9: p2p jitter post-layout simulation result in the worst case.

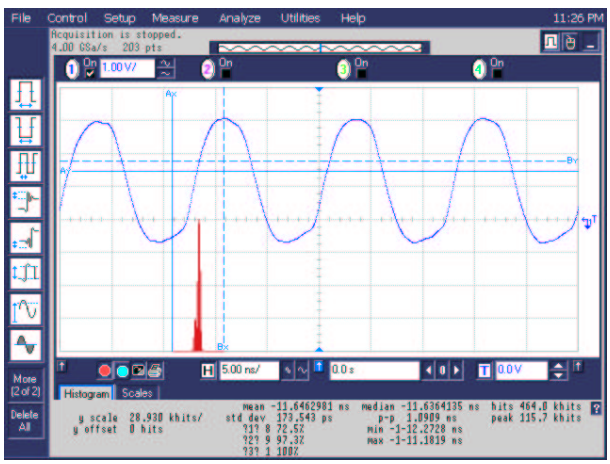

Fig. 10: The measurement jitter historgram of the PLL.

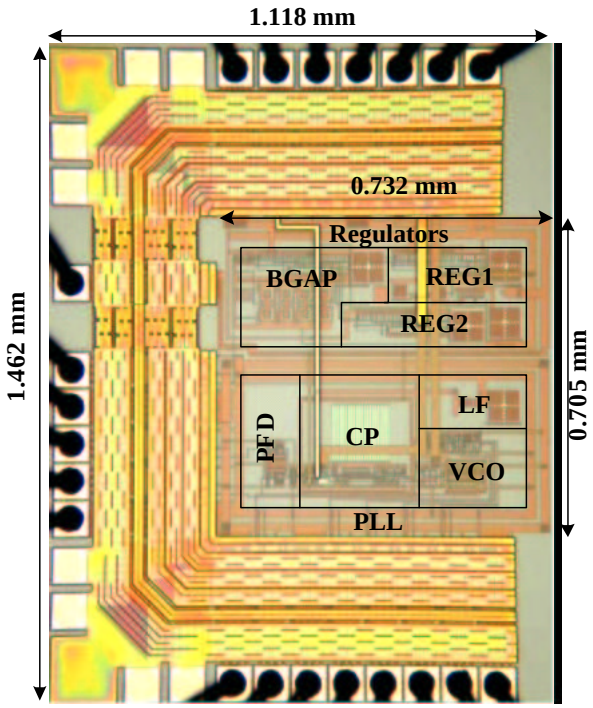

Fig. 11: The die-photo of the proposed PLL.