A LOW-JITTER 80 MHZ PLL FOR DVB-T RECEIVERS[§]

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Abstract–**This paper presents a design of a 60-ps peak-to-peak jitter, 80 MHz, phase-locked loop (PLL) circuit for digital video broadcasting over terrestrial (DVB-T) receivers. A step-down voltage regulator is utilized to suppress the coupled supply noise. A zero offset charge pump is employed to eliminate the static phase offset caused by the charge offset when the PLL is in lock. The simulation results using the TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 2P4M CMOS process show that the proposed PLL achieves as low as 60 ps peak-to-peak jitter when the output frequency is 80 MHz and the power consumption is merely 10.5 mW given a 3.3 V power supply.**

I. INTRODUCTION

The conclusive version of the standard for digital terrestrial television (DTTV) broadcasting was finalized by the DVB consortium in 1997, which has been known as DVB-T in many countries [1]. The digital television signals (in MPEG-2 format) are encoded for the purpose of error correction and modulated by a coded orthogonal frequency division multiplexing (COFDM) algorithm. DVB-T receivers, which should be capable of transforming the radio-frequency (RF) signal into an MPEG transport stream, must perform the down-conversion and sampling in the analog front-end. The RF signal is converted into low frequency signals and then fed to a following analog-to-digital converter (ADC). This signal is assumed to be sampled at 18.28 MHz and quantized by a 10-bit ADC in the prior work [2]. The performance would be much better if we sample the incoming signal at a higher frequency since the quantization error will be reduced. We, thus, select 80 MHz as the ADC sampling rate, since it is around four times of the prior 18.28 MHz sampling rate. Therefore, a PLL is required to generate such a 80 MHz clock with a low-jitter, since the jitter of the clock will result in a serious sampling uncertainty. The jitter at the output of the PLL might be caused by a variety of sources. It was shown that the contribution of device noise and thermal noise to jitter is typically much less than that caused by supply noise and substrate noise [3]. In this work, we employ several techniques to reduce the supply noise and other non-ideal effects in the PLL. The worst case of post-layout simulations justifies a 60 ps peak-to-peak jitter in the PLL output which is used as the clock source for the ADC in DVB-T receivers. The power consumption is found to be 10.5 mW @ 80 MHz by using TSMC 0.35 μm 2P4M CMOS technology.

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II. LOW-JITTER PLL ARCHITECTURE

Figure 1 is the block diagram of the proposed PLL. The supply noise is the major noise source which will impose irregular fluctuations upon the voltage-controlled oscillator (VCO) and the charge pump. The step-down voltage regulator is then utilized to provide a stable supply voltage for the VCO and the charge pump to reduce the supply noise. Besides, there are several non-ideal effects that would lead to a large phase noise of the PLL. For instance, the dead zone in the charge pump circuit will result in the accumulation of the random phase error in the VCO, and the charge offsets in the charge pump will cause the phase offsets. The phase-frequency detector (PFD) should assert the output signals, DN and UP, simultaneously for an equal duration to eliminate the dead zone. When the PLL is in lock, the net charge in the loop filter should not be drifting. Otherwise, these charge offsets introduce jitters even when the PLL is in lock. We utilize the zero offset charge pump [4] to prevent any net charge transferring from or to the loop filter. The VCO [5] without tail currents is employed to avoid the noise introduced by the mismatch of current mirrors. Meanwhile, we reduce the gain of the VCO to keep the phase noise from being over-amplified.

Phase-frequency detector (PFD)

The PFD compares the difference of phase and frequency between the external reference clock signal EXT and the feedback clock INT. Figure 2 is our PFD circuit which is the bang-bang-type PFD [6]. The speed of this kind of circuits result is limited by their critical delay path. Figure 3 shows the critical delay path, which is the path to reset all of the internal nodes in the circuit. The function of reset is to assert output signals, UP and DN, for a equal

duration. This duration is required to allow UP and DN signals reaching their logical levels to either turn on or turn off the current source/sink of the charge pump, respectively. Consequently, the PLL is still capable of adjusting phase and frequency even when the phase difference of EXT and INT equals to zero. Furthermore, if the charging current and discharging current are identical in such a scenario, the PLL can be locked in the zero phase offset state [6]. Figure 4 is the simulation result when the PLL is in lock.

Zero offset charge pump

Noise and the mismatch between charging current and discharging current in the charge pump invoke the phase error. Supply noise occupies a significant portion of noise, which will reduce the charge-pump gain. A step-down regulator is used to suppress the supply noise and provide a stable voltage for the charge pump as well as the supply voltage. Figure 5 is the schematic of the charge pump, which is the zero offset charge pump [4]. Referring to Figure 5, two NMOS source couple pairs are connected by the current mirrors composed of the symmetric load buffers. As mentioned before, the PFD asserts the signals UP and DN as two identical pulses once in every clock cycle when the PLL is locked. When both the UP and DN are asserted, the symmetric loads, PM01, PM02, PM03, and PM04, operate as a current mirror (I_{34}=I_{12}), and the right source coupled pair will sink the same current as that flowing through PM03 and PM04 (I_6=I_{34}). Since the current flowing into the loop filter is identical to that flowing out of the loop filter, these currents are canceled out to make the net charge in the loop filter be a constant. Hence, the zero static phase offset is ensured. Figure 6 shows the variation of VCTRL when the PLL is locked, where VCTRL is the output signal of the charge pump. The maximum variation in Figure 6 is less than 10 mV.

Voltage-controlled oscillator

Figure 7 shows the schematic of the VCO, which is a three-stage no-tail-current VCO [5]. Take a single stage as an example. The differential delay cell consists of the transistors NM11, NM12 and p-type cross-coupled pair formed by PM11 and PM12. NM13 and NM14 control the oscillation frequency of the VCO. The regulator provides the stable supply voltage to the VCO. The no-tail-current VCO is utilized to avoid the mismatch of current mirrors. Moreover, we reduce the gain of the VCO to suppress the jitter of the PLL. Although the reduction of the gain of the VCO decreases the tuning range, it poses no crucial influence on the desired DVB-T receiver applications. Figure 8 shows the gain of the VCO.

Regulator

The supply noise can be drastically isolated from the charge pump and the VCO by the regulator. Figure 9 is the schematic of our regulator. The bandgap circuit generates a stable reference voltage VBGAP which is insensitive to the variation of the temperature and the power supply. This reference voltage VBGAP is fed to the feedback network, which is composed of the operational amplifier OPA and resistors, to generate the desired voltage, VREG.

III. SIMULATION AND IMPLEMENTATION

The overall design is implemented by TSMC 0.35 μm 2P4M CMOS process. The layout of the proposed design is given in Figure 10. In order to simulate the power supply noise, we impose small 100 KHz, 1 MHz, 10 MHz, and 80 MHz signal sources upon the power supply. Each of them possesses the amplitude of 10 mV. Figure 11 demonstrates the variation of the VCO control signal, VCTRL, in the process of locking the phase. The initial frequency of the VCO is 65 MHz, namely, the initial difference between EXT and INT is 1.875 MHz. The lock time at 80 MHz is 2.26 μs as show in the Figure 11. Figure 12 shows the pick-to-pick jitter (p2p jitter) at several PVT (process, supply voltage, temperature) corners, where the p2p jitter is the maximum value derived from 1600 rising edges of the input clock. The maximum of the p2p jitter found at these corners is 60 ps. The overall post-layout simulation results are summarized in the Tabel 1. The comparison between our design and several prior works is summarized in the Table 2. Our design possesses the lowest p2p jitter without supply noise and desirable 60-ns p2p jitter with the presence of the supply noise.

input frequency	10 MHz
output frequency	80 MHz
peak-to-peak jitter	60 ps
power	10.5 mW @ 80 MHz
die size	1.29×1.318 mm^2
charge pump current	40 μA
damping factor	0.61
natural frequency	3.39 MHz

Table 1: Post-layout simulation results of the proposed design

	[7]	[4]	[8]	[9]	ours
process(μm)	0.8	0.5	0.5	0.4	0.35
output freq.(MHz)	592	550	240	612	80
p2p jitter(ps)	270	144	50	80	60* 23‡
power(mW) consumption	N/A	9.24	33	N/A	10.5
area(mm^2)	N/A	1.91	0.82	0.665	1.7

Table 2: Comparison to prior designs (* Note : with supply noise, ‡ Note : without supply noise)

IV. CONCLUSION

A 60-ps peak-to-peak jitter 80 MHz PLL design is presented in this paper. The regulator is utilized to reject the power supply noise. The zero charge offset charge pump and the differential VCO contribute to the reduction of the phase errors. The post-layout simulation of the PLL manifests its low jitter, thus making it suitable for the receivers of the DVB-T system.

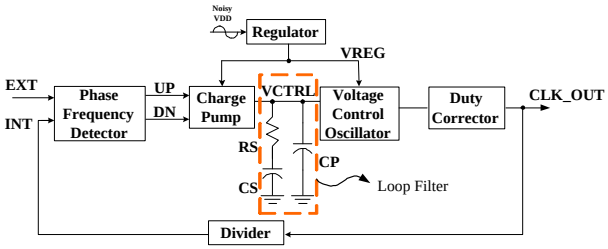


Figure 1: block diagram of the proposed PLL

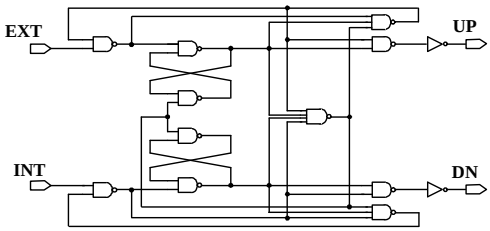


Figure 2: bang-bang-type PFD

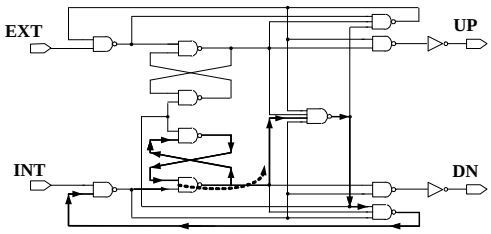


Figure 3: critical delay path of the bang-bang-type PFD

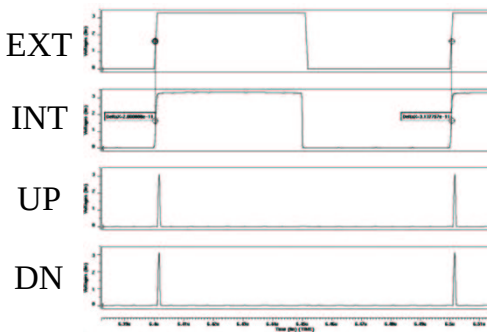


Figure 4: the simulation waveforms when the PLL is locked

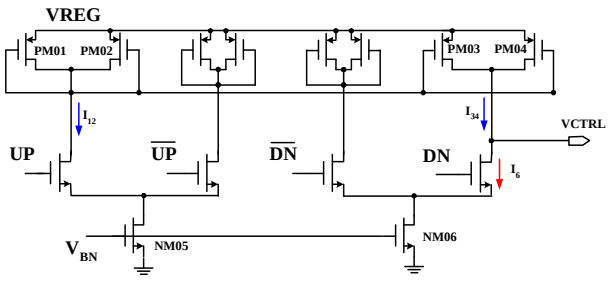


Figure 5s chematic of the charge pump

REFERENCES

[1] European Telecommunications Standardds Institute (ETSI) ETS 300 744 v1.1.2(1997-08): *Digital Video Brocasting (DVB); Framing Structure, Channel Coding and Modulation for Digital Terrestrial Television,* 1997.

[2] C. D. Toso, P. Combelles, J. Galburm, L. Lauer, P. P'enard, P. Robertson, F. Scalise, P. Semn, and L. Soyer, "0.5-μm COMS Circuits for demodulation and decoding of an OFDM-based digital TV signal conforming to the European DVB-T standard," *IEEE J. of Solid-State Circuits,* vol. 33, no. 11, pp. 1781-1792, Nov. 1998.

[3] F. Herzel, and B. Razavi, "A study of oscillator jitter due to supply and substrate noise," *IEEE Trans. on Circuits and Systems-II,* vol. 46, no. 1, pp. 56-62, Jan. 1999

[4] J. G. Maneatis, "Low-jitter and process independent DLL and PLL based on self-biased techniques," *IEEE J. of Solid-State Circuits,* vol. 31, no. 11, pp. 1723-1732, Nov. 1996.

[5] J. Lee, and B. Kim, "A 250MHz low jitter adaptive bandwidth PLL," *1999 International Solid-State Circuits Conference,* pp. 346-347, Feb. 1999.

[6] C. Kim, I. Hwang, and S. Kang "A lower-power small-area ±7.28-ps-Jitter 1 GHz DLL-Based clock generator," *IEEE J. of Solid-State Circuits,* vol. 37, no. 11, pp. 1414-1420, Nov. 2002.

[7] K. Yoon, and W. Kim, "Charge pump boosting technique for power noise immune high-speed PLL implementation," *Electronics Letters,* vol. 34, no. 15, pp. 1445-1446, 23, July 1998.

[8] Novof, J. Austln, R. Chmela, T. Frank, R. Kelkar, K Short, D. Strayer, M. Styduhar ,and S. Wyatt, "Fully-integrated CMOS phase-locked loop with 15 to 240Mhz locking range and ±50ps jitter," *1995 Inter. Solid-State Circuits Conf.,* pp. 112-113, Feb. 1995.

[9] W. B. David, "A Low-jitter PLL clock generator for microprocessors with lock range of 340-612 MHz," *IEEE J. of Solid-State Circuits,* vol. 34, no. 4, pp. 513-519, Apr. 1999.

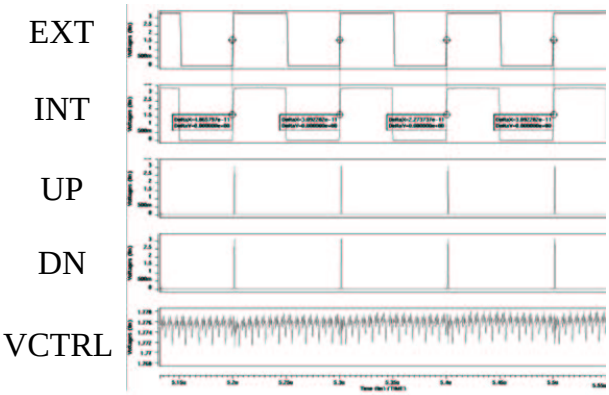


Figure 6: the simulation wavs84vu0eforms when the PLL is locked

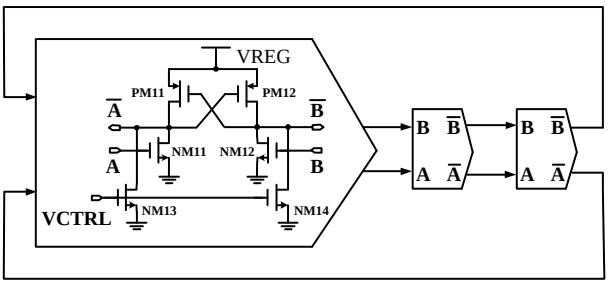


Figure 7: schematic of the no-tail-current VCO

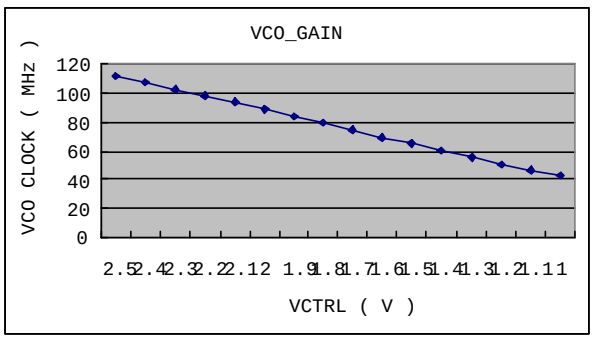


Figure 8: the gain of the VCO

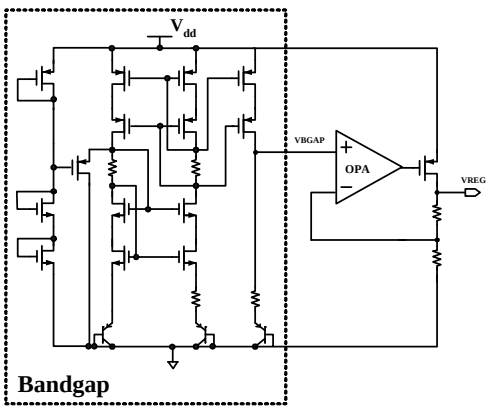


Figure 9: schematic of the regulator

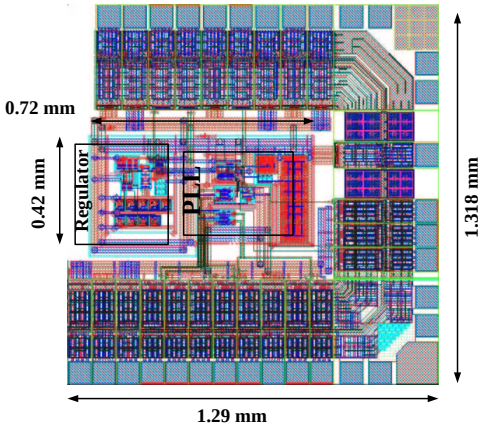


Figure 10: layout of the proposed PLL

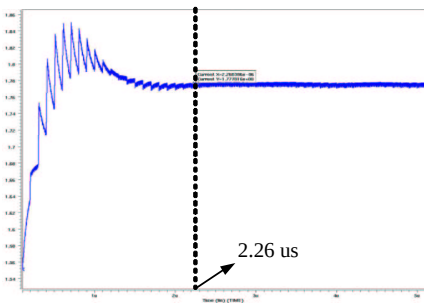
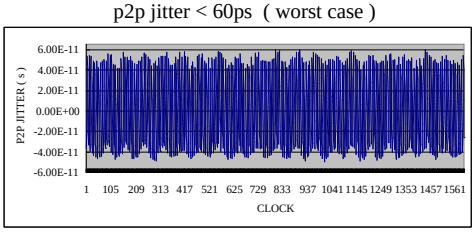


Figure 11: waveform of VCTRL

(with supply noise) SS model, 75 °C, VDD - 10 %
p2p jitter < 60ps (worst case)



(without supply noise) SS model, 75 °C, VDD - 10 %
p2p jitter < 23ps (worst case)

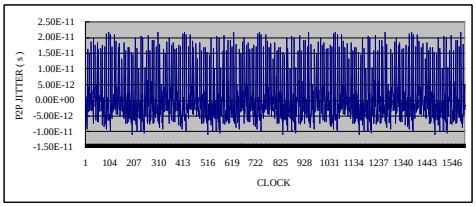


Figure 12: peak-to-peak jitter