A 38-DB STOPBAND ATTENUATION AND 120-DB CMRR SMALL-AREA LNA FOR NEURAL SIGNAL SENSING AND RECORDING[§]

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Abstract – **This paper presents a novel LNA (low noise amplifier) design for implantable biomedical devices and systems with 38-dB stopband attenuation and 120-dB CMRR (common-mode rejection ratio). The proposed LNA is composed of 4 stages, including a preamplifer, a 2nd-order LPF (low-pass filer), a differential-to-single converter (DSC) with high-pass filtering, and an output stage with high-pass filter. The proposed design provides a high stopband attenuation to the nearby noise close to the vague neural signals, and neutralizes the offset voltage and high impedance caused by the implanted electrodes. The neural signals, thus, can be faithfully sensed and recorded with least contamination and distortion. Detailed analysis of the circuitry is derived to solidify the proposed LNA architecture. The proposed design is implemented using TSMC 0.35 μm 2P4M CMOS process. The results of post-layout simulations verify the performance of our design. The CMRR is more than 120 dB, and the stopband attenuation is more than 38 dB/dec at all PVT (process, supply voltage, temperature) corners.**

I. INTRODUCTION

Information provided by implantable biomedical devices is essential to any further detailed neural diagnosis as well as treatment, e.g., implanted wireless chips in [3]. The sensing of the neural signals and the recording thereof allow the the use of the sensory signals as either feedback information or observational data to control the implanted devices, which can be a part of a neuroprosthesis. Notably, the neural signals possess low signal amplitude in the range of 1 to 10 μV, and low frequency in the spectrum between 100 Hz to 7 KHz. Therefore, the LNA (low noise amplifier), which is in charge of faithfully picking up vague neural signals hidden in the background noise floor, plays a critical role in the entire implantable system. Important measurements to justify the LNA include CMRR (common-mode reject ratio, > 90 dB), stopband attenuation (> 30 dB/dec), and high gain (> 80 dB). Besides, small area and low power are also considered as design goals, too. Although several LNA designs have been proposed, e.g., [2], [5], [6]. Most of these prior works did not meet all of the requirements, particularly the CMRR and the stopband attenuation. The former implies the capability of common-mode noise rejection, while the latter indicates that of rejecting noise close to the meaningful neural signals. The reason why CMRR is so important in LNA designs is that the electrodes used in the implantable systems to either sense or stimulate the nerves will cause a significant of offset voltage (around several hundreds of mV) and an inherent impedance. The stopband attenuation of the LNA characterizes the slope of the bandpass filtering which is supposed to be as large as possible such that the band rejection to the unwanted close noise in the spectrum can be ensured. In this work, a novel LNA design composed of 4 stages, including a preamplifier, a 2nd-order LPF (low-pass filer), a differential-to-single converter (DSC) with high-pass filtering, and an output stage with high-pass filter, is proposed. Several prior design techniques, including the DDA (difference differential amplifier) in [5] and [8], stable bandgap bias and current sources derived from [1], and the preamplifier in [6], are re-tuned and utilized to meet the design specifications.

II. HIGH CMRR LNA DESIGN

We have proposed an SOC (system-on-chip) design to carry out the mission utilizing wireless and non-penetrating transmission to accept external instructions and execute required stimulations [7]. The entire electrical micro-stimulus system is given in Fig. 1. In dual respect, the SOC chip is also expected to sense the response of the nerves, convert into wireless signals and finally send back to the external monitoring devices. The LNA is responsible for picking up the signals present at the electrodes surrounding the nerve. It is obvious that the neural sig-

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nals have very small amplitude while the background noise generated by the tissues, the fluid, or possibly the SOC chip itself is adequately large. Meanwhile, the LNA must get rid of all of the unwanted noise and amplify the sensory signal large enough to be accepted by the following ADC (analog-to-digital converter) to convert into meaningful binary signals.

4-Stage LNA architecture

The structure of the proposed 4-stage LNA is shown in Fig. 2. It is composed of four cascaded stages : a preamplifier, a 2nd-order LPF, a DSC with HPF, and an output buffer with HPF. Besides, a bandgap current reference, i.e., the I-reference, and a bandgap voltage bias, i.e., the V-bias, are also required to make the LNA stable at all PVT corners.

sub-circuit design

The first stage, which is the preamplifier, is mainly in charge of reducing the thermal noise effect. We adopt the preamplifier in [6] to attain a high input transconductance. The rest of the stages are described as the following text.

2nd stage - 2nd-order LPF : Obviously, RC-based LPF designs will not be an option in implantable devices, since they result in huge area consumption, thermal noise, and low performance. We adopt and modify the low-noise gm-C LPF design in [6] to be our 2nd-order LPF, as shown in Fig. 3. They are composed basically of a resonator loop with a linearized transconductance amplifier and floating capacitors. However, the short circuit of the foot current sink NMOS transistors are removed to increase the DC gain as well as the stopband attenuation. Referring to Fig. 3, the gm_0 stage provides the passband gain $\approx$ 15 dB. The gm_1 and gm_3 stages, respectively, creates a pole around 7 KHz to sharpen the slope of the transition band. Last but not least, gm_2 enhances the Q of the resonator loop.

bandgap current source : A temperature-insensitive voltage reference, [1], [4], with a current mirror is utilized to generate the required reference currents, I_bias1 and I_bias2, for the preamplifier and the 2nd-order LPF, respectively, as shown in Fig. 4. Notably, the resistor R_b1 with a positive temperature coefficient can be used to tune the magnitude of the reference currents such that the power consumption might be reduced as low as possible.

3rd stage - a DSC with HPF : The task of this stage is to define a pole at 100 Hz and convert the differential signal into a single-ended signal such that the following ADC can further convert the sensory signal into a binary format for digital signal processing. The DDA (differential difference amplifier), [8], [5], is utilized. Referring to Fig. 5, there are two differential input pairs in the circuitry. The first pair is for the actual input signals. By contrast, the second pair constitutes two feedback loops. The first loop provides the gain as follows.

$$A_{21} = \frac{R_{32} + R_{31}}{R_{31}} \tag{1}$$

Meanwhile, the second loop is a positive feedback loop producing a high-pass pole at the pre-defined 100 Hz. The analysis can be derived as follows.

$$V_o = D[V_i + V_o \cdot \left(\frac{1}{A_{21}} - \frac{-\beta}{s}\right)], \tag{2}$$

$$\beta = \frac{1}{A_{21} R_{int} C_{int}},$$

$$H(s) = \frac{D}{1 - D \cdot \left(\frac{1}{A} - \frac{-\beta}{s}\right)}$$

$$\approx \frac{A_{21} s}{s + A_{21}\beta}, \quad \text{if} D \to \infty \tag{3}$$

where D is the open-loop gain, and $H(s)$ is the transfer function.

However, since the high-pass pole is aimed at 100 Hz, either a large resistor or R_{int} or a large capacitor for C_{int} is required. Neither is acceptable in any implantable biomedical devices because of the area consumption. We, thus, select a feasible $C_{int} \approx 30$ pF, and replace the required large resistor with a biased PMOS, as shown in Fig. 6. The main idea is to supply stable bias voltages to the bulk and gate of the PMOS such that a large equivalent resistance is generated between the source and the drain thereof. The biasing circuitry of the PMOS is given in Fig. 7. The equivalent resistance of the PMOS, M_{eqr}, is derived to be as follows [5].

$$R_{eqr} = \frac{L_{M_{eqr}} W_{M_{r1}} R_{r1} \cdot K}{W_{M_{eqr}} L_{M_{r1}} \ln N}, \tag{4}$$

where $L_{M_{eqr}}$ and $W_{M_{eqr}}$ are the length and the width of M_{eqr}, K and N are the aspect ratio between M_{r5} and M_{r4}, respectively, to M_{r3}.

4th stage - output buffer with HPF : The last stage of the proposed LNA needs to add another high-pass pole at 100 Hz such that the stopband attenuation can be enhanced. Referring to 8, a 2nd-order HPF is revealed. The ratio of R_{42} to R_{41} defines the passband gain. Notably, R_{eqr41} and R_{eqr42} are realized by the same methodology of the large resistor, R_{eqr}. They are in the range of several MΩ. Thus, the capacitors, C_{41} and C_{42} can be reduced to a reasonable size on the chip. The function of V_{ext3} is to tune the output swing of this buffer stage to the voltage range for the following ADC.

III. SIMULATION AND IMPLEMENTATION

TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 2P4M CMOS process is adopted to carry out the proposed LNA design. The layout

of the proposed design is shown in Fig. 9 and the chip core area is 600 μm $\times$ 480 μm (1374 μm $\times$ 1282 μm with pads). Fig. 10 shows the filter transfer function at several PVT corners which shows that the passband gain is over 80 dB, and the stopband attenuation at both sides of the passband is over 38 dB/dec. The CMRR performance is revealed in Fig. 11 where the worst-case PVT corner is still over 120 dB. A performance comparison of the proposed design with several prior LNAs are summarized in Table 1. Though the proposed design consumes more power, mainly due to the number of stages, it still meets the power budget of the LNA. On the other hand, the proposed LNA possesses the least normalized area, the sharpest transition band, and the highest CMRR, which is considered as a better LNA design alternative.

IV. CONCLUSION

We have proposed an LNA using a 4-stage architecture using DDA, preamplifier, and PMOS-based large on-chip equivalent resistor to attain high CMRR, stopband attenuation, and small area. It is very suitable to be used in SOC-based biomedical implantable systems to sense and record the response of nerves.

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	[5]	[6]	ours
process	0.7 μm	0.7 μm	0.35 μm
area (mm^2)	1.1	2.7	0.3
passband (Hz)	100 $\sim$ 7K	100 $\sim$ 3K	100 $\sim$ 7K
DC gain (dB)	77 $\sim$ 103	55	80
stopband attenuation (dB)	$\approx$ 30	$\approx$ 20	$>$ 38
CMRR (dB)	96	80	$>$ 120
power (mW)	N/A	1.3	9.4
Applications	ENG	ENG	ENG

Table 1: Performance comparison of LNAs.

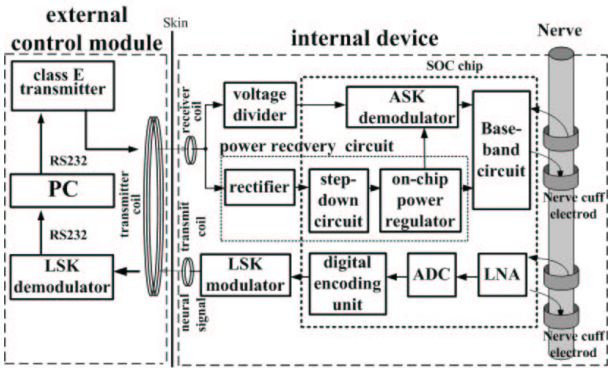

Fig. 1: The implantable micro-stimulation system.

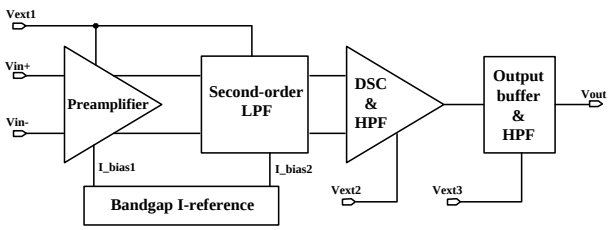

Fig. 2: The proposed LNA architecture.

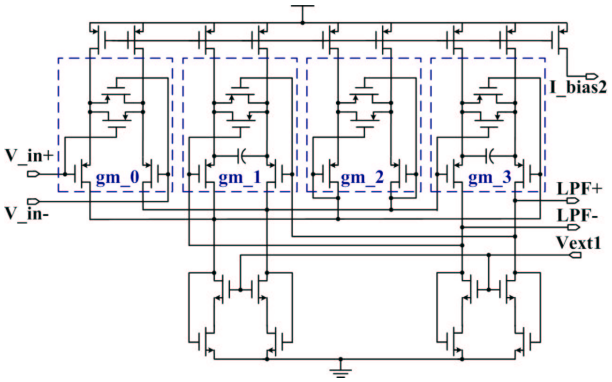

Fig. 3: The 2nd-stage : the 2nd-order LPF.

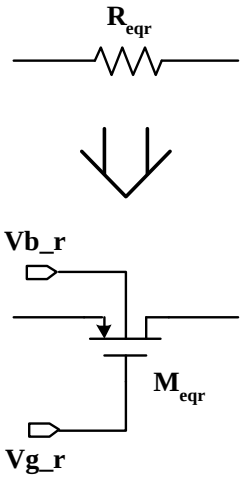

Fig. 6: PMOS-based equivalent resistor

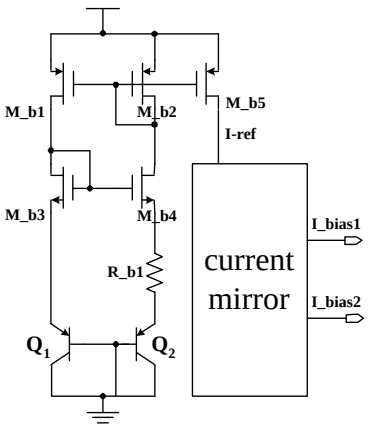

Fig. 4: Reference current sources.

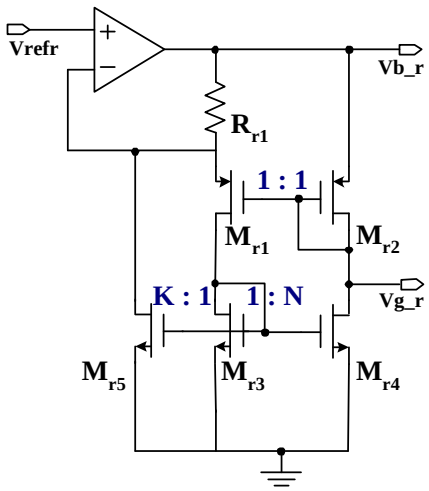

Fig. 7: Bias generator for the PMOS-based equivalent resistor

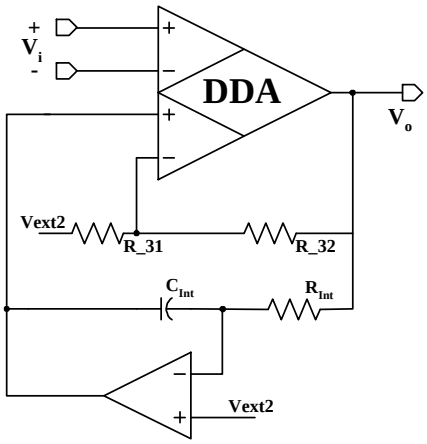

Fig. 5: The 3rd stage : the DSC with HPF.

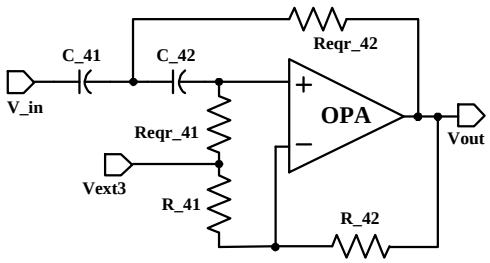

Fig. 8: The 4th stage : output buffer with HPF

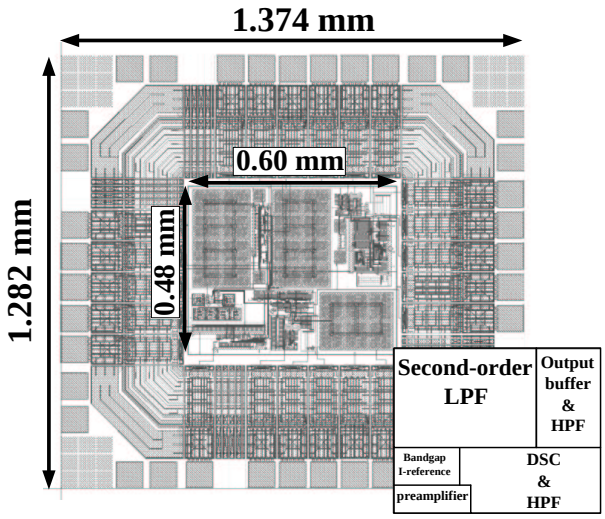

Fig. 9: Layout of the proposed LNA

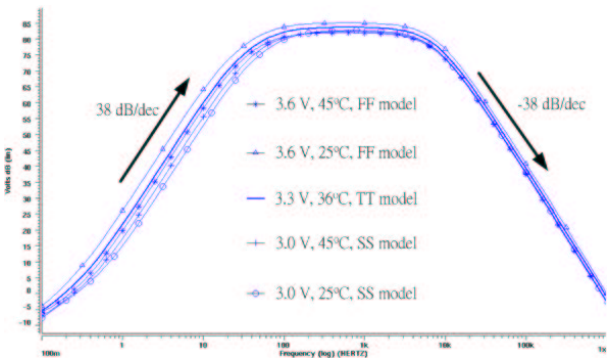

Fig. 10: Frequency response of the post-layout simulations

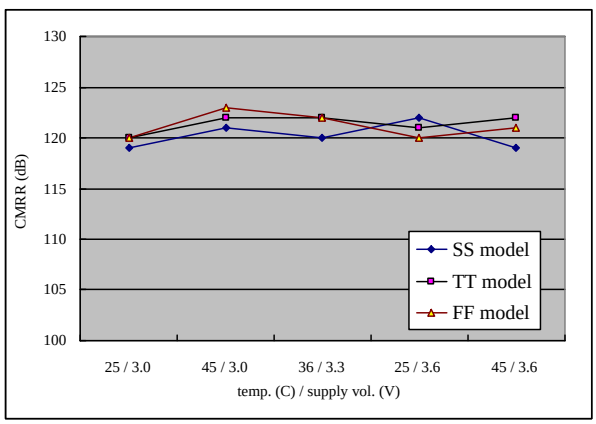

Fig. 11: CMRR performance of the proposed LNA