A 2K/8K MODE SMALL-AREA FFT PROCESSOR FOR OFDM DEMODULATION OF DVB-T RECEIVERS[§]

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ABSTRACT

We present a novel implementation for 2K/8K dual-mode small-area FFT for the OFDM demodulator of DVB-T receivers. Besides pipelining the FFT to reduce the area and enhance the data throughput, SDF butterfly units for radix-2 and radix-4 processing is adopted to resolve the power consumption difficulty and the P&R (place and route) problem. The SRAM is used in the butterfly units to relax the auto-refreshing requirement if DRAM is used.

I. Introduction

Digital TV (DTV) is currently one of the major consumer products which imposes a strong impact to a large amount of users globally. The DVB compliant DTV and set-top box (STB) has been gradually adopted in Europe as well as Asia mainly owing to that OFDM processing supported by DVB has been proven to overcome the multi-path effects in mobile receivers. It also leads to the concept of SFN (single frequency network) in which many transmitters send the same signal on the same frequency. With regard to the terrestrial broadcast, DVB-T allows two modes : 2K and 8K modes [5]. The former is proper to mobile receiving, while the latter is used in the SFN. The implementation of the FFT is the most difficult part for the DVB-T receivers [5]. Hence, many efforts have been thrown upon the research of efficient implementation of the FFT realization. Pipelining is probably the most common feature in prior designs, [1], [3], [5]. However, the design of a more area-efficient butterfly stage seems to play a more important role which determines the throughput of the pipelining architectures. In this work, we adopt a SRAM-based SDF (signal-path delay feedback) butterfly stage in a DIF (decimation in frequency) rather than a DIT (decimation in time) FFT design.

II. Low-Power Small-Area FFT Design for OFDM

An illustrative DVB-T receiver is shown in Fig. 1. According to the DVB-T specifications, FFT/IFFT should be able to carry out 8192(8K) points in carrier spacing interval. It can be told that the realization of the OFDM Demodulator, i.e., the 2K/8K FFT, is the very critical part since it directly affects the accuracy of the channel estimation as well as the symbol demapper.

FFT theory

The basic butterfly stages widely used in prior FFT designs are radix-2, radix-4, radix-n, and split-radix. The radix-2 unit is the most popular one owing to its simplicity. However, when the points of the FFT required to be computed increase, radix-4 will possess the edge of less computation complexity. Another factor to be take into consideration is the difference between DIT and DIF. Since the OFDM algorithm is based upon the utilization of multiple subcarriers, we tend to adopt DIF scheme instead of DIT to avoid any transformation between time domain and frequency domain.

The input signal to the N-point FFT is denoted by $x[n]$. Hence, it is well known as follows : $X[k] = \sum_{n=0}^{N-1} x[n]W_N^{nk}, \quad k = 0, 1, \ldots, N-1$, where $W_N^{nk} = e^{-j2\pi nk/N}$ is the twiddle factor. Thus, the function of a radix-4 unit is represented by the following equality : $X[4r+p] = \sum_{n=0}^{N/4-1} \{x[n] + x[n+\frac{N}{4}] \cdot W_4^p + x[n+\frac{N}{2}]W_4^{2p} + x[n+\frac{3N}{4}]W_4^{3p}\} \cdot W_N^{np} \cdot W_{N/4}^{np}$, where $r = 0 \sim (N/4) - 1$, $p = 0, 1, 2, 3$, and $n = 0 \sim (N/4) - 1$. Notably, $x'[n]$ is the intermediate value of $x[n]$ in the figure.

Low-power FFT architecture

The DVB-T specs require that the symbol data rate is 8 MHz. Given such a high data, the stage of memory as well as the routing area will be very demanding particularly in the 8K mode (= 8192 symbols). The pipeline structure seems to be an unavoidable option to carry out the high data rate design. Fig. 2 shows the pipeline structure of the 2K mode FFT design. Every block in Fig. 2 is called a butterfly stage. Notably, the data are serial-in-serial-out. For instance, the top-leftmost radix-4 butterfly stage won't start the operation until the 0th ($x[0]$), the 512nd ($x[0 + 2048/4]$), the 1024th ($x[0 + 2048 \cdot 2/4]$), and the 1536th ($x[0 + 2048 \cdot 3/4]$) points. As soon as the radix-4 computation is done, the result is propagated to the very next stage. As for the next operation of the top-leftmost butterfly stage, it is triggered as soon as the the 1537th ($x[0 + 2048 \cdot 3/4 + 1]$) point is collected. Obviously, the number of waiting latencies is reduced.

The process of 2K mode is composed of 5 radix-4 stages and one radix-2 stage. By contrast, the 8K mode is realized by 6 radix-4 stages and one radix-2 stage. For the sake of area-saving, the first radix-4 stage can be bypassed by a mode selection signal. Notably, since the DIF is adopted in our design, the final result generated by the last radix-2 stage must be bitwise reversed.

Low-power butterfly unit

The radix-4 unit used in the proposed FFT is shown in Fig. 3. Notably, the temporary storage elements are SRAMs which consume much less area than DFF-based registers, and no self-refreshing dynamic power consumption as the DRAM-based storage cells. A single operation of the radix-4 butterfly unit is composed of 4 cycles, which are summarized as follows.

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cycle 0-2 : The input data point, $x[n]$, $x[n+N/4]$, $x[n+N/2]$, are serially read and stored in individual SRAM cells. Meanwhile, the intermediate values of the last OFDM demodulation operation, $x^{'}[n+N/4]$, $x^{'}[n+N/2]$, $x^{'}[n+N\cdot 3/4]$, are delivered to the next pipeline stage after the multiplication with twiddle factors stored in the ROM.

cycle 3 : As soon as $x[n+N\cdot 3/4]$ is ready, the operation of the radix-4 butterfly is triggered. The generated intermediate values will then be stored, which will be delivered in the next butterfly operation.

It can be concluded that as soon as the operation of the previous symbol is completed, the next one will take place right away. There is no waiting latency nor idle cycle. The throughput of the pipeline structure is maximized.

III. Simulation and Implementation

The proposed FFT is implemented by TSMC 0.35 μm 2P4M CMOS technology to verify the performance. Notably, all of the process corners : [0°C, +100°C], (SS, TT, FF) models, and VDD±15%, are simulated. The layout of the proposed Tx and Rx on silicon is shown in Fig. 4. Meanwhile, we also make a performance comparison of our FFT with several prior designs in Table 1. Not only do we have the smallest gate count as well as the chip area, the proposed design consumes the least power in general.

References

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	[1]	[3]	[4]	[2]	ours
Tech.	0.5 μm	0.5 μm	0.5 μm	0.5 μm	0.35 μm
Area	N/A	N/A	140 mm^2	1.0 cm^2	35.75 mm^2
#Gate	1.8 M	1.1 M	1.3 M	1.5 M	139 K
Power	N/A	N/A	650 mW	600 mW	535 mW
Rate	9.14 MHz	4R	N/A	N/A	8 MHz
modes	2K	2K/8K	2K/8K	8K	2K/8K

Table 1: Performance comparison

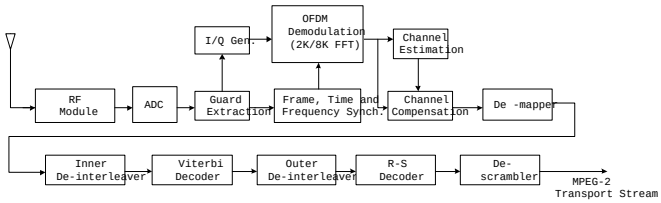

Figure 1: DVB-T receiver

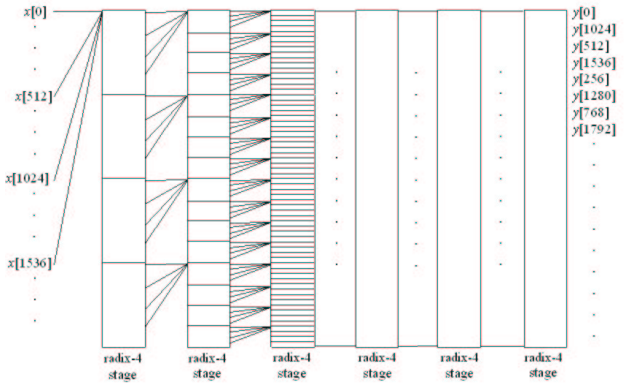

Figure 2: 2K/8K mode pipeline-structured OFDM FFT

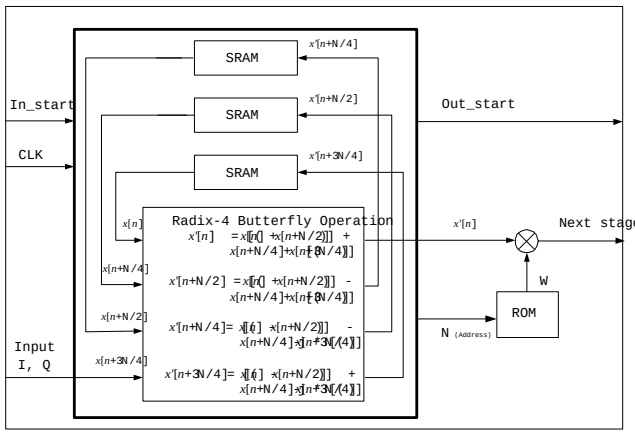

Figure 3: schematic of the proposed radix-4 butterfly

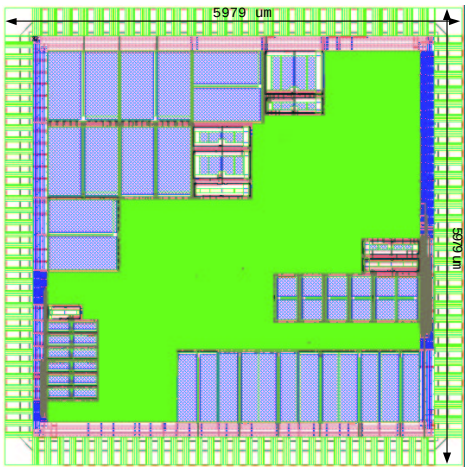

Figure 4: layout of the proposed FFT for OFDM demodulator