LOW-COST VIDEO DECODER WITH 2D2L COMB FILTER FOR NTSC DIGITAL TVS[§]

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ABSTRACT

A low-cost video decoder for NTSC signals is present in this paper. The proposed NTSC video decoder design employs a 2D2L comb filter, and a DDFS-based DCO (digital control oscillator) basing upon trigonometric quadruple angle formula in a digital PLL to track and lock the demodulation clocks. The complexity of the digital video decoder, hence, is drastically reduced.

I. Introduction

Video decoder (VD) plays a very important role in the design of the most popular consumer electronics, TVs. Particularly, NTSC-based TVs [1]. The tasks of the VD include the Y/C separation, sync separation, and color demodulation. Many prior works have been reported to pursue the digital version of NTSC TV. The difficulties to recover the color information are resulted from the poor received signal quality which in turn introduces serious jitters existing in the clocks of color burst as well as the H-sync and V-sync. We, thus, analyze the PSNR (peak noise to ratio) performance of different comb filters to explore the low-cost feasibility. A novel NTSC video decoder solution with a DDFS-based DCO (digital control oscillator) and a 2D2L comb filter is present in this work.

II. Digital Video Decoder Design

An overview of a generic digital NTSC video decoder system is shown in Fig. 1, which is used to extract the Y (luminance) and C (chrominance) signals of an NTSC signal given in Fig. 2.

Comb Filter Selection : Three widely adopted comb filters are 2D1L, 2D2L, and 3D2F (D: delay, L: line, F: frame). The larger the numbers of lines and frames means the large the memory sizes to be used. Besides, the 3D2F comb filter requires much more memory size to store two frames of video data. The transfer functions of the 3 types of comb filters are as follows.

$$\textbf{2D1L} \quad C : 0.5 - 0.5 \cdot z^{-1}, \quad Y : 0.5 + 0.5 \cdot z^{-1} \tag{1}$$

$$\textbf{2D2L} \quad C : -0.25 + 0.5 \cdot z^{-1} - 0.25 \cdot z^{-2}, \quad Y : +0.25 + 0.5 \cdot z^{-1} + 0.25 \cdot z^{-2} \tag{2}$$

$$\textbf{3D2F} \quad C : 0.5 + 0.5 \cdot z^{-1}, \quad Y : 0.5 - 0.5 \cdot z^{-1} \tag{3}$$

Many different video patterns are used to measure the PSNR of the mentioned comb filters, e.g., patterns in Fig. 3. The definition of the PSNR is as follows : $\text{PSNR}_{dB} = 20\log_{10}\frac{2^n-1}{\text{RMSE}}$, where RMSE denotes the root mean square error. Notably, every line of the video signal is 328×3×8 ≈ 8K bits, while a frame is composed of 525 lines which means we need to use a 525×328×3×8 ≈ 4M bits to store a whole frame. Although the 3D2F has the best PSNR, it requires to store two frames of video data which are far larger than the other two comb filters. Hence, the 2D2L comb filter is employed in the final chip implementation.

Clock recovery by DDFS-based DCO : Prior works proposed many complicated comb filter designs to pursue the quality of the decoded images. What worse is that a high-resolution ADC might be required to resolve the problem. The bottom line of this problem resides in the line length variation of the received NTSC signal which leads to the synchronization difficulties of H-sync edges. We adopt two methods besides the weighting window [3] to relax this problem.

A. Digital PLL : The jitter of the burst clock causes the locking problem of the burst clock. The received NTSC signal has neither constant swing nor amplitude. A sophisticated DDFS-based DCO is used to replaced the common VCO in the proposed video decoder. Notably, the large and slow cos and sin ROMs can be removed by using a modified 4θ-based DDFS which will be described later in the following text. The sampling frequency is selected to be an integer times of the sub-carrier's frequency to minimize the phase error. If it is not the case, a significant variation of phase error will be produced. A digital version of the loop filter (LF), which is a 1st-order IIR, is included in the digital PLL. The equivalent loop contants, C_1 and C_2, are determined by the following $w_n = \frac{1}{T}\sqrt{\frac{4C_2K_oK_d}{4-(2C_1+C_2)K_oK_d}}$, $\zeta = \frac{C_1}{2\cdot C_2}\sqrt{\frac{4C_2K_oK_d}{4-(2C_1+C_2)K_oK_d}}$, $T_n = \frac{2\pi}{w_n}$, where T is the sampling period, K_o and K_d denote the gain of PFD and VCO, w_n is the natural frequency, T_n is the lock time.

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B. ROM-less DDFS : A modified 4θ-based DDFS [3] is employed to carry out the function of the required DCO such that the slow and large ROMs can be removed. The central frequency is set to be 3.58 MHz. The sin and cos ROMs are pre-computed by [3] and hard-wired with combinational logic to get rid of real embedded and slow ROMs.

Chrominance Demodulator : The C is derived to be : $C = (C_b - 128) \cdot 0.504 \cdot \sin wt + (C_r - 128) \cdot 0.711 \cdot \cos wt$. The C_b and C_r are produced after the multiplication products of C and the outputs of the digital PLL are low-passedly filtered based on the follows.

$$2 \cdot 1.406 \cdot \cos wt \cdot C \quad \rightarrow \quad C_r - 128 \qquad (4)$$

$$2 \cdot 1.984 \cdot \sin wt \cdot C \quad \rightarrow \quad C_b - 128 \qquad (5)$$

The LPF to execute the filter operation is a 20-tap transposed FIR. Notably, the 128 in Eqn.(4) and (5) is an DC offset of the 8-bit ADC.

III. Simulation and Implementation

Artisan 0.35 μm 1P4M CMOS technology cell library is adopted to implement the proposed design. Post-layout simulation results of proposed video decoder are revealed in Fig. 4. The overall characteristics of the proposed video decoder as well as the comparison with prior works are summarized in Table 1.

References

[1] Faroudja, and Y. Charles, "NTSC and Beyond," *IEEE Trans. on Consumer Electronics,* vol. 34, no. 1, Feb. 1988.

[2] M. Ohta, K. Kohiyama, N. Tahara, K. Sugihara, F. Asami, O. Kobayashi, Y. Hino, and T. Akiba, "A single-chip CMOS analog/digital mixed NTSC decoder," *IEEE J. of Solid-State Circuits,* vol. 25, no. 6, pp. 1464-1469, Dec. 1990.

[3] C.-C. Wang, Y.-L. Tseng, C.-C. Chen, and C.-S. Chen, "Low-cost NTSC Digital Video Decoder Using 4θ-based DDFS," *2003 Workshop on Consumer Electronics (WCE2003),* pp. 41 (CD-ROM version), Nov. 2003.

	[2]	[3]	ours
Area (mm^2)	67.76 ‡	6.02	7.22
Power	980 mW	86 mW	109.2 mW
Gate#	N/A	39 K + 2×8 Mb SRAM	22 K + 3×8 Mb SRAM
Process	1.2 μm 2P2M	0.35 μm 1P4M	0.35 μm 2P4M
avg. PSNR	N/A	15.59 dB	18.36 dB

‡ : estimated from the die photo

Table 1: Performance comparison

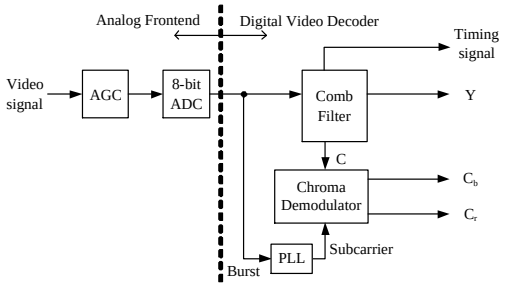

Figure 1: Overview of a digital NTSC video decoder

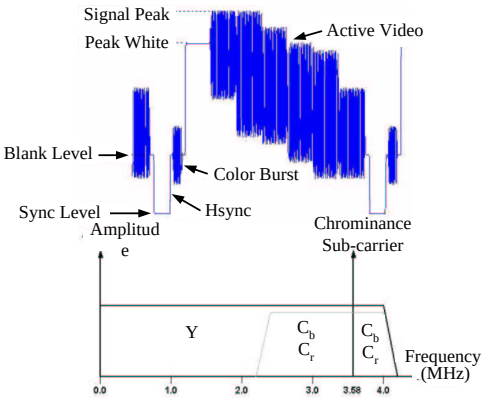

Figure 2: NTSC signal in time domain and frequency domain

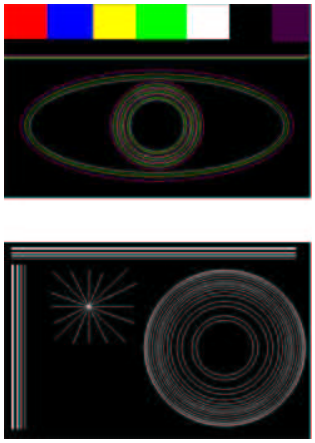

Figure 3: Two of test patterns for comb filters

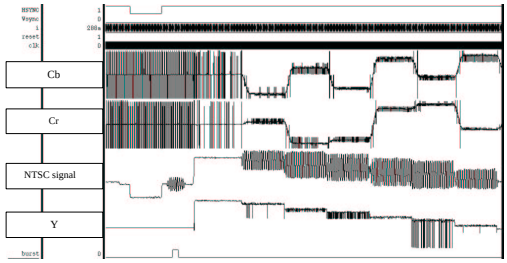

Figure 4: Post-layout simulation result