HIGH-PSR NTSC VIDEO SYNC SEPARATOR[§]

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ABSTRACT

This paper presents a novel NTSC video sync separator (NSS) with a high-PSR (power supply rejection) bias generation circuitry (BGC) which comprises a temperature compensation circuitry. The proposed BGC utilizes step-down regulators and a bandgap-based bias with cascode current control. The clamping voltages required for sync separation from an NTSC signal are generated. Detailed PSR analysis of the proposed BGC is also derived to circumscribe the clamping voltage variation. The worst variation of the proposed design verified by HSPICE post-layout simulations is 5% given a [-50° C, +150° C] temperature range, and a VDD(= 5V)±10%.

Keywords : NTSC signal, clamping levels, PSR, bandgap bias, sync separation

1. INTRODUCTION

Video decoders NTSC TV products, e.g. [5], heavily reply on precise clock sources, particularly HSYNC, VSYNC, color burst, even/odd field, and back porch [3], [4]. However, these clock sources built in the TV-related products, particularly the compact hand-held or mobile TVs, will be drastically affected by the ambient temperature as well as the highly unreliable power supplies. Those mentioned clock signals existing in the NSTC composite signals might not be extracted correctly. On top of that, the generated heat will be very likely to drift the clock edges if there is no compensation mechanism. Severe damages are possibly made, e.g., fuzzy image and ghost shadow problems. Lots of work have been done to develop design methods of the NTSC sync separation circuitry. Most of the product datasheets, e.g., [4], were focused on the functionality of video signal processing. On the other hand, most of the related prior works were focused on either the bandgap designs [1], [2], or simple clock generations [5], [6], [7]. A fact which has been long ignored is that the hostile environment jeopardizes the clock locking and the voltage clamping of a video decoder [8]. Besides, the peak-to-peak amplitude of the received NTSC signals, called V_{pp}, will be varied from 2V to 5V. A temperature-insensitive bias generation circuitry, thus, is required to provide stable reference voltages for clock tracking, data slicing, and noise rejection. Hence, we present a NTSC sync separator with a robust temperature-insensitive bias with high PSR (power supply rejection) comprising regulators and a reference voltage generator to resolve the problem. The worst-case variation of the bias is estimated to be less than 5%.

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2. ROBUST NSTC SYNC SEPARATOR

Although EIA (Electronic Industries Alliance) has announced that the V_{pp} of the NTSC signal is set to 140 IREs [3], the amplitude of V_{pp} might still be varied form 2 $\sim$ 5 V in hostile environments [4]. Besides, the power supply voltage is likely to be an unreliable source, particularly in those hand-held TV sets. However, several clamping voltages are needed to extract the clock information in the received NTSC signal such that the peak white, black level, clip level, and sync tips can be correctly extracted and separated. The architecture of the proposed sync separator is shown in Fig. 1. The bias voltages generated by the High-PSR Bias are fed to OSC as well as Sync Generator. OSC is in charge of generating a stable clock, which is set to 12.0 MHz in this work, to the following DSP core. On the other hand, the DAC (digital to analog converter) converts digital signals from the DSP core into a voltage which is monitored by AGC (auto-gain control) to dynamically adjust threshold voltages required in the Clamper.

2.1. High PSR Bias Generator

The performance of the entire NSS highly depends upon the sensitivity of the bias, i.e., Bias in Fig. 2. The proposed bias circuit comprising regulators, a bandgap bias (BB) with high PSR, and a resistor string, is proposed to resolve the difficulty of providing the required clamping voltages.

The temperature independent bias generated by the BB, called V_{ref}, is fed into the plus input of the OP-AMP in Regulator 1 as well as the minus input of the OP-AMP in Regulator 2. Meanwhile, the BB also supplies a pair of bias voltages to control the gate drives of the cascode pair in Regulator 1 which in turn stabilizes the source current (tail current) of the built-in OP-AMP in the regulator.

A. High PSR bandgap

The bandgap reference, i.e., BB, is shown in Fig. 3. Notably, the casocde configuration comprising PM31, PM32, PM33, PM34, PM35, and PM36, and the feedback loop consisting of OP-AMP A_{OP1} and NM31 are employed to resist the noise coupled with the power supply, VDD. The output impedance from V_{ref} looking into the drain of PM34 will be increased to $\approx g_m r_o^2$ at the sacrifice of the "headroom" of the output swing. However, since the the

circuitry is aimed at the clamping voltage generation which is usually below 2.0 V, it will not introduce any problem. Meanwhile, A_{OP1} monitors the voltage difference at node V_{31} and V_{32} to control the current via NM31, which in turn stabilizes the voltage of the PMOS cascode configuration.

Assume A_1 and A_2 are the area of the BJTs, Q_1 and Q_2, respectively. The expected V_{ref} is analyzed as follows.

$$V_{ref} = I_2 \cdot R_2 + V_{EB2} = V_{EB2} + L \cdot V_T \cdot \ln(K), \qquad (1)$$

where K is the BJT area ratio, i.e., A_1/A_2, the ratio of R_2/R_1 is assumed to be L. Hence, the bandgap reference can be pre-determined by tuning L and K.

B. PSR analysis

Since the NM31 acts as a current subtractor to control the gate drives of PM32, PM34, and PM36, we simply analyze the voltages applied to the plus and minus inputs of the OP-AMP A_{OP1} to find out the PSR which is defined as : $V_{32} = \frac{\frac{1}{g_{mQ_2}}}{R_2+\frac{1}{g_{mQ_2}}+g_{mp}r_{op}^2} \cdot \mathrm{VDD}$, $V_{31} = \frac{R_1+\frac{1}{g_{mQ_1}}}{R_1+\frac{1}{g_{mQ_1}}+g_{mp}r_{op}^2} \cdot \mathrm{VDD}$, where g_{mQ_1} and g_{mQ_2} denotes the transconductance of Q_1 and Q_2, respectively, g_{mp} and r_{op} represents the transconductance and the output impedance of the PMOS transistors in the cascode configuration. Thus, the PSR is found to be,

$$\mathrm{PSR} \approx \frac{\mathrm{VDD}}{V_{32}-V_{31}} \cdot \frac{1}{A_{OP1}} \approx \frac{1}{\frac{R1}{g_{mp}r_{op}^2}} \cdot \frac{1}{A_{OP1}} \qquad (2)$$

The A_{OP1} is supposed to be an ideally large gain to avoid other side effects. Hence, we can reduce $\frac{R_1}{g_{mp}r_{op}^2}$ to increase the PSR by a small R_1 and a cascode configuration.

C. Regulators

One of the most efficient approaches to avoid the effects of unstable power supplies is to employ step-down bandgap-referenced voltage regulators to supply a temperature independent reference voltage, V_{ref}, to the rest of the circuitry [7]. Since the received V_{pp} might be as low as 2.0 V, the generated V_{ref} should be no higher than this lower bound. Referring to Fig. 4, Regulator 1 is composed of PM41, PM42, NM41, R_0, R_L, and OP-AMP A_{OP2}. Notably, PM41 and PM42 are cascoded to provide a high output impedance and two stable reference voltages, V_{P41}, V_{P42} to the following OP Bias Generator (OBG). With large $\frac{\partial I_{o1}}{\partial V_{o1}}$ (V_{o1} is the voltage at NODE A.), the loading effect at NODE A can be reduced. Assume R_{out1} is the output impedance from OBG looking into NODE A. gm_{PM41} and gm_{NM41} are the transconductances of PM41 and NM41, respectively. Since PM41 and PM42 are sized equally, the transconductance of PM42 is equal to gm_{PM41}. The relationship between $\frac{\partial I_{o1}}{\partial V_{o1}}$ and R_{out1} can be derived as: $\frac{\partial I_{o1}}{\partial V_{o1}} = \frac{1}{R_{out1}}$, $R_{out1} \approx \frac{2}{gm_{\mathrm{PM41}}} \parallel gm_{\mathrm{NM41}} \cdot r_{oA2} \cdot (R_o \parallel R_L)$, where r_{oA2} is the output impedance of A_{OP2}.

Because of small R_{out1}, $\frac{\partial I_{o1}}{\partial V_{o1}}$ will be large enough to ignore the loading effect. Such that stable bias voltages can be achieved. Similar results can be derived at NODE B. The output bias of OBG, V_{op1} and V_{op2}, are used to control the tail current of the differential stage of A_{OP3}. Regulator 2 comprising A_{OP3}, PM61, and a resistor string, is shown in Fig. 5.

2.2. Clamper and Timing

The generated V_{burst}, V_{sync}, and V_{bottom}, are fed into the Clamper shown in Fig. 6 to serve as the slicing thresholds. The NTSC signal will be coupled to the clamper via a LPF with a 600 KHz stopband. By contrast, if the color burst signal is also taken into account, the LPF can be switched to a 3.58 MHz stopband. The external digital control signals, DI3, ..., DI6, cooperated with the output of A_{op6}, i.e., DI7, to control the switches in the clamper, as shown in Fig. 6. The truth table of the digital control block is given in Table 1.

The output voltage of the DAC is coupled to the positive input of A_{op5} of which the negative input is the V_{LPF}, which is the output of the filtered NTSC signal. The output of A_{op5} is fed into the gate drive of NM101 in Fig. 7 which is the schematic of the Clamper. Namely, it is the AGC (auto gain control) pin to dynamically adjust the threshold voltage level. In short, the operation of the AGC loop comprising Clamper and A_{op5} is summarized as follows.

$V_{LPF} \uparrow \Rightarrow V_{AGC} \downarrow \Rightarrow$
$V_{DAC} = V_{LPF}$ when SW00 is turned on $\Rightarrow V_{LPF}$ stable

Thus, the DAC output voltage serves as a dynamically adjustable level to determine and clamp the NTSC video signal. Besides the clamper, the proposed sync separator also generates two critical digital signals which will be utilized in the following DSP core.

HSYNC : HSYNC is generated at the output of A_{op6} by comparing the V_{fd} which is a DC level provided by Clamper and the output of A_{op4} which is a threshold voltage level.

$V_{\mathbf{all\ data}}$: This signal is present at the output of A_{op7} which comprises all of the edges of the original NTSC signal.

$V_{\mathbf{composite}}$: By the combination of switches EI1 and EI2, A_{op8} outputs a waveform composed of VSYNC and HSYNC which are both required in the later DSP operations.

3. SIMULATION AND IMPLEMENTATION

TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 2P4M CMOS process was adopted to carry out the proposed design. According to Eqn. (1), the following equality for a temperature-independent bandgap reference is derived.

$$\frac{\partial V_{ref}}{\partial T} = L \cdot \ln(K) \cdot \frac{\partial V_T}{\partial T} + \frac{V_{EB2}}{\partial T} = 0 \qquad (3)$$

By substituting all of the parameters in the above equation and setting $L = 10$, $K = 8$, $R_1 = 140\Omega$, the V_{ref} is found to be approximately 1.15 V. Then, we select the most common clamping voltages for the NTSC signal given a 5 V power supply : $V_{burst} = 3.30$ V, $V_{sync} = 1.92$ V, and $V_{bottom} = 1.69$ V, to design the entire bias circuitry. Fig. 8 shows the layout of the proposed design.

The post-layout simulations are revealed, respectively, in Fig. 9 (HSYNC) and Fig. 10 ($V_{\mathrm{all\ data}}$), given all of the PVT corners.

4. CONCLUSION

We have proposed a temperature-insensitive high-PSR bias generation circuitry for the sync separation of

NTSC signals in this paper. The cascode configuration as well as the regulators stabilize the clamping levels to cope with hostile receiving environments. Besides the physical implementation, the detailed PSR analysis of the proposed design is also revealed to illustrate the methodology. All of the required sync signals are successfully extracted for any later digital signal processing. The accuracy of the chip is enhanced to be less than 5 percent in all of the critical conditions.

5. REFERENCES

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INPUT				
DI3	DI4	DI5	DI6	DI7
0	0	X	X	X
0	1	X	X	X
1	0	X	X	X
1	1	1	0	1

OUPUT						
SW00	SW01	SW02	SW03	Clamper	DO1	DO2
ON	OFF	ON	OFF	ON	0	1
ON	OFF	ON	OFF	ON	0	1
OFF	X	OFF	ON	OFF	1	0
ON	OFF	OFF	OFF	ON	0	1

Table 1: Truth table of the digital control block

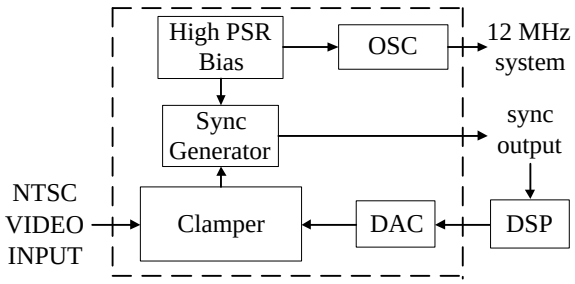

Figure 1: Architecture of the proposed NTSC sync separator

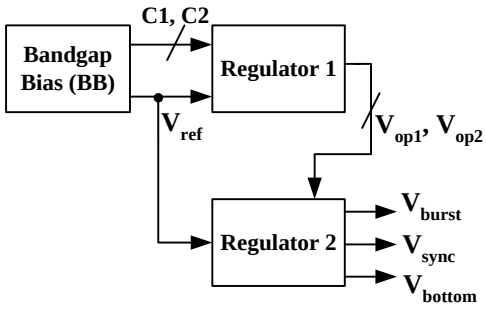

Figure 2: The proposed high-PSR bias circuit

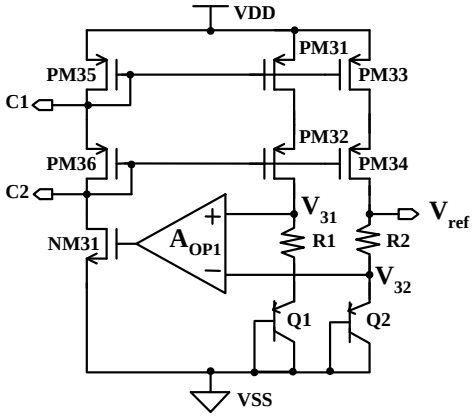

Figure 3: The bandgap reference

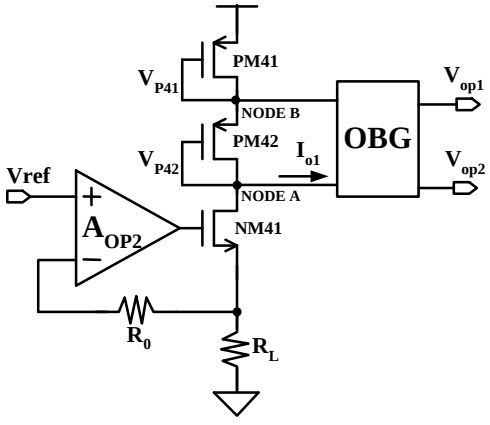

Figure 4: The circuitry of Regulator 1

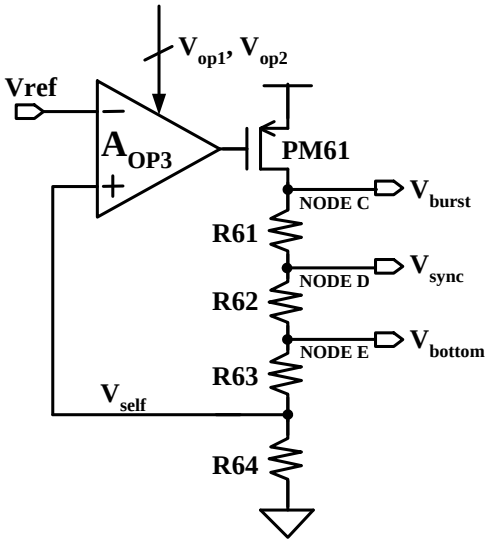

Figure 5: The circuitry of Regulator 2

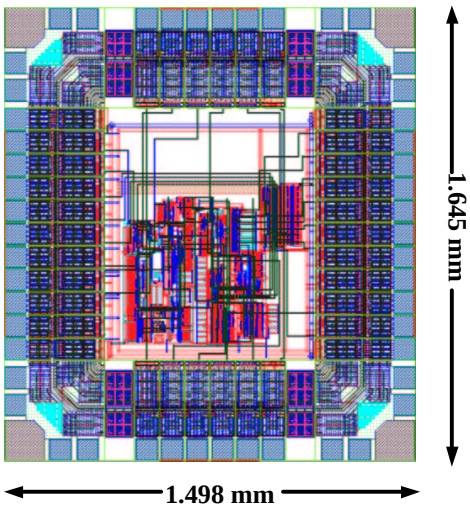

Figure 8: Layout of the proposed sync separator

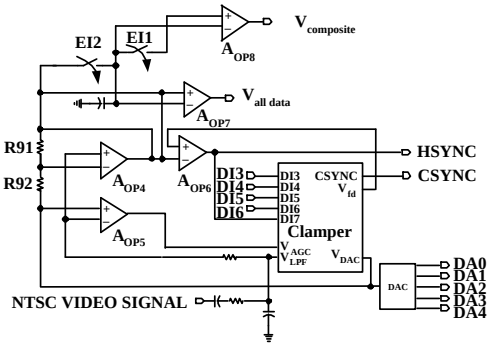

Figure 6: Architecture of the Clamper

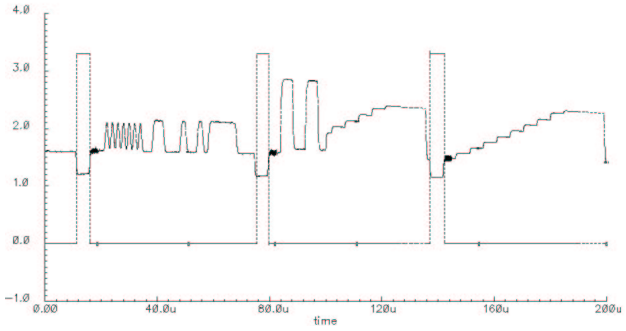

Figure 9: HSYNC post-layout simulation result

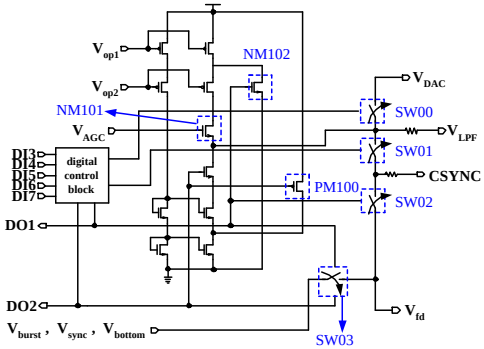

Figure 7: Schemstic of the Clamper

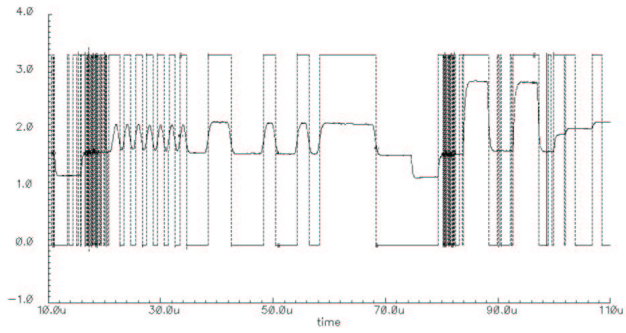

Figure 10: $V_{\text{all data}}$ post-layout simulation result