CLOCK RECOVERY AND DATA RECOVERY DESIGN FOR LVDS TRANSCEIVER USED IN LCD PANELS[§]

Chua-Chin Wang[†], Ching-Li Lee, Chun-Yang Hsiao, and Jih-Fon Huang[¶]

Department of Electrical Engineering
National Sun Yat-Sen University
Kaohsiung, Taiwan 80424
email : ccwang@ee.nsysu.edu.tw

Abstract- **This work presents the design and implementation of a CDR (clock and data recovery) design for LVDS transceiver operations. Instead of using an oversampling scheme which requires a high-speed clock generator, we adopt an interpolation scheme which relaxes the demand of a high-speed PLL with very high precision. A dual-tracking design is proposed to precisely align both edges of a data eye. Hence, the center of a data eye can be optimally sampled. A typical 0.25 μm 1P5M CMOS technology is used to realize the proposed dual-tracking CDR for 7×100 (bit-MHz) LVDS signaling. The post-layout simulation reveals that the worst-case jitter of the sampling clocks is less than 450 ps (peak-to-peak) and 250 ps (rms) at all process corners.**

Index Terms- **LVDS signaling, CDR, dual-tracking, eye diagram, phase interpolation**

I. INTRODUCTION

Regarding the CDR designs for LVDS signaling, there were two major design schemes : oversampling, [2], and interpolation, [1]. The former scheme demands a high frequency PLL[3]. We adopt the phase interpolation design scheme to design the CDR for LVDS signaling circuitry which requires only a PLL possessing the same output frequency with the data frequency. Instead of assuming the eye diagram is symmetric and tracking only one side of the eye as prior works [1], [3]. we use 14-phase clocks to trace and track two edges of an eye, called dual-tracking, to align data sampling at the middle of the eye. Hence, the detection of the data is ensured to be optimal and the BER (bit error rate) is drastically reduced. The proposed CDR is fully complied with the IEEE STD. 1596.3. A typical 0.25 μm 1P5M CMOS technology is used to realize the proposed CDR. The post-layout simulation reveals that the jitter is 450 ps (peak-to-peak) and 250 ps (rms), while the BER is less than 10^{-13}.

§ This research was partially supported by Acer-United Optronics (AUO) Corp. under grant 92A20353 and National Science Council under grant NSC 92-2220-E-110-001 and 92-2220-E-110-004.

† the contact author

¶ Mr. Huang is the section manager of Plasma Display Panel of AUO Corp., Hsin-Chu, Taiwan.

II. DUAL-TRACKING CDR DESIGN FOR LVDS SIGNALING

The architecture of the proposed dual-tracking CDR is shown in Fig. 1.

A. CDR System Architecture

BLOCK-1 (PLL) : Since the transmission bit rate of the required LVDS signaling is 140 to 700 Mbps, we use a phase shifting design in the multi-phase PLL. The PLL receives an external 20 to 100 MHz clock and generates a bank of clocks with 7 different phases, i.e., CLKN_i and CLKP_i, where i = 0, 1, ..., 6, to sample 7 data in one PLL cycle, as shown in Fig. 2.

BLOCK-2 (Eye Edge Finder, EEF) : The data edge generator (DEG) generates pulses corresponding to the edges of the incoming bit stream. We define the pulse width of a single cycle (a.k.a. mark level) as the right eye and the ground portion (a.k.a. space level) as the left eye in this paper. The phase early/late detector (PELD-R) for the right eye samples the current edge and compares with the previous detected edge which was produced at the output of the right-eye phase interpolator (PI-R) and its associative differential-to-single signal converter (DSC-R). On the other hand, the PELD-L, PI-L, and DSC-L executes the same function to the left eye.

BLOCK-3 (Eye Center Generator, ECG) : The locked left and right edges of the eye are respectively denoted by LW0 to LW5 and their complements, and RW0 to RW5 and their complements. These signals are fed into center phase interpolator (CPI) which generates a pair of control signals, i.e., BP0 and BN0, to drive the

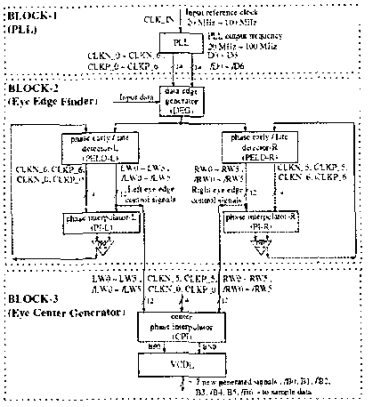

Figure 1: The architecture of the proposed dual-tracking CDR

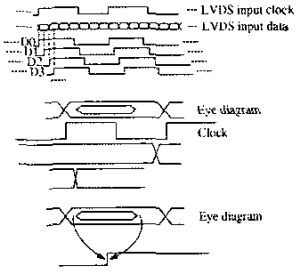

Figure 2: Data flow of the proposed dual-tracking CDR

following 7-stage voltage-controlled delay loop (VCDL). The VCDL, thus, generates 7 sampling pulses aligning the individual centers of the eyes.

B. CDR Data Processing Flow

The entire CDR data processing flow can be illustrated by Fig. 2. A total of 7 data bits are transferred in one LVDS clock cycles. Thus, the PLL in BLOCK-1 locks the LVDS clock and generates 1×7 clocks with the same frequency and equally differentiated phases. The edge-finding of the eye's right edge is summarized as follows.

(R1). PELD-R samples the current edge and compares with the previous detected edge which was produced at the output of PI-R and its associative DSC-R. If the current edge is found to be at the left side of the previously detected edge, then the right edge of the eye is set to be the last detected edge.

(R2). On the contrary, if the current edge is found to be at the right of the previously detected edge, we need to compare the current edge with the output of PI-R. If the current edge lags (that is, falls at the right of the PI-R's output), the right edge of the eye is "locked" by a DFF which is the DFF-R1 in Fig. 3 which in turn disables the advancing of the 6-bit shift register (SR-R). If the current edge leads the PI-R's output and the SR-R is not locked, the SR-R advances by 1 bit to move the next PI-R's output toward the center of the eye.

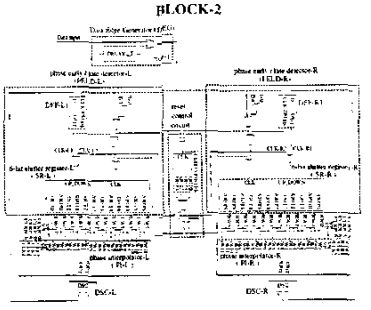

Figure 3: BLOCK-2

(R3). The locked right edge of the eye can only be released by the next detected edge appearing at the left of the PI-R's output.

By dual respect, the edge-finding of the eye's left eye is similar to that for the right edge. As soon as both edges of the eyes are detected, the center of the eye, which is the optimal sampling edge, will be determined by the ECG.

C. Circuit Implementation

PLL in BLOCK-1 : Referring to Fig. 4, the PLL comprises a Bias Generator, a Replica Bias, a CP (charge pump) containing two individual charge pumps which controls the voltages, VP and VN, fed into the 7 voltage-controlled delay cells. The 7 voltage-controlled delay cells constitute a VCO. The differential output pair of each delay cells, namely CLKN_i and CLKP_i, where i = 0, 1, ..., 6, are respectively converted into a pair of single-ended voltage pulse trains, i.e., Di and /Di, where i = 0, 1, ..., 6 by 7 DSCs . Notably, Di and /Di are complementary to each other. The schematic of the DSC is given in Fig. 5.

EEF in BLOCK-2 : The EEF is composed of the reset control circuit, DEG, the right edge detector consisting of PELD-R, SR-R, PI-R and DSC-R, and the left edge detector including PELD-L, SR-L, PI-L and DSC-L, as shown in Fig. 3. The schematic of DSC-R and DSC-L is identical to the DSC in Fig. 5. SR-R and SR-L are typical shift registers. What left to be addressed is the PI-R, PI-L and the reset control circuit.

PI (phase interpolator) : In fact, all of the PI-R, PI-L and CPI in BLOCK-3 are identical. Fig. 6 shows the schematic of the PI. CLK1 and /CLK1, CLK2 and /CLK2 are two pairs of differential signals, while W_i and

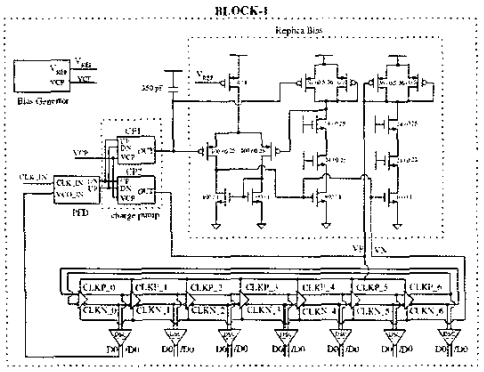

Figure 4: BLOCK-1

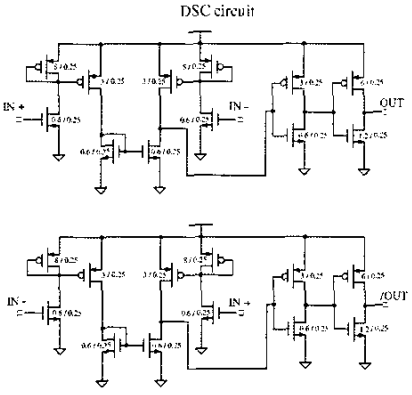

Figure 5: The schematic of DSC

$/W_i$, where $i = 0, \ldots, 11$, are current control signals. More W_i's are 1's, larger current will be induced via the VP-controlled current sources and the VN-controlled current sinks. Hence, the transition at the OUT and /OUT will be faster. For instance, CLK1 and /CLK1, CLK2 and /CLK2 of PI-L are respectively coupled to CLKN_6 and CLKP_6, CLKP_0 and CLKN_0. Meanwhile, the W_i's are coupled to the outputs of the 6-bit SR-L as the lower right part of Fig. 3. Fig. 7 shows the simulation results that curve A, B, C, D, E, respectively, denotes the phase slicing given 5, 4, 3, 2, 1, of 1's in the SR-L between curve $< 1 >$ and $< 2 >$. It should be noted that curve $< 0 >$, $< 1 >$, $< 2 >$, $< 2 >$, etc., are the generated CLKP_0, CLKP_1, CLKP_2, CLKP_3, etc. of the PLL. Hence, the duration between CLKP_0 and CLKP_1 can be divided into 6 phase intervals. So are the rest of the generated clocks.

reset control circuit : To avoid a possibility that an edge of incoming data completely falls outside the range of the eye which will lead to at least one of the phase interpolators can not align its corresponding edge with

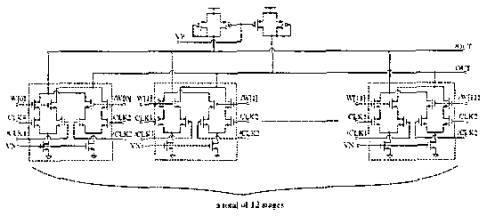

Figure 6: The schematic of a PI

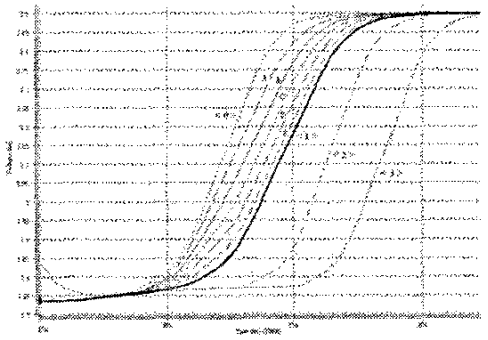

Figure 7: The phase interpolation between two clock edges

the data edge, a reset control circuit comprising a 4-bit counter as shown in Fig. 3 is required to resolve this problem. After counting 15 cycles and PI-R or PI-L can not spot the correct position of the current, a "1" and a "0" are generated and propagated to the UP_DOWN pin of SR-R and SR-L, respectively, via CLK-R2 and CLK-L2. The former forces the PI-R to shift its range to the right, i.e., widen its searching range. On the other hand, the "0" at the UP_DOWN of SR-L makes the PI-L shift its range to the left. The entire scenario is shown in Fig. 8.

VCDL in BLOCK-3 : Referring to Fig. 9, the CPI receives a total of 24 signals delivered by SR-R and SR-L, including RW_i and $/RW_i$, and LW_i and $/LW_i$, where $i = 0, \ldots, 5$. They denotes where the right and left edges of the eye are positioned. What difference between CPI and PI-R, PI-L is that CPI is used to generate sampling pulses.

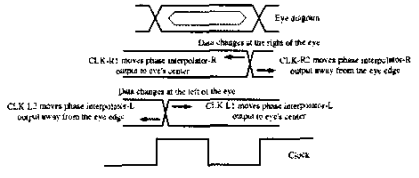

Figure 8: The dual-tracking operations

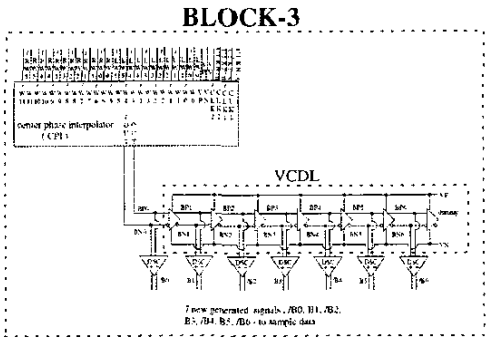

Figure 9: BLOCK-3

Thus, its input clocks must be two phase pitches apart, e.g., using CLKP_5 and CLKN_5, CLKP_0 and CLKN_0, not like those CLKN_6 and CLKP_6, CLKP_0 and CLKN_0 used in PI-L. A VCDL (voltage-controlled delay line) which is identical to the VCO in the PLL. Notably, a dummy cell should be added at the end of the VCDL to equalize the load at the output of each stage. A total of 7 sampling pulses at the output of the 7 DSCs are generated, /B0, B1, /B2, B3, /B4, B5, and /B6.

III. Simulation and Implementation

The proposed CDR is implemented by TSMC (Taiwan Semiconductor Manufacturing Company) 0.25 μm 1P5M CMOS technology to verify the performance. Notably, all of the process corners : [0°C, +100°C], (SS, SF, TT, FS, FF) models, and VDD±10%, are simulated. The layout of the proposed CDR is shown in Fig. 10. Fig. 11 shows the output waveforms to reveal the advantage of the proposed CDR. On top of the figure, it is a normal data and sampling edge at 100 MHz. By contrast, if the data is delayed or interfered, the B0 generated at BLOCK-3 will align with the edge of the delayed data bit. Then, B1 becomes the new sampling pulse to latch the data correctly. The characteristics of the proposed dual-tracking CDR is summarized in Table .

IV. Conclusion

We propose a novel dual-tracking CDR design by detecting both edge of an eye such that the center of the eye can be precisely sampled. The proposed CDR is immune to the asymmetricity of data eys. Besides, the phase interpolation design scheme is adopted to avoid the necessity of a very high sampling clock to relax the jitter accumulation problem.

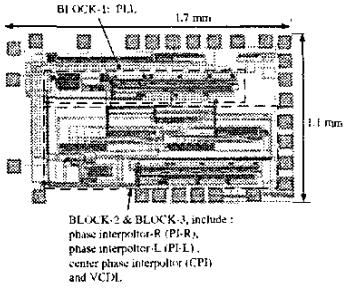

Figure 10: Layout of the proposed dual-tracking CDR

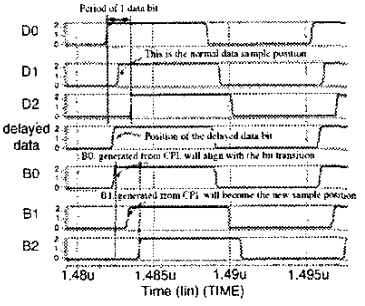

Figure 11: Post-layout simulations of the proposed dual-tracking CDR

Table 1: Characteristics of The Proposed Dual-Tracking CDR

	STD 1596.3	Our Design
VDD	2.2 ~ 2.8 V	2.2 ~ 2.8 V
input clock	25 ~ 100 MHz	25 ~ 100 MHz
max. current	20 mA	20 mA
jitter (p-to-p)	N/A	450 ps
jitter (rms)	N/A	250 ps
area	N/A	1.7×1.1 mm^2

References

[1] M.-J. E. Lee, W. J. Dally, J. W. Poulton, P. Chiang, and S. E. Greenwood, "An 84-mW 4-Gb/s clock and data recovery circuit for serial link applications," *Digest of Techinical Papers of 2001 Symp. on VLSI Circuits*, pp. 149-152, June 2001.

[2] S.-H. Lee, M.-S. Hwang, Y. Choi, S. Kim, Y. Moon, B.-J. Lee, D.-K. Jeong, W. Kim, Y.-J. Park, and G. Ahn, "A 5-Gb/s 0.25-/spl mu/m CMOS jitter-tolerant variable-interval oversampling clock/data recovery circuit," *IEEE J. of Solid-State Circuits*, vol. 37, no. 12, pp. 1822-1830, Dec. 2002.

[3] B. Razavi, "Chanllenges in the design high-speed clock and data recovery circuits," *IEEE Communication Magazine*, vol. 40, no. 8, pp. 94-101, Aug. 2002.

[4] "IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)," 1596.3 SCI-LVDS Standard, IEEE Std. 1596.3-1996, 1994.