1.0 GBPS LVDS TRANSCEIVER DESIGN FOR LCD PANELS[§]

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ABSTRACT

LVDS has become a popular choice for high-speed serial links in large-sized display units. This work presents the design and implementation of I/O interface circuits for Gbps operation which is fully complied with the IEEE STD. 1596.3 (LVDS). A step-down voltage regulator is employed to reject the noise coupled in the system power supply. A CMFB (common mode feedback) circuitry is utilized in the transmitter to stabilize the common mode voltage in a pre-defined range. By contrast, a regenerative circuit which provides a positive feedback loop gain between the preamplifier and the output buffer in the receiver. A typical 0.25 μm 1P5M CMOS technology is used to realize the proposed LVDS transceiver. The post-layout simulation reveals that the data rate is 1.0 Gbps at all process corners.

Keywords : LVDS signaling, regulator, positive feedback, CMFB, high-speed D-latch

1. INTRODUCTION

A bottle neck in the digital transmission of chips via longs wires on PCB is the I/O cells which are responsible for voltage level shifting and ESD protection. Besides, long wires are huge R and C load to the chips. The I/O cells, namely I/O pads, are asked to supply sufficient current to drive these large loads. Hence, not only is the pad area large, but also the power consumption occupied a great portion of the overall power. Most of prior CMOS I/O cells utilized very large area to accommodate large driving transistors as well as large passive elements [2]. The side effect is more power dissipation. Ever since the booming of LCD panels, the LVDS [7] become one of the most promising solutions to resolve the massive data communication between a host processor with memories and a flat panel [2], [4], [5], [6], [8]. The LVDS signaling technology provides a low-power, and low-voltage alternative to other high-speed I/O designs, e.g., ECL. One of the major goals of the LVDS signaling besides the mentioned low power and high speed is aimed at minimizing the PCB complexity and the production cost, particularly for display panels. Hence, external discretes as well as voltage references should be avoided together with wafer-level and board-level trimming. We present the design and implementation of I/O interface circuits for Gbps operation which is fully complied with the IEEE STD. 1596.3 (LVDS signaling). At the transmitter (Tx), a step-down voltage regulator is employed to isolate the noise coupled in the system power supply. A CMFB (common mode feedback) circuitry is utilized to stabilize the common mode voltage in a pre-defined range. At the receiver (Rx), a regenerative circuit which provides a positive feedback loop gain between the preamplifier and the output buffer in the receiver such that a high differential gain of input voltage signals is achieved without any loss of bandwidth. A typical 0.25 μm 1P5M CMOS technology is used to realize the proposed LVDS transceiver. The post-layout simulation reveals that the data rate is 1.0 Gbps at all process corners.

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2. LVDS LINK DESIGN

A typical LVDS link is shown in Fig. 1. The required communication interface is summarized as : If the in input voltage at the Tx is low, a differential pair of voltage signals are generated, V_{oa} and V_{ob}, and $V_{oa} < V_{ob}$. If the input voltage is high, then $V_{oa} > V_{ob}$.

2.1. Transmitter (Tx)

The proposed Tx composed of a step-down regulator and a driver is shown in Fig. 2. The regulator supplies the required voltage supply, V_{dc}, for the driver. Hence, the coupling noise as well as the variation of the external power supply is isolated from the driver.

Fig. 3 reveals of the schematic of the proposed driver. The current switch constituted by MD21, MD22, MD23, and MD24 is controlled by TX_IN1 and TX_IN2. (Notably, TX_OUT1 and TX_OUT2 are identical to V_{oa} and V_{ob}, respectively, in Fig. 1.) TX_OUT1 and TX_OUT2 are the outputs coupled to the transmission lines.

Case 1 TX_IN1 = 1, TX_IN2 = 0 : MD22 and MD23 are turned on, while MD21 and MD24 are off. Thus, TX_OUT1 is pulled high, TX_OUT2 is pulled down to ground.

Case 2 TX_IN1 = 0, TX_IN2 = 1 : MD22 and MD23 are turned off, while MD21 and MD24 are on. Thus, TX_OUT1 is pulled down, TX_OUT2 is pulled high.

The feature of the proposed transmitter is the CMFB in Fig. 3. A stable common mode voltage (V_{CM}) is required by the LVDS standards [7]. A prior design to achieve this goal is to use a voltage divider composed of two large resistors ($\approx$ MΩ) between TX_OUT1 and TX_OUT2, e.g., [2]. The reason why the large resistors are used is to reduce the currents thereon. However, the large resistors demand large die area or off-chip discrete components. Either one is hostile to the cost reduction.

By contrast, we intend to use a CMFB (common mode feedback) scheme to resolve the problem. Referring to Fig. 3, TX_OUT1 and TX_OUT2 are respectively compared to a V_{REF} by two differential amplifiers consisting of M21 and M22, and M23 and M24. Assume TX_IN1 = 1 and TX_IN2 = 0. The current via MD23 and MD22 is I, the V_{CM} can be derived to be the following equality.

$$V_{CM} = (V_{\text{TX\_IN1}} - V_{TH,\ \text{MD23}}) - \left(\sqrt{\frac{2 \cdot I}{k'_{\text{MD23}} \cdot (\frac{W}{L})_{\text{MD23}}}} + \frac{I}{2} \cdot R_{term}\right), \quad (1)$$

where k'_{MD23} and $V_{TH,\ \text{MD23}}$ are the transconductance parameter and threshold voltage of MD23, respectively, $(\frac{W}{L})_{\text{MD23}}$ is the aspect ratio of MD23, R_{term} is the termination resistance of the transmission lines.

The target process of the proposed design is 0.25 μm CMOS process with 2.5V power supply. Hence, the V_{CM} is chosen to be 1.2V, which is the required V_{REF}. After taking the process parameters into the calculation of Eqn. (1), the currents via MN21 and MN22 are 35 μA, while the current in the current mirror constituted by MP23 and MN23 is estimated to be 0.35 mA. Besides, the driver stage current in MPN and MDN is 3.5 mA. The operation of the feedback loop is as follows.

1). As soon as TX_OUT1 and TX_OUT2 drops to cause V_{CM} to be smaller than V_{REF}, the current via MP21 is reduced which in turn decreases the current in the MDN and MPN pair. Thus, V_{CM} will be increased.

2). On the other way around, if TX_OUT1 and TX_OUT2 is pulled high to cause V_{CM} larger than V_{REF}, the current of MP21 is increased such that the current in the MDN and MPN pair is also increased. Hence, V_{CM} will be dropped.

Regarding the noise-rejecting voltage regulator in Fig. 2, Fig. 4 shows the details. It is composed of an OPAMP, i.e., OP_1, and a bandgap voltage reference. The schematics of the voltage reference and the OPAMP are respectively given in Fig. 5 and Fig. 6.

2.2. Receiver (Rx)

The bottleneck of the Rx design for LVDS is the sensing speed of the incoming data pulses. We propose a novel design for the LVDS Rx in Fig. 7. The preamplifier is in charge of the sensing speed, i.e., high bandwidth, at the cost of low gain. The following regenerative circuit is used to compensate the low gain problem by providing a positive feedback loop gain to magnify the sensed differential signals. Besides, owing to the positive feedback loop, the short transient response time makes the delay very small. The last stage of the proposed design is the output buffer which is utilized to restore the differential signals to the full swing for the following digital circuitry.

Fig. 8 shows the schematic of the proposed Rx design in which a noise-rejecting regulator composed of a bandgap voltage reference and an OPAMP is used to supply a stable 0.8V BIAS and a 2.5 V voltage source (Vdc) to the preamplifier and the regenerative circuit. The regenerative circuit is nothing but a high-speed D latch.

preamplifier : As shown in Fig. 9, the preamplifier consists of two OTAs (operational transconductance amplifier) which converts and amplifies the incoming RX_IN1 and RX_IN2 to a differential pair of signals, VP and VN.

latch : The VP and VN are respectively coupled to the LI1 and LI2 of the latch in Fig. 10 [3]. M81 to M86 are the latch circuitry. M8B is the tail current sink. M811 to M814 and M821 to M824 respectively constitute two current source inverters to increase the swing of LO1 and LO2. Thus, the output voltage at LO1 and LO2 is capable of driving the output buffers.

3. SIMULATION AND IMPLEMENTATION

The proposed I/O cell is implemented by TSMC 0.25 μm 1P5M CMOS technology to verify the performance. Notably, all of the process corners : [0°C, +100°C], (SS, SF, TT, FS, FF) models, and VDD±15%, are simulated. Die photo of the proposed Tx and Rx on silicon is shown in Fig. 11. Fig. 12 shows the output waveforms of the transmitter at the 3 corner conditions given a 1.0 GHz data input. Table 1 summarize the V_{CM} at different corners.

On the other hand, Fig. 13 shows the simulation result of the receiver output given the VDD = 3.3 V and Vdc = 2.5 V coupled with a noise of which amplitude is 10% of input signal amplitude. It is obvious that the output waveforms of the receiver at RX_OUT1 and RX_OUT2 are fully restored to the 2.5 V swing for the operation of any further digital processing. We have compared the performance of our proposed I/O cell with two prior designs in Table 2. Not only do we have the maximum operating clock rate, the proposed design consumes the least area on silicon.

4. CONCLUSION

We propose a novel LVDS TX and Rx cell design by taking advantage of the CMFB scheme, the noise-rejecting regulator, the preamplifiers, and the D latch to achieve high speed and small area. Besides, the sacrifice in terms of the power dissipation is obscure. Thorough post-layout simulations confirm the superiority of our design.

5. REFERENCES

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corner (model, temp, VDD)	V_{CM} (V)
SS 0°C 2.805 V	1.200
SS 100°C 2.805 V	1.215
SS 0°C 3.795 V	1.150
SS 100°C 3.795 V	1.210
FF 0°C 2.805 V	1.270
FF 100°C 2.805 V	1.300
FF 0°C 3.795 V	1.270
FF 100°C 3.795 V	1.300

Table 1: V_{CM} at PVT corners

max. figure	[2]		[1]		ours	
	Tx	Rx	Tx	Rx	Tx	Rx
load (pF)	10	1	10	N/A	8	5
freq. (GHz)	1.0	0.6	0.4	0.256	1.0	1.0
delay (ns)	0.8	1.4	N/A	N/A	0.3	0.6
area (mm^2)	0.175	0.081	N/A	N/A	0.026	0.040

Table 2: Performance comparison

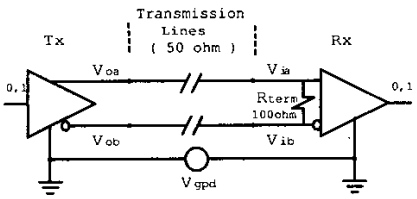

Figure 1: LVDS link

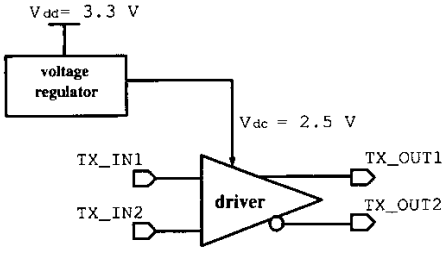

Figure 2: The proposed LVDS Tx

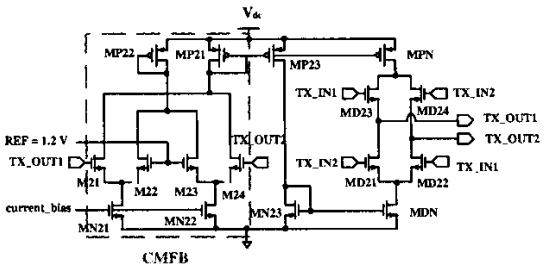

Figure 3: The schematic of the Tx driver

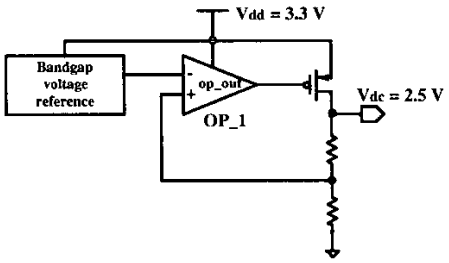

Figure 4: Noise-rejecting regulator

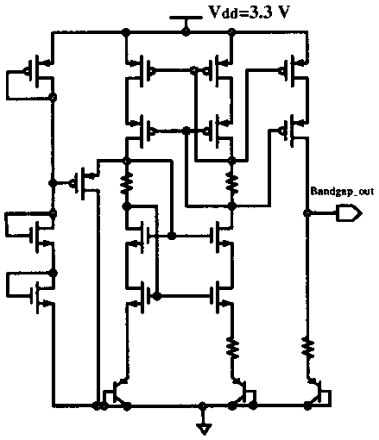

Figure 5: Bandgap voltage reference

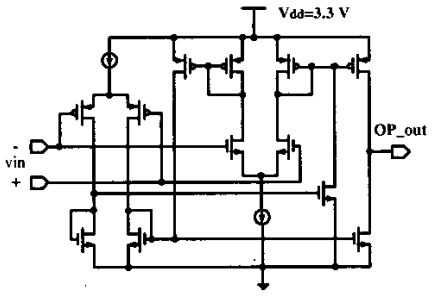

Figure 6: The OP_1 schematic

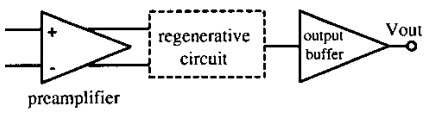

Figure 7: The proposed LVDS Rx

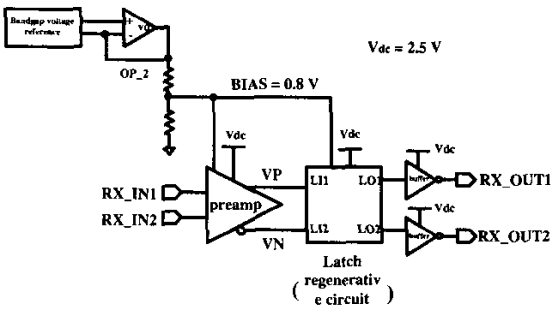

Figure 8: The schematic of the proposed LVDS Rx

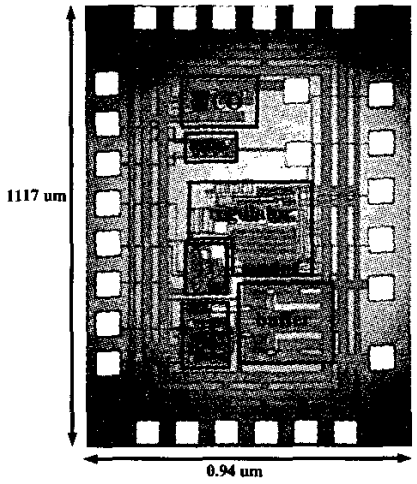

Figure 11: Die photo of the proposed LVDS transceiver

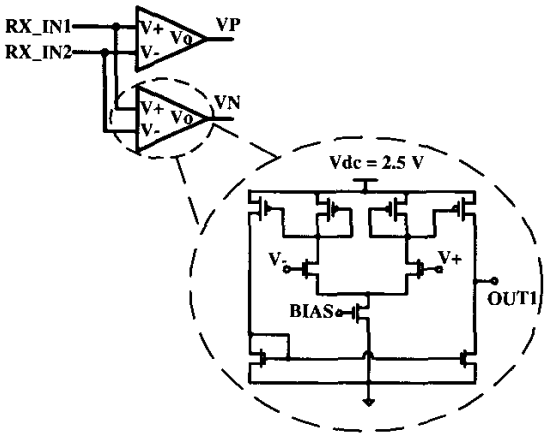

Figure 9: The schematic of the preamplifier

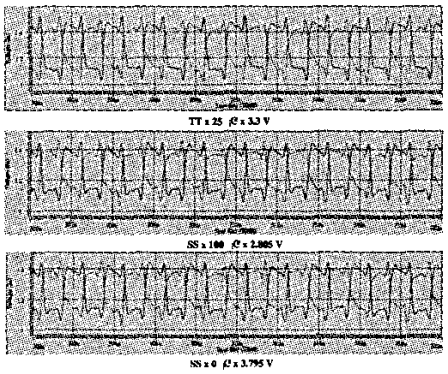

Figure 12: Simulation results of the Tx given a 1.0 Gbps data input

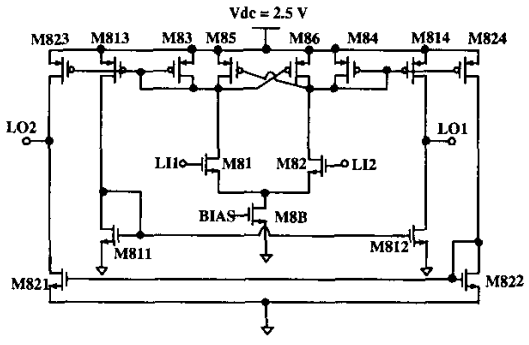

Figure 10: The schematic of the regenerative circuit (latch)

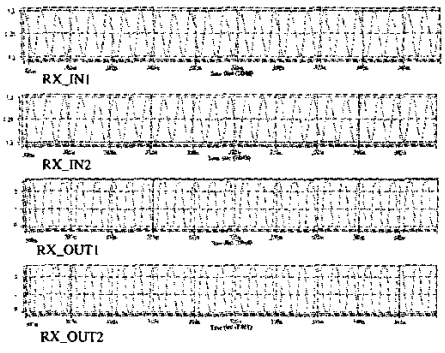

Figure 13: Simulation results of the Rx given a 1.0 Gbps data input