POWER-AWARE PIPELINING DESIGN OF AN 8-BIT CLA USING PLA-STYLED ALL-N-TRANSISTOR LOGIC[§]

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Abstract- **A high speed and low-power 8-bit carry-lookahead adder (CLA) using two-phase all-N-transistor (ANT) blocks which are arranged in a PLA design style with power-aware pipelining is present. The pull-up charging and pull-down dis-charging of the transistor arrays of the PLA are accelerated by inserting two feedback MOS transistors between the evaluation NMOS blocks and the outputs. The analysis of the area (transistor count) tradeoff is also provided in this work. The output of the addition of two 8-bit binary numbers is done in 2 cycles. The proposed power-aware pipelining design methodology takes advantage of shutting down the processing stages with identical inputs in two consecutive cycles. Not only is it proved to be also suitable for the long adders, the power consumption is drastically reduced by at most 50% at every process corner.**

Index Terms- **power-aware, ANT, single clock, CLA, pipeline**

I. INTRODUCTION

Fast adders are key elements in digital circuits, including multipliers, and DSP chips. Many efforts have been focused on the improvement of adder designs [3], [5], [6]. CMOS dynamic logic has been recognized as one of the promising options to challenge the GHz operations for the adder design [1], [2]. Other logics suffer from different difficulties which were addressed in [5]. However, the major trade-off of these prior GHz logic circuits is the high power consumption which is not a tolerable price to pay in recent mobile technologies. We, hence, propose a power-aware PLA-like structure using our high-speed all-N-transistor (ANT) function block [5], [6], [7]. An 8-bit CLA using ANTs which are arranged in the power-aware PLA-like structure and triggered by a single clock is implemented to verify the power reduction as well as the preservation of high speed. The major advantage of the power-aware design methodology is that it is robust regardless of long data words, e.g., 64-bit binary data. The 8-b CLA using PLA-styled ANT logic is simulated to be fully functional up to 1.0 GHz at 2.5 V power supply, while the correct result of addition is available after 2 cycles. The power reduction is simulated to be almost 50% compared to the prior works.

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II. POWER-AWARE HIGH-SPEED 8-BIT CLA

A. All-N-Transistor (ANT) Function Unit

A modified dynamic logic, ANT [7], has been proposed in Fig. 1. The feature of this modification is the feedback transistor pair, P3 and N3, between the evaluation block and the output.

1). When $clk = 0$, P1 is on and the gate of P2 is precharged to be Vdd. Then, P2 is off and N4 is off. This makes the output to stay at the previous state.

2). When $clk = 1$ and the N-block is evaluated to be "pass", the charge at node a should be ground through the N-block and N1 theoretically. Note that N4 is on and N2 is also on at the beginning. If the previous state of output is high, then N3 will be turned via N4. This means that N3 provides another fast discharging path for the charge at node a. When the voltage at node a is dropped below the threshold voltage of PMOS, P2 and P3 start to be on. The output will then be charged to be Vdd via paths P2 and P3-N4.

3). When $clk = 1$ and the previous state of the output is low and the N-block is evaluated to be "pass," the voltage at node a starts to drop. When $V_a - V_{dd} > V_{tp}$, P3 will be on such that the gate of N3 will be charged to be V_{dd}. Not only the charge at node a will be discharged faster, but also the output will be charged to high via P2 and N4.

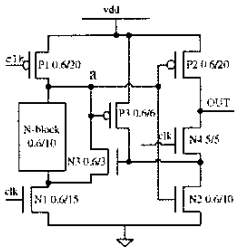

Figure 1: ANT logic

4). When $clk = 1$ and the N-block is evaluated to be "stop", the charge at node a should be kept if the previous state of output is low. There will be no discharging path for node a because N3 will be off via N4. If the previous state is high, the output will be ground via N4 and N2 before the voltage at node a starts to drop.

Summarized from 2). and 3). in the above, the output will be high when the N-block is evaluated "pass", i.e., "1", during $clk = 1$. By 4), the output will be low when the N-block is evaluated "stop", i.e., "0", during $clk = 1$. The function of ANT logic block, thus, is conclusively correct and non-inverting. Restated, P3 and N3, respectively, provide an extra charging path and an extra discharging path such that the speed of the evaluation can be accelerated.

In addition to the previous discharging path problem, one of the reasons why other high-speed logic can not run correctly given clocks with short rise time or fall time is that the size of each transistor can not be tuned properly. Both [1] and [2] intrinsically possess this shortcoming. The sizing problem of the transistors in the ANT besides those in the N-block drastically affect the speed. We have been proceeded several simulations to find out the best figure of merit for the sizing of each transistor in Fig. 1 using TSMC (Taiwan Semiconductor Manufacturing Company) 0.25 μm 1P5M CMOS technology.

B. *PLA-Styled 8-Bit CLA Design*

The formulation of a 8-b CLA is represented by the following equations:

$$\begin{aligned} S_i &= C_{i-1} \bigoplus P_i \\ C_i &= G_{i-1} + P_{i-1}G_{i-2} + P_{i-1}P_{i-2}G_{i-3} + \\ &\quad \ldots + P_{i-1}P_{i-2}\ldots P_1P_0C_0 \end{aligned} \quad (1)$$

where $A_i, B_i, i = 0...7$, are inputs, and P_i, G_i are *propagate* and *generate* signals, respectively, $P_i = A_i \bigoplus B_i$, $G_i = A_i \cdot B_i$. If the P_i's and G_i's are produced by combinatorial logic function blocks before they are fed into the function blocks for S_i's and C_i's, then Eqn. (1) implies that a two-level AND-OR logic function block is a possible solution to achieve high speed operations. Thus, the PLA-styled design is suitable for such a function block. A conceptual PLA-styled design for CLA is shown in Fig. 2. A typical PLA consists of an AND array and an OR array. It is well known that the series NMOS in the evaluation block of NAND or AND gates will produce long discharging delays which subsequently slow down the entire circuit. We can take advantage of the non-inverting feature of the ANT logic to utilize a NOT-OR-NOT-OR configuration instead of the typical AND-OR style, where the two OR planes are made of ANT logic blocks. Meanwhile, it can also minimize the series transistor count in the evaluation block. The OR array is made of the ANT logic with a predefined evaluation block. The inputs to the first OR array is the inverted P_i's (propagate) and G_i's (generate) signals which are also produced by other ANT logic units as shown in Fig. 3. Note that we define the propagate signals in a different way from the traditional $P_i = A_i + B_i$ because the $P_i = A_i \bigoplus B_i$ can be reused to generate the sum term, i.e., S_i.

C. *Speed and Area Analysis*

Speed : The critical path of an adder resides on the generation of carry signals, i.e., C_7 in the 8-bit adder. After the binary data are ready, the generation of P_i's and G_i's by using the ANT logic takes the high half of a full cycle. That is, the results of GP blocks will be ready when the clk is low. The inverted P_i's and G_i's will then be fed into the first OR plane of the ANT-based PLA. The inverted outputs of the first OR plane will be presented to the second OR at the high half of the second cycle. The final C_i's results then are ready in the low half of the second cycle. Right after the generation of every C_i's, they are inverted and fed into the S_i's function blocks. Another half cycle then is required to produce all of the S_i's. The final result will be latched after 2 cycles.

Area : As for the transistor count of the PLA-styled implementation for CLA using ANT logic, an analytic form is obtained after careful derivations. In short, if an n-bit CLA is to be realized by our methodology, the transistor count can be computed as : $T_{total} = \frac{1}{6}(n + 1)(n + 2)(n + 3) + 5n(n + 1) + 50n + 3$

D. *Power-Aware Pipelining*

A simple thought to improve the power efficiency is to "deny" the current fed into those function units of which the input data are identical between two consecutive operation cycles. The dynamic power, hence, of CMOS logic elements will be drastically reduced. Take the ANT block shown in Fig. 1 as an example. Assume the N-block is composed of two cascaded NMOS tran-

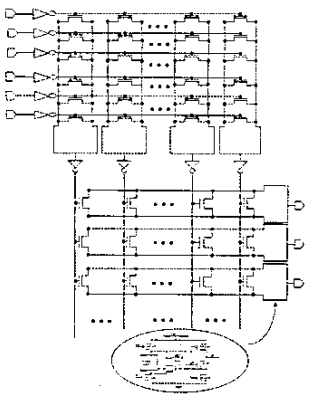

Figure 2: PLA-styled CLA

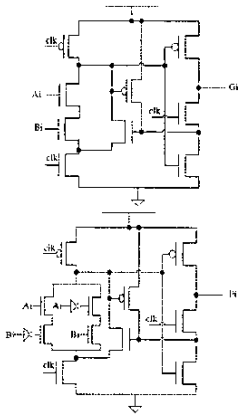

Figure 3: GP block

sistors to constitute an AND gate. The probability of the data inputs of two consecutive operation cycles is 25% which implies a significant portion of power consumption. Hence, a monitoring circuitry as shown in Fig. 4 is proposed to resolve the low power demand. The power-aware pipelining (PAP) design is composed of three blocks : an ATD, a 2-bit counter, and a voltage regulator. Four cascaded inverters and an XOR gate consist of a simple ATD (asynchronous transition detector). If any data bit flips its state, a strobe will be generated at the output of the XOR which consequently enable the 2-bit counter to tick for two clocks which are enough for the ANT unit to complete its computation. As soon as the two clocks are elapsed, the feedback circuitry of the counter clear the register cells therein to wait for the next enabling strobe. Notably, Q_0 is used as the clock signal of the following ANT unit. When the counter is disabled, the Q_0 is kept at high to disable the current source in the following ANT unit such that its output state remains.

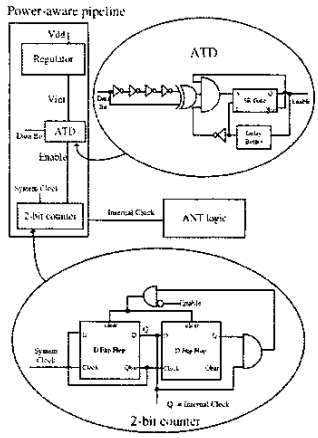

Figure 4: Power-aware circuitry

However, the most critical part of the proposed PAP is the sensitivity of the strobe duration with respect to the power variation. One of the most efficient approach to avoid the unstable power supply is to employ step-down bandgap-referenced voltage regulators to supply a temperature independent reference voltage, V_{ref}, to the rest of the circuitry [4]. Referring to Fig. 5, the regulator is composed of A_{OP3}, PM61, and a resistor string. The generated internal voltage for the PAP is a very stable $V_{int} = V_{dd} - V_{thp}$.

III. Performance Simulations and Comparison

The data flow block diagram of the proposed 8-bit power-aware PLA-styled ANT-based CLA is shown in Fig. 6. The detailed schematic and layout of the CLA implemented by TSMC 0.25 μm 1P5M CMOS process shown in Fig. 7 and 8, respectively. An example of the output waveform of 8-bit power-aware PLA-styled CLA using ANT logic shown in Fig. 9 illustrates that the result of an addition appears after two cycles given the clock = 1.0 GHz. The characteristics of the proposed proposed power-aware CLA is tabulated in Table 1.

In order to reveal the power-saving advantage of the proposed power-aware design, two 2-input ANT-based OR gates are respectively implemented by [7] and the proposed design using the same CMOS process. The power reduction of the power-aware design is shown in Table 2. The simulations are carried out by HSPICE Monte Carlo method with sweep = 30.

IV. Conclusion

We propose a power-aware high speed PLA-styled ANT logic design for the adders' implementation. Not only the correctness of the function in the giga hertz range is preserved, but also the power dissipation is

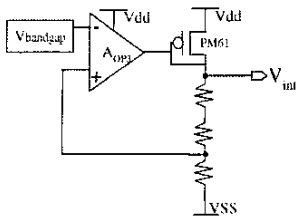

Figure 5: Regulator in the power-aware circuitry

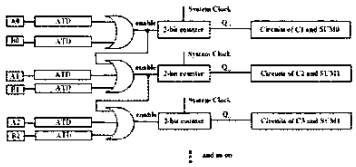

Figure 6: Data flow block diagram of the proposed CLA

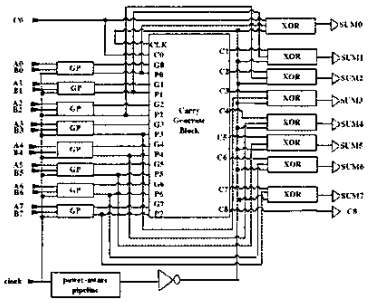

Figure 7: Schematic of the proposed CLA

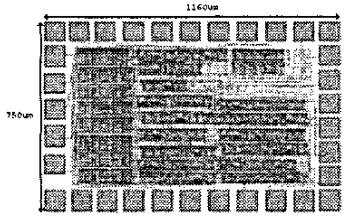

Figure 8: Layout of the proposed CLA

reduced. The PLA-styled ANT-based structure using only one clock makes the result of an 8-b adder appear in 2.0 cycles (ns if the 1.0 GHz clock is used), or a hierarchical 64-b adder in 4.0 cycles.

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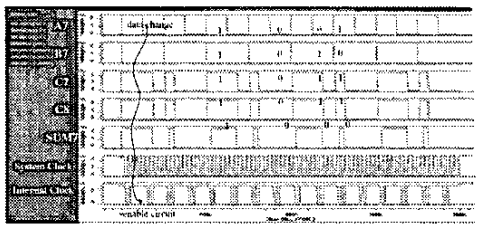

Figure 9: Post-layout simulation result

Table 1: CHARACTERISTICS OF THE PROPOSED PROPOSED POWER-AWARE 8-BIT ADDER

	proposed CLA
system clock	1.0 GHz
input data rate	100 - 500 MHz
avg. power	7.5 mW@500 MHz
area	$1.16 \times 0.75 mm^2$
transistor count	1026

Table 2: POWER REDUCTION BY USING THE POWER-AWARE CIRCUITRY

period	[7]	power-aware	reduction
50 ns	35.295 mW	16.326 mW	51%
100 ns	34.125 mW	10.923 mW	68%
200 ns	34.472 mW	7.628 mW	78%

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