A C-LESS ASK DEMODULATOR FOR IMPLANTABLE NEURAL INTERFACING CHIPS[§]

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ABSTRACT

Various implantable micro-stimulators have been proposed for clinical applications in recent years. Most of the no-battery implanted devices can be powered by a transcutaneous magnetic coupling, which basically utilizes an external transmitter coil to power and communicate with the implanted device. Reducing chip area of the implanted device is the key to any field application. We propos a C-less (no capacitor) area-saving ASK demodulator in this work. Besides, the power regulator design is another task to conquer because of the low-efficient RF induced power. Therefore, a complete power regulator supplying a stable 3.3V VDD is also present.

Keywords : implantable devices, neural interface, micro-stimulator, wireless transmission, regulator

1. INTRODUCTION

The implantable stimulator is one of the recent major medical reaserch topics. It is widely used in ladder leakage control [2], muscle nerve stimulation [5], and Cochlear implants [1]. The implanted device can be powered by a transcutaneous magnetic coupling method using an external transmitter coil to power and communicate with the implanted devices. One of the most important issues for implantable devices is the chip area. Another one would be whether there is an internal stable power supply. Most of the prior implanted devices adopted ASK (amplitude shift keying) modulation because its simplicity. However, those prior designs for the ASK demodulator in implanted devices, [6], [7], [8], contained a large capacitor, which either occupies a huge area in the SOC (system-on-chip) chip or becomes as discrete component on a PCB. By contrast, the proposed ASK demodulator design contains no capacitor which leads to a much smaller area. Meanwhile, since the internal power is generated by the RF induced signal, a supply and temperature independent regulator is required to ensure the functionality of the system operation. The dropout of the proposed power regulator is estimated to be 0.7V at a stable 3.3V VDD output for the core circuit. The entire circuits are implemented by TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 2P4M CMOS technology.

[§] This research was partially supported by National Science Council under grant NSC 92-2218-E-110-001 and National Health Research Institutes under grant NHRI-EX93-9319EI.

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2. C-LESS ASK DEMODULATOR AND POWER REGULATOR

The infrastructure of the entire micro-stimulator system is given in Fig. 1. The external control module includes PC, class E amplifier and transmitter coil. Amplitude shift keying (ASK) modulation protocol is employed to transfer the external control data and power to the internal stimulation chip by the class E amplifier. An on-chip power regulator is required to supply a stable VDD output voltage to the internal core by regulating the a power generated by the on-board coupling coils. We propose a C-less ASK demodulator and power regulator circuit to carry out the decode of the external data and the power.

2.1. On-chip C-less ASK demodulator

The data flow of C-less (capacitor-less) ASK demodulator is shown in Fig. 2, while the entire circuit is given in Fig. 3. The proposed design is divided into three parts, which are an envelope detector, a threshold detector, and a load driver.

1). envelope detector: Not only the supply-independent bias circuit locks the DC level, it also can trace the voltage divider's output envelope. PM103 provides a current through PM102 and NM101 to ground upon start-up. According to [3], if we ignore the body effect, then

$$I_{out} = \frac{2}{\mu_n C_{ox} (\frac{W}{L})_{NMOS}} \cdot \frac{1}{R_S^2} (1 - \frac{1}{\sqrt{k}}), \quad (1)$$

where μ_n is electron mobility, C_{ox} is gate oxide capacitance per unit area, k is a multiple of NM102 to

NM101. It shows that the circuit can provide a stable output current, since I_{out} is irrelevant to VDD by Eqn. (1) even if the power supply is fluttered.

2). threshold detector: The raw digital data signal is sliced by the Schmitt trigger circuit. Fig. 4 is the transfer curve of the Schmitt trigger [4]. The low switching voltage V_{SPL}=0.8V, and high switching voltage V_{SPH}=1.7V.

3). load driver: It is a buffer composed of two cascaded inverters to increase the signal driving capability.

Fig. 5 shows the equivalent circuit of the envelope detector, where the Schmitt trigger is replaced with a capacitor (C_L). Notably, PM103 is removed owing to that it is a start up circuit. Thus, NM101 and PM102 are, respectively, equal to a diode. The threshold voltage of NMOS transistors is V_{THN} (typically = 0.6V), and PMOS transistors is V_{THP} (typically = -0.8V). The logic level LOW of the ASK_SIG is -2.5∼2.5, and the logic level HIGH is -3.34∼3.34.

(A) Initialization: In the first cycle of the ASK_SIG, V_X=ASK_SIG-$V_{SD(PM101)}$.

- initially, $V_X < V_{THN}$: When ASK_SIG is varied from -2.5 to 2.5V for a coded "0" (or -3.34 to 3.34V for a coded "1"), NM101 and NM102 are cutoff ⇒ ENV_SIG=0.
- $V_X > V_{THN}$: NM101 and NN102 are saturated ⇒ ENV_SIG=$V_{DS(NM102)}$+I_e·R_S. Hence, the voltage of C_L (V_{C_L}) is not zero.
- again, $V_X < V_{THN}$: When ASK_SIG from 2.5 to -2.5V (or 3.34 to -3.34V), NM101 and NM102 are cutoff ⇒ ENV_SIG=V_{C_L}.

(B) In the rest of the ASK_SIG cycles:

- when ASK_SIG-ENV_SIG>V_{THP} and $V_X < V_{THN}$: PM101 and PM102 are in the saturation region, while NM101 and NM102 are cutoff. ⇒ The capacitor C_L is to be charged.
- when ASK_SIG-ENV_SIG>V_{THP} and $V_X > V_{THN}$: PM101, PM102, NM101, and NM102 are all in the saturation region. ⇒ ENV_SIG=$V_{DS(NM102)}$+I_e·R_S.
- when ASK_SIG-ENV_SIG<V_{THP} and $V_X < V_{THN}$: PM101, PM102, NM101, and NM102 are all cutoff ⇒ ENV_SIG=V_{C_L}=0.36V (when ASK_SIG is "0"), ENV_SIG=V_{C_L}=0.95V (when ASK_SIG is "1").

2.2. Power recovery circuit

The power of the core circuit is generated by the induced RF signal. The voltage swing of the induced signal is as high as ±24 V. Therefore, the signal must be rectified and regulated before it is delivered to the chip.

2.2.1. On-chip power regulator

The implanted device design must be aimed at reducing the circuit area and power. Hence, the number of passive elements must be as few as possible. The LDO (low dropout) voltage regulator circuit, as shown in Fig. 6, is composed of 3 sub-circuits [4], [9], [10].

1). start-up: The startup circuit is required to prevent the self-biased circuit from the zero current state. After the bandgap circuit reaches a stable operating point, the start-up circuit stops sinking current and presents a high impedance.

2). bandgap: It is a bandgap design with substrate PNP BJT technique [4]. The voltage output is simulated to be 1.18V, which is close to the expected 1.13V.
VREF=$(l \cdot n \cdot \ln K) \cdot nV_T \cdot \ln \frac{I}{K \cdot I_S}$=1.13V,
where l=11.628 is a factor for temperature coefficient, n=1 is the emission coefficient, K=5 is the multiple of diode emitter area (Fig. 6), V_T=0.026V, $I = 7.625\mu$A, I_S is the saturation current= 2.95×10^{-17}A in TSMC 0.35 μm 2P4M CMOS process.

3). error amplifier and pass element: The one-stage high-gain differential amplifier increases the operation bandwidth, lock time, and PSRR (power supply ripple rejection). When the aspect ratio of the pass element PM211 increases, not only it decreases the dropout voltage, but also increases the driving capability.

3. SIMULATION AND IMPLEMENTATION

The chip is designed by using TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 2P4M CMOS process. The layout of the ASK demodulator is shown in Fig. 7. Fig. 8 is the worst-case post-layout simulation given the SS model, and 36^{o}C. The characteristics of ASK the demodulator is tabulated in Table 1.

Table 1. Characteristics of ASK demodulator

freq. of the input	data rate: 10 Kbps, carrier freq.: 2 MHz
voltage level of the input	logic low level: 2.4∼2.6 V, logic high level: 3.2∼3.4 V
freq. of the demodulator output	20 KHz, duty cycle: 50.1∼50.6%
logic level of the demodulator output	logic low level: 0 V, logic high level: 3 V
power consumption	10.234 mW (at 2 MHz)¶
¶:the load at the O/P of ASK demodulator is 10pF and 1KΩ.	

The layout of voltage regulator is shown in Fig. 9. Fig. 10 is the worst-case post-layout simulation given SS model, and 36^{o}C, with input voltage varying from 4 to 5 V. The characteristics of voltage regulator is listed in Table 2. Fig. 11 shows the output voltage vs. temperature.

Table 2. Characteristics of voltage regulator

input voltage	4∼5 V, 0∼3MHz
output voltage	3.31 V±0.12% (36∼41^{o}C)
power consumption	23.9 mW (at 2 MHz)$^{\mathcal{L}}$

$^{\mathcal{L}}$:the load at the O/P of ASK demodulator is 10pF and 1KΩ.

The comparison of the proposed ASK demodulator with several prior works is summarized in Table 3. It shows that our design is the only one without using any capacitor.

Table 3. Comparison with prior ASK demodulators

Design	capacitor	MOS #
Liu's [6]	10 pF	14
Barú's [7]	10 pF	13
Yu's [8]	3 capacitors	13
Ours	0	16

Note: A 10 pF capacitor occupies roughly 0.01197 mm^2 in the 0.35 μm 2P4M CMOS process.

4. CONCLUSION

A small-area solution for an implantable ASK demodulator and a stable 3.3 V on-chip voltage regulator design are present in this work. The MOS count and the capacitor size are clearly analyzed. The post-layout simulation results turn out to be very appealing.

5. REFERENCES

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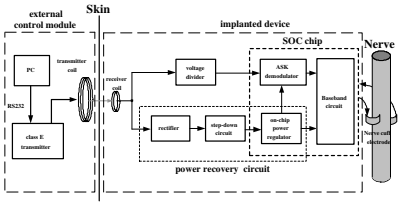

Fig. 1. Wireless neural stimulating system

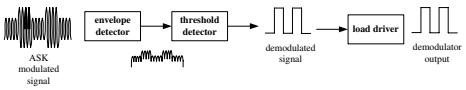

Fig. 2. The data flow of ASK demodulator

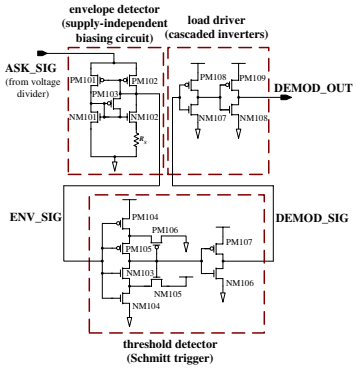

Fig. 3. Schematic diagram of the C-less ASK demodulator

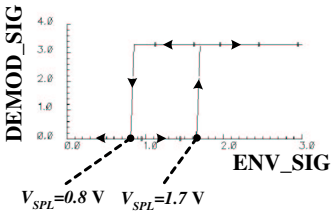

Fig. 4. Transfer characteristic curve

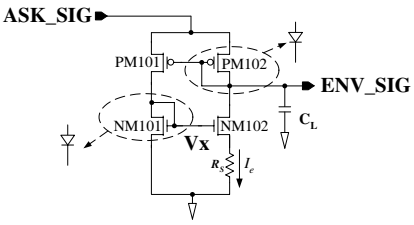

Fig. 5. ASK demodulator equivalent circuit

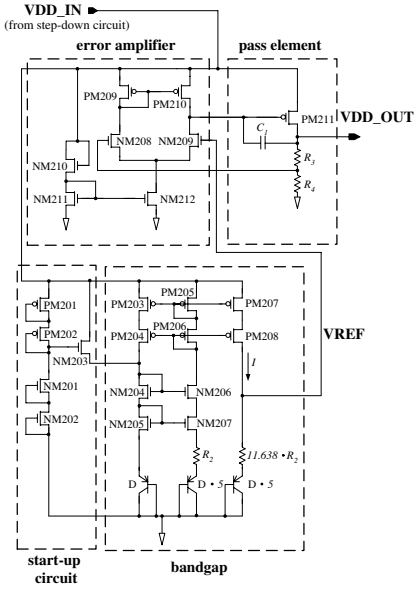

Fig. 6. Schematic diagram of the power regulator

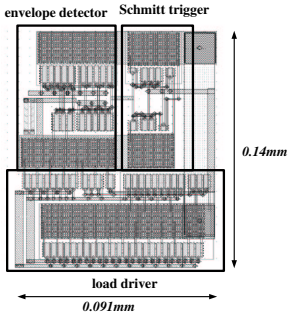

Fig. 7. Layout of C-less ASK demodulator

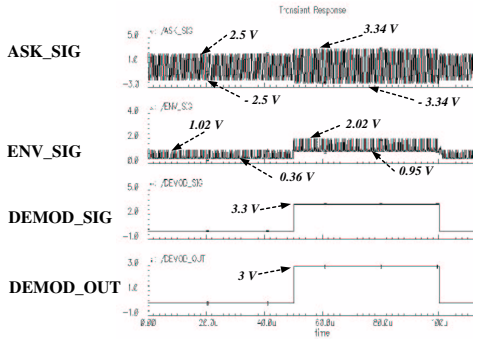

Fig. 8. Post-layout simulation result of ASK demodulator (SS, 36^{o}C)

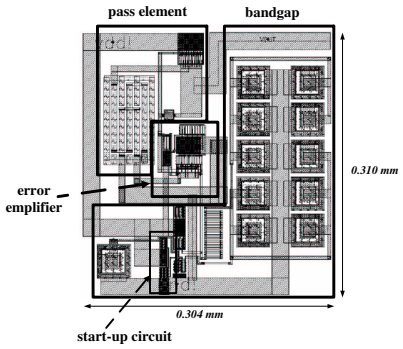

Fig. 9. Layout of power regulator

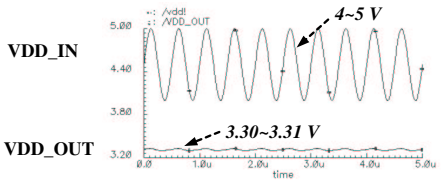

Fig. 10. Post-layout simulation result of power regulator (SS, 36^{o}C)

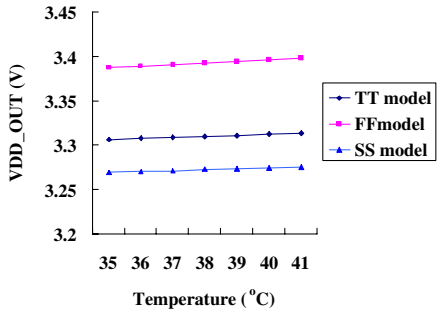

Fig. 11. Regulator output voltage vs. temperature