BASEBAND DESIGN OF A WIRELESS TRANSCEIVER FOR IMPLANTABLE NEURAL INTERFACE[§]

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ABSTRACT

An implantable SOC-based neural interfacing baseband dsign including controllable stimulators, and telemetry for data and power transmission is proposed. The micro-stimulator consists of multi-channel addressable current-source stimulators. The implanted device can be powered by transcutaneous magnetic coupling, using an external transmitter coil to power and communicate with implanted device. It can avoid the risk of causing infection and the problem of limited battery life. The SOC-based implantable system will be compatible to several prior neuronics assemblies. The neural interface SOC implementation is aimed at the control and monitor of the neural-interfaces which might be applied to the area of neural prosthetics or orthotics which replace or restore function lost due to damage to nerve systems.

Keywords : implantable, neural interface, SOC, wireless, DAC, baseband

1. INTRODUCTION

Traditional medical treatment has been drastically influenced by the advance of modern sciences and technologies. One of the astonishing medicare tools is the implantable micro-electrical stimulators thanks to the deeply miniaturized silicon technology. The implantable micro-electrical stimulators as well as the entire system are widely used in the treatment of the ladder leakage control [11], interrupt of pains, shaking syndromes of Parkinson's disease, muscle nerve stimulation, and Cochlear implants [4].

The electrical stimulator techniques are expected to be intensively used in the nerve systems where the electronic signals may be invoked to connect broken nerves, i.e., neural prostheses. The proposed design is intensively focused on an SOC-based system which leads to the restoration of functional movements of paralyzed extremities, e.g., paraplegia, quadriplegia, etc. Both the stimulative and sensory functions, therefore, have to be considered simultaneously. Paralysis patients might have chances to re-gain the sensing capability by the transmission of these electronic signals between their brains and muscle nerves. The proposed implantable SOC-based baseband design includes controllable constant-current stimulators, and telemetry for data and power transmission. The micro-stimulator consists of multi-channel addressable current-source stimulators. The implanted device can be powered by transcutaneous magnetic coupling, using an external transmitter coil to power and communicate with implanted device. It can avoid the risk of causing infection and the problem of limited battery life. The SOC-based implantable system will be compatible to several prior neuronics assemblies, including multi-shank probes [9], PEAs (planar electrode array) [5], regeneration-typed microelectrodes [6], and particularly injected micromodular BIONs (BIOnic Neurons) stimulators [7]. Besides the SOC design methodology which is required to carry out the core chip, both the micro-electronic packaging method (e.g, SMT, SiP and flip-chip packaging) and the bio-compatible materials (e.g, polyimide, or hermetic capsule) [5] are needed to fabricate the final prototype of the implantable SOC-based device. Thanks to the highly advanced semiconductor process and IC design, the size of the implanted SOC device is expected to far smaller than that of all of the prior electrical stimulators, including capsuled BIONs, cardiac pacemakers, and cochlear implants.

2. BASEBAND DESIGN OF A WIRELESS NEURAL INTERFACE

We propose an SOC (system-on-chip) chip to carry out the mission utilizing wireless and non-penetrating transmission to accept external instructions and execute required stimulations. The infrastructure of the entire electrical micro-stimulus system is given in Fig. 1.

2.1. System design

Power and Regulator: Due to the small size of receiver coil of the implanted device, the power trans-

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mission efficiency in the micro-devices is rather low. In order to supply enough power to implanted device, a high efficiency transmitter/amplifier must be used. Class-E power amplifiers show efficiency above 90% and suitable for this low coupling application. Power amplification is based on the class E amplifier and self-oscillating. The coupling of the coil influences the oscillation frequency. The resulting operation frequency offset yields an improved power transmission performance since the oscillation frequency tracks the absolute transmission efficiency maximum. Besides, a on-chip power regulator is required to supply a stable VDD output voltage to the internal digital core by regulating the power of on-chip coupling coils. Large batteries, thus, are not needed in such a system.

Safety : Since the SOC is targeted to be an implantable device, safety is naturally the first thing on the list. Manchester code is used for noise rejection reasons in the digital wireless communication.

Packet Format : The format of a valid packet is shown in Fig. 2. The first field composed of 5 bits is the START field. Five consecutive zero's trigger the stimulating function. The ADDRESS field comprises 3 bits to select which of the three channels are enabled and excited. The D bit determines the direction of the stimulating current. In other words, it is the sign of the current. The final MAG field is the amplitude of the stimulating current. These 5 bits are fed to the DAC associated with each channel.

RF Band Selection : Regarding the choice of carrier frequency band, we must consider that the electromagnetic wave is absorbed by the tissue of the body proportional to the frequency of electromagnetic wave. Besides, lower carrier frequencies will influence the transmission data rate. Thus, the general carrier frequency of implanted system is within ISM band, e.g., 1 to 20MHz.

Digital Modulation Scheme : The scheme in the data transmission comprises data coding and modulation. In order to reduce the size of implanted circuit and more accommodate to Class E transmitter, amplitude shift key (ASK) modulation is used in this device.

Bio-compatibility : The micro-stimulator send electrical pulses through the cuff electrodes to the nerve trunks as shown in Fig. 1. The magnitude as well the the pulse width required by neural trunks are given in Table 1 based on [1], [2], [3], [8], and [10]. The nerve is deemed as a 1 KΩ resistive load instead of a capacitive load, since the stimulus current is absorbed. In short, the strength of stimulus applied to a nerve can be controlled by an external device through the wireless transmission.

2.2. Schematic design

Referring to Fig. 3, the internal architecture of the implantable SOC chip is revealed. OSC is a ring-based 5 MHz clock generator, while the "BIST & Reset" comprises initialization and test settings of the system. The rest of the chip are described as follows.

Manchester Decoder : It receives the bit stream, Data_in, generated by the ASK demodulator (not shown) and executes the framing of valid packets, i.e., Data_out. Another function is to recover a 10 KHz clock, i.e. Clock_out for the following FSM and S/P (serial-to-parallel) converter.

FSM (finite state machine) : There are a total of 4 states to execute required stimulating functions as shown in Fig. 4.

S0 : When the decoded bit stream consists of consecutive 1's, the system simply pumps the voltage supplied by the built-in regulator in the BIST module. As soon as any 0 is detected, FSM moves into S1.

S1 : If five consecutive 0's are detected, FSM moves into S2. Otherwise, it goes back to S0.

S2 : This state decode the ADDRESS field : A_2, A_1, and A_0, respectively, enable DAC_2, DAC_1, and DAC_0 if the corresponding bit is set.

S3 : The D bit determines the current direction of the enabled DAC's. The amplitude of the stimulating current is controlled by $M_4, \ldots, M_0$. The schematic of the DAC is given in Fig. 5. The duration of the simulation is 3 recovered clock cycles.

DAC (digital-to-analog converter) : The DACs directly supply the driving currents to the associative nerves to serve as a stimulus. The amplitude of the current is determined by the MAG field of the incoming packet. The widths of the MOS's controlled by M_i's as well as the associative mirroring currents are binary-weighted. The D bit decides the direction of the overall current which indicates the sign of the stimulus.

3. SIMULATION AND IMPLEMENTATION

The chip is designed using TSMC 0.35 μm 1P4M CMOS process. The layout is shown in Fig. 6. Fig. 7 is the post-layout simulation by PowerMill. The channel 2 is selected to generating a 1.38 mA stimulating current lasting for 600 μs given the testing condition of TT model, 25^{o}C, VDD = 3.3 V.

Fig. 8 shown a consecutively 2-channel stimulating scenario with negative currents given a worst testing condition of SS model, 75°C, VDD = 3.0 V. The characteristics of the proposed design is tabulated in Table 2.

The comparison of the proposed design with several prior works is summarized in Table 3. Our design outperforms in almost every category. A performance measure is proposed as $E = \frac{I \times t}{\text{size} \times \text{power}}$ for a micro-stimulator, which is given in the last row of Table 3. The proposed design possesses the edge, since [9] is a penetrating device.

4. CONCLUSION

An SOC-based solution for implantable neural interfacing baseband design is present. By taking advantage of the advanced process technologies and EDA tools, the system-level integration is carried out to explore the feasibility of bio-chip designs. The post-layout simulation results verifies the correct functionality as well as the impressive performance.

5. REFERENCES

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	stimulating	blocking
freq.	10 - 100 Hz	1 - 2 KHz
current	1 - 3 mA	1 - 3 mA
pulse width	100 - 1000 μs	30 - 300 μs

Table 1: Bio-compatible requirements of electrical pulses

Technology	0.35 μm 1P4M CMOS
Max. bit rate	10 Kbps
Power	5 mW @ 5 MHz
Chip area	2.23×1.48 mm^2
Core area	1.50×0.74 mm^2
Max. O/P current	1.38 mA
#Channels	3

Table 2: Characteristics of the proposed design

	[7]	[9]	ours
size (mm^2)	16×2	4.4×2.5	2.23×1.48
output signal ($I \times t$)	30 mA × 514 μs	0.254 mA × 2 ms	1.38 mA × 600 μs
max. power	510 mW	80 μW	5 mW
#Channels	1	2	3
implantable	Yes	No	Yes
E	0.95	568.18	50.18

Table 3: Comparison with prior works

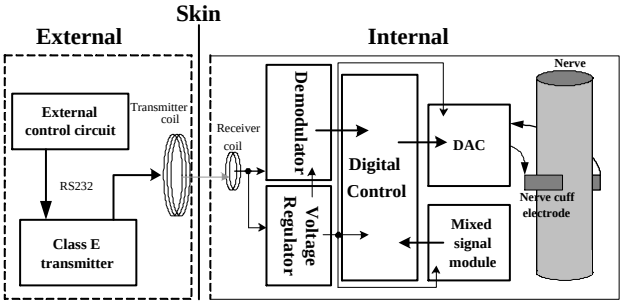

Figure 1: Wireless neural stimulating system

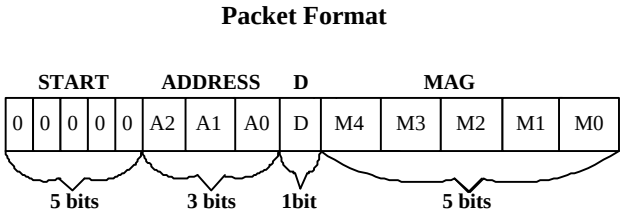

Figure 2: Packet format of data transmossion

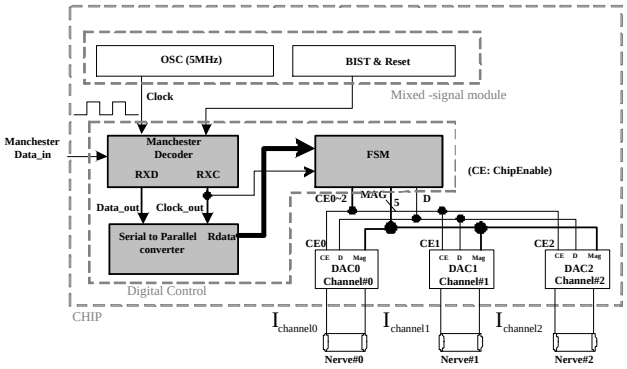

Figure 3: Baseband architecture of the implantable device)

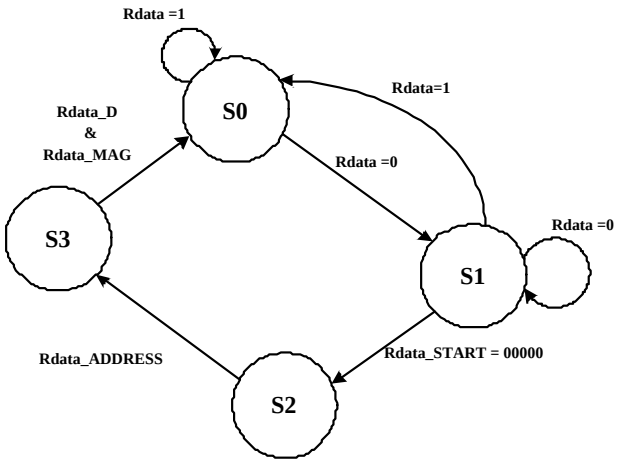

Figure 4: State transition of the FSM

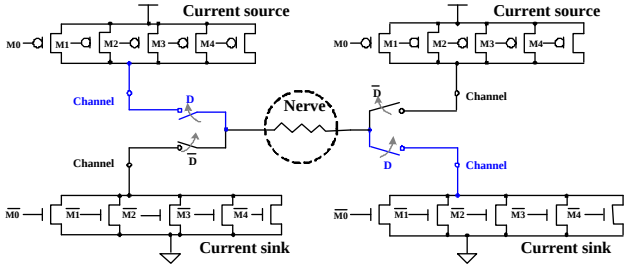

Figure 5: Interface of DAC and the nerve

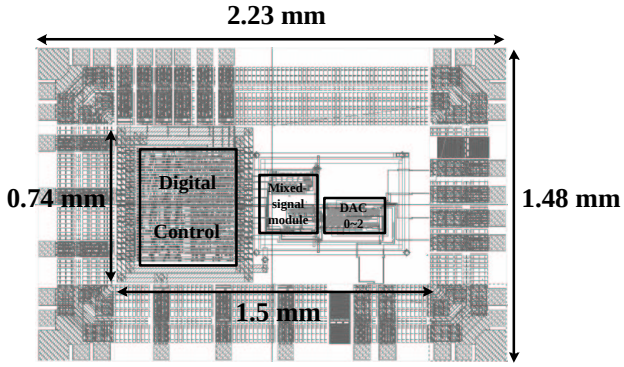

Figure 6: Layout of the proposed baseband

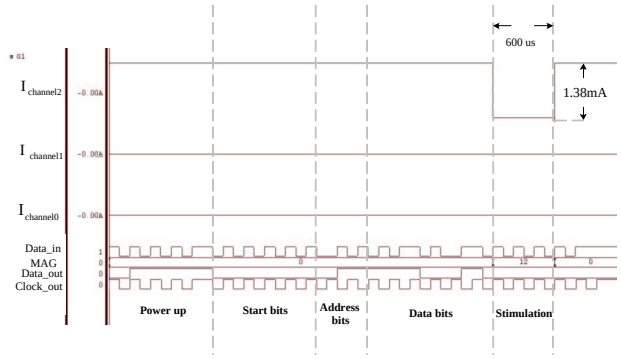

Figure 7: Post-layout simulation result at a normal condition

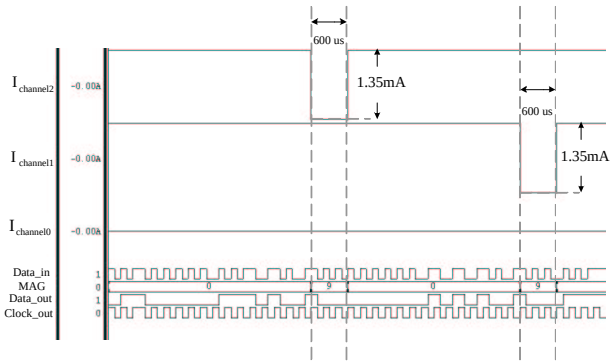

Figure 8: Post-layout simulation result at the worst condition