LOW-VARIATION 1.0 MHZ CLOCK GENERATOR WITH TEMPERATURE COMPENSATION BIAS[§]

Chua-Chin Wang† , Yih-Long, Tseng, Tzung-Je Lee, and Ron Hu¶

Department of Electrical Engineering
National Sun Yat-Sen University
Kaohsiung, Taiwan 80424
email : ccwang@ee.nsysu.edu.tw

ABSTRACT

This paper presents a simple and novel on-chip oscillator (OSC) with temperature compensation. The proposed OSC utilized a ring-like loop of which current sources are controlled by a temperature-insensitive bias. The bias contains neither BJT nor diode to constitute a traditional bandgap bias. Detailed analysis of the temperature-insensitive bias is derived to circumscribe the frequency variation to be less than 1.0% in the range of $0^o C$ to $100^o C$. The HSPICE simulation results verifies the prediction of our design. The maximum frequency of the proposed OSC is 1.45 MHz.

Keywords : temperature insensitive, ring oscillator, CMOS, start-up circuitry, bias

1. INTRODUCTION

Many consumer electronics products rely on precise clock sources, e.g., alarms, rice cookers, microwave ovens, etc. However, the on-chip clock sources built in the heat-generating products, e.g., cookers, will be drastically affected by the ambient temperature. The generated heat will be very likely to drift the clock edges if there is no compensation mechanism. Severe damages are possibly made to cause security problems. For instance, overheating or burning. Lots of work have been done to develop the design methods of the clock source circuitry, e.g., differential buffers and symmetric load [7], parallel OSC topology [5], and voltage regulator [6]. All of these prior works require complicated arrangement of components which, on the other way around, creates the difficulty of analysis. By contrast, we present a simple temperature-insensitive bias design to supply a nearly fixed voltage to a ring OSC. Detailed analysis of the bias is derived to approach a 1% frequency variation in a range of 0°C to 100°C.

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†the contact author, who is also the Chief Technology Officer of Asuka Semiconductor Inc., Taiwan

¶Dr. Ron Hu is the General Manager of Asuka Semiconductor Inc., Taiwan.

2. TEMPERATURE-INSENSITIVE CLOCK GENERATOR

The entire clock generator is shown in Fig. 1. The Bias Circuit block is responsible for providing a temperature-insensitive bias to the following Ring OSC.

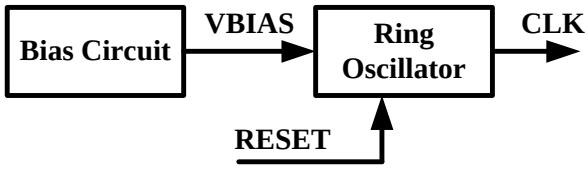

Figure 1: Architecture of the proposed VFC

2.1. Ring OSC

Referring to Fig. 2, PMi and NMi, $\forall i = 1 \ldots 5$, consist a 5-stage ring. A reset signal, RESET, controls NM7 via INV1. If RESET = low, the ring OSC is disabled. PM6 and NM6, INV2, and INV3 are deemed as a 3-stage inverting buffer to drive the CLK output. Thus, the clock frequency is as follows.

$$\begin{aligned} f_{CLK} &= \frac{1}{n(t_{PHL} + t_{PLH})}, \\ t_{PHL} &= R_N(C_{out} + C_{load}), \\ t_{PLH} &= R_P(C_{out} + C_{load}), \end{aligned} \tag{1}$$

where n is the stage count of the OSC, t_{PHL} is the propagation delay of high to low, t_{PLH} is the delay of low to high, and C_{out} and C_{load} denote the capacitance of the previous stage and the next one, respectively. Notably, R_N is the equivalent impedance of the NMOS in a single stage, while R_P is that of the PMOS. Notably, the equivalent impedance is controlled by the VBIAS applied to the gates of PM1 to PM5. Hence, as long as the VBIAS is table, the generated CLK will be considered as a reliable clock source.

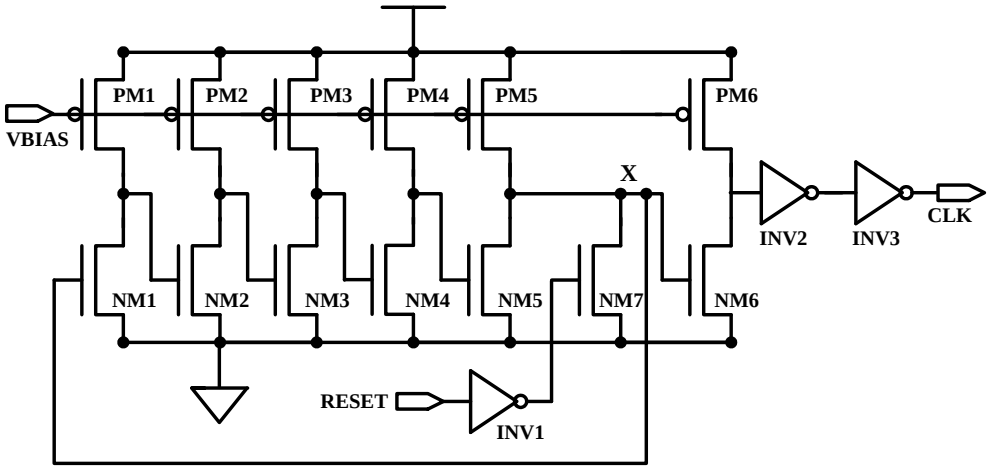

Figure 2: Schematic of the proposed VFC

2.2. Bias circuitry

A simple but temperature-insensitive bias circuit is shown in Fig. 3. Size ratio of PMb1 and PMb2 is 1:1, which consist of a current mirror, i.e., $I_1 = I_2$. The widths of NMb1 and NMb2 is set to be K:1. Notably, NMb3 is a startup device to avoid the entire bias circuit converging into a cutoff operation point at 0 V. The length of each of the mentioned MOS is set to be at least 3 times longer than the minimal feature size to avoid the channel length modulation effect [1].

The bias current, I_2, is found to be

$$I_2 = \frac{2(\sqrt{K}-1)^2}{K} \cdot \frac{1}{K_n^{'}(W/L)_{\mathrm{NMb2}} R_S^2}, \qquad (2)$$

where R_S is the resistor in Fig. 3, and $K_n^{'} = \mu_n \cdot C_{ox}$. The voltage drop between of the gate and the source of PMb1 is denoted by V_{GSP}. The current I_1 via PMb1 is also expressed to be

$$I_1 = \frac{1}{2} \cdot K_p^{'} \cdot (W/L)_{\mathrm{PMb1}} \cdot (V_{GSP} - V_{THP})^2, \qquad (3)$$

where $K_p^{'} = \mu_p \cdot C_{ox}$, and V_{THP} is the threshold voltage of PMOS. For the sake of clarity, the term $\frac{2(\sqrt{K}-1)^2}{K}$ is denoted by $Const$. Owing to the current mirror composed of PMb1 and PMb2, I_1 is identical to I_2. We can solve the VBIAS by equalizing Eqn. (2) and (3).

$$\begin{aligned} \mathrm{VBIAS} &= VDD - V_{THP} - \\ &\quad \sqrt{\frac{2 \cdot Const}{(W/L)_{\mathrm{NMb2}}(W/L)_{\mathrm{PMb1}}} \cdot \frac{1}{R_S^2 K_n^{'} K_p^{'}}} \\ &= VDD - V_{THP} - B \cdot \sqrt{\frac{1}{R_S^2 K_n^{'} K_p^{'}}} \qquad (4) \\ B &= \sqrt{\frac{2 \cdot Const}{(W/L)_{\mathrm{NMb2}}(W/L)_{\mathrm{PMb1}}}}, \qquad (5) \end{aligned}$$

where B is used to simplify the equation by grouping all of the temperature irrelevant terms. The rest of the terms, including R_s, V_{THP}, $K_p^{'}$, and $K_n^{'}$, are all sensitive to the temperature variation. We take the differential of VBIAS to temperature (T) based on Eqn. (4) as follows.

$$\begin{aligned} \frac{\partial \mathrm{VBIAS}}{\partial T} &= -B \cdot (-\frac{1}{2}) \cdot (R_S^2 K_n^{'} K_p^{'})^{-\frac{3}{2}} \cdot \frac{\partial R_S^2 K_n^{'} K_p^{'}}{\partial T} \\ &\quad - \frac{\partial V_{THP}}{\partial T} \\ &= A \cdot \left(2 R_S K_n^{'} K_p^{'} \frac{\partial R_S}{\partial T} + R_S^2 K_p^{'} \frac{\partial K_n^{'}}{\partial T} + \right. \\ &\quad \left. R_S^2 K_n^{'} \frac{\partial K_p^{'}}{\partial T} \right) - \frac{\partial V_{THP}}{\partial T} \qquad (6) \\ A &= -B \cdot (-\frac{1}{2}) \cdot (R_S^2 K_n^{'} K_p^{'})^{-\frac{3}{2}} \end{aligned}$$

2.3. Parameter tuning

Hence, there are a total of 4 terms to be tuned to make $\frac{\partial \mathrm{VBIAS}}{\partial T} = 0$, which are $\frac{\partial R_S}{\partial T}$, $\frac{\partial K_n^{'}}{\partial T}$, $\frac{\partial K_p^{'}}{\partial T}$, and $\frac{\partial V_{THP}}{\partial T}$. They are analyzed individually as follows.

$\frac{\partial V_{THP}}{\partial T}$: According to [1], $V_{THP}(T) = V_{THP}(T_0)[1 + TC_{VTHP}(T - T_0)]$, where TC_{VTHP} is the temperature coefficient of the PMOS threshold voltage, T and T_0 represents the current temperature and 25°C. TC_{VTHP} is a constant. It is -0.001824 V/°C in the TSMC 0.25 μm CMOS process that we utilize to carry out the proposed OSC.

$\frac{\partial K_n^{'}}{\partial T}$, $\frac{\partial K_p^{'}}{\partial T}$: Since $K^{'} = K^{'}(T_0) \cdot \left(\frac{T}{T_0}\right)^{-1.5}$, the following derivative is concluded.

$$\frac{\partial K^{'}}{\partial T} = K^{'}(T_0) \cdot (-1.5) \cdot \left(\frac{T^{-2.5}}{T_0^{-1.5}}\right). \qquad (7)$$

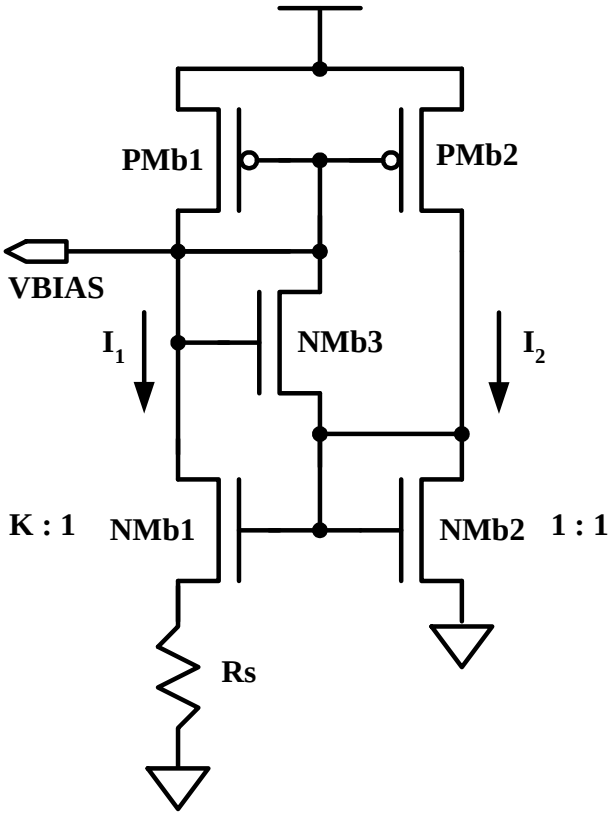

Figure 3: The temperature-insensitive bias circuit

It is found that $K_n^{'} = 2.03733 \times 10^{-4}$ V^{-1}, $K_p^{'} = 5.75385 \times 10^{-}$ V^{-1} at $T_0 = 25°$C. Thus, $\frac{\partial K_n^{'}}{\partial T}$ and $\frac{\partial K_p^{'}}{\partial T}$ can be derived easily.

$\frac{\partial R_S}{\partial T}$: The temperature coefficient of the polysilicon resistor in the mentioned process is 0.000867 $\Omega/°$C.

3. SIMULATION AND IMPLEMENTATION

In order to achieve the goal of less than 1% frequency variation of the OSC in [0°C, 100°C] for consumer electronics, the ring circuitry in Fig. 2 is simulated to discover that the linearity error, e.g., $\frac{\partial \text{VBIAS}}{\partial T}$, must be smaller than 0.0012 V/°C to fulfill the mentioned requirement.

The sizes of all of the transistors and the R_S are calculated according to the analysis in the previous section. The detailed size data are tabulated in Table 1. The layout of the proposed OSC is, thus, carried out in Fig. 4. Fig. 5 is the comparison of the pre-computed, simulated and ideal $\frac{\partial \text{VBIAS}}{\partial T}$. Notably, the difference between the pre-computed curve and the simulated curve are mainly resulted from the ignorance of the channel length modulation effect. Fig. 6 is the VBIAS post-layout simulation result in the range of [0°C, 100°C]. The frequency variation is worsened to be 5.86% because of the parasitics. However, Table 2 reveals that our design still outperforms the prior works in terms of the frequency variation.

Notably, though the precision of [2] is better than that of our design, the output frequency and the temperature range is too small for most of consumer products. Fig. 7 is the frequency spectra of our design at 0°C and 100°C, which show that there are at least 10 dB deficit between the target frequency and the 3rd harmonic tone.

	W/L
PM1 to PM5	72/11
NM1 to NM6	48/11
NM7	48/11
PMb1, PMb2	520/1
NMb1	90/1
NMb2	15/1
NMb3	225/0.6
R_S	810 Ω

Table 1: Detailed sizes of the proposed design

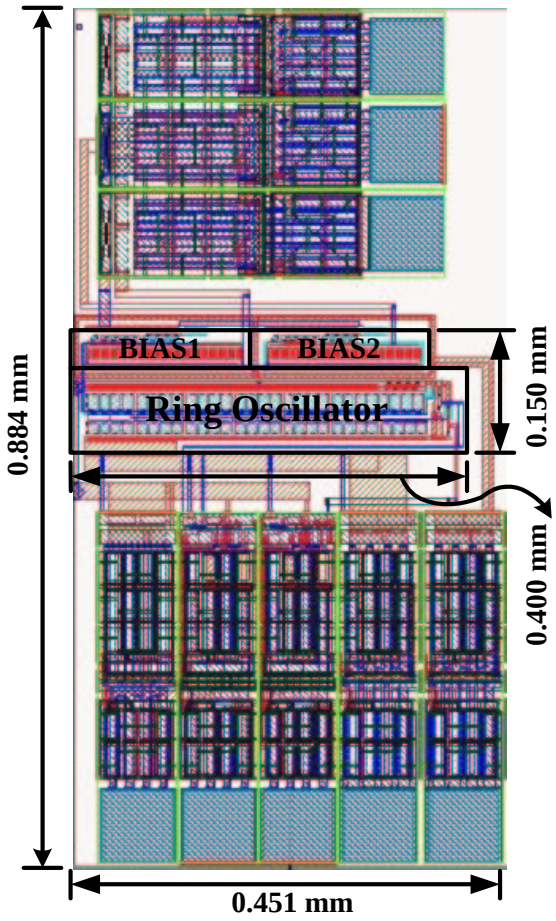

Figure 4: The layout of the proposed OSC

$\partial VBIAS/\partial T$

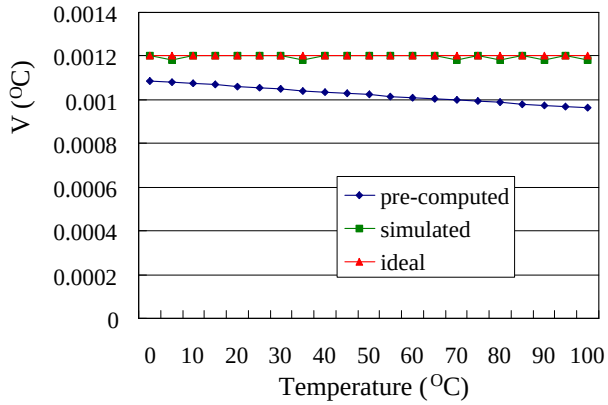

Figure 5: The comparison of the pre-computed, simulated and ideal $\frac{\partial VBIAS}{\partial T}$

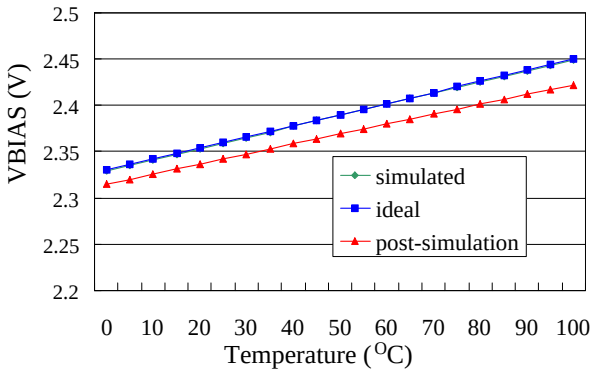

Figure 6: The VBIAS post-layout simulation result in the range of $[0°C, 100°C]$

4. CONCLUSION

We have proposed a temperature-insensitive OSC for consumer electronics in this paper. Not only the frequency variation and the output frequency are dramatically improved, the overall manufacturing cost is reduced by not using complicated bias generation circuitry. The accuracy of the chip is constrained be be less than 6 percent.

5. REFERENCES

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	[7]	[5]	[2]	ours
CMOS	0.6 μm	0.5 μm	0.5 μm	0.25 μm
max. f_{out}	0.68 MHz	380 MHz	0.1 MHz	1.45 MHz
temp. range	[35^{o}C, 115^{o}C]	[0^{o}C, 100^{o}C]	[0^{o}C, 70^{o}C]	[0^{o}C, 100^{o}C]
max. error	6.8%	14.8%	1.0%	5.86%
max. power	0.4 mW	14 mW	1.4 mW	14.9 mW
core area	0.0075 mm^2	N/A	0.4 mm^2	0.06 mm^2

Table 2: Comparison to prior designs

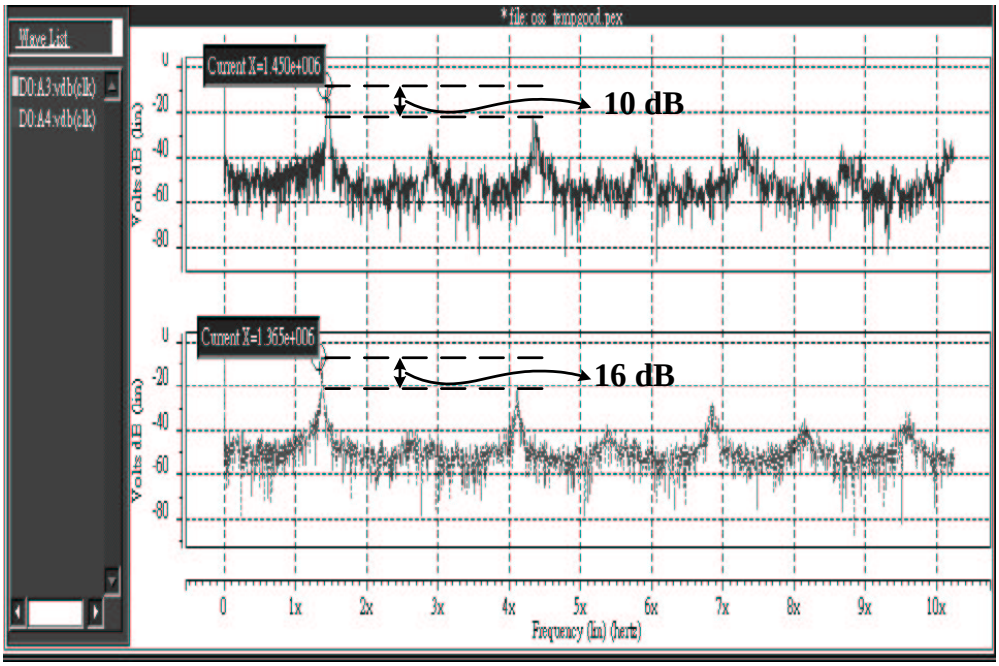

Figure 7: The frequency spectra of our design at 0^oC and 100^oC