58 MHZ/V SENSITIVITY CMOS VOLTAGE-TO-FREQUENCY CONVERTER USING A CURRENT-MODE VOLTAGE WINDOW COMPARATOR[§]

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ABSTRACT

A CMOS high-sensitivity voltage-to-frequency converter (VFC) is present in this work. The circuit is composed of one V-to-I converter, one current-controlled oscillator, and one voltage window comparator (VWC). The input voltage is converted into a current which in turn triggers the current-controlled oscillator composed of current mirrors and the current multipliers. The proposed VFC tracks the variations of the stored charge of a built-in capacitor. The voltage window comparator monitors the voltage of the capacitor to determine whether the output is pulled high or pulled down. The worst-case linear range of the output frequency of the proposed VFC is 0 to 55.40 MHz by simulations given a 0 to 0.9 V input range. The physical measurement of the proposed VFC shows a 0 to 52.95 MHz output frequency given a 0 to 0.9 V input range. The accuracy is less than 8.5% while the power dissipation is 0.218 mW.

Keywords : voltage window comparator, voltage-to-frequency converter, CMOS, voltage detection, current multiplier

1. INTRODUCTION

Lots of work have been done to develop the design methods of the circuits where oscillation parameters, e.g., amplitude, phase, frequency, or duty cycle in multivibrators, provide information on the value of passive or active elements [2]. There values might be functions of some other factors, e.g., mechanical pressure, magnetic field, or temperature. The variation of the oscillation needs to faithfully give the corresponding change of these factors. Hence, bandwidth, sensitivity, and linearity are the most important measures to judge the quality of these circuits. Besides, one of the measurement methodologies is to convert the physically estimated values into oscillations such that the correctness of the information is ensured owing to the fact that the oscillations are more noise immune. In this work, we present a high-bandwidth linear interfacing circuit which converts the sensed voltage into frequency. The frequency output is relatively noise resistant compared to other types of outputs, e.g., current or voltage. It meets the requirement of integration with other IPs (intellectual properties), e.g., uP or communication MAC (media access) circuitry. In contrast to the the bipolar or BiCMOS implementations [2], our proposed design is carried out by TSMC 0.25 μm 1P5M CMOS technology. It possesses the edges of low power, small area and high bandwidth. Although there were several prior CMOS-based converters, they either required an extra OSC [7], or additional timing control signals and many switched capacitors [6]. They became the overhead of the converter design. By contrast, our proposed converter is composed of one V-to-I converter, and one current-controlled oscillator which is driven by the voltage window comparator (VWC). The worst case range of the linear output frequency by the simulations is 0 to 55.40 MHz provided that the input voltage is 0 to 0.9 V. The physical measurement of the proposed VFC shows a 0 to 52.95 MHz output frequency given a 0 to 0.9 V input range.The accuracy is less than 8.5% while the power dissipation is 0.218 mW.

2. CMOS VOLTAGE-TO-FREQUENCY CONVERTER

The basic theory of voltage-to-frequency conversion (VFC) is to track the back-and-forth variations of a certain signal level in a pre-determined range. Thus, not only can it easily be carried out by low-cost CMOS technology, neither external oscillators nor internal PLLs are required in the design.

2.1. Architecture of the proposed VFC

Referring to Fig. 1, the building blocks of the proposed VFC are revealed. The input voltage, V_I, is converted into a current signal, I_I, by a V-to-I circuit. The I_I is fed to the Charge-Discharge circuit (CDC) to generate a reference voltage, V_{cap}, which is

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provided to the following voltage window comparator (VWC). The VWC is fed with two pre-defined reference voltages, VH (voltage high) and VL (voltage low), which determine the range of the voltage window. If $V_{cap} \in$ [VL, VH], the VWC sends the comparison result, VOUT = 1 (2.5 V), to charge a storage capacitor in the CDC. On the contrary, a VOUT = 0 (0 V), is delivered to discharge the capacitor. Hence, the VOUT is the generated oscillation signal.

2.2. Schematic design of VFC

Linearity is a must for a V-to-I conversion is our design. An OPA feeds a gate drive to an NMOS, NM21, in Fig. 2. The virtual ground is shorted to ground through a resistor, R_T. Because of the large input impedance of NM21, the current will be very small through NM21 and R_T. Notably, the length of all of the MOS transistors are set to be at least 5 times of the feature size to avoid any short-channel effect. The width of PM21 is M times of that of PM22 and PM23. Hence, the charging current for C_T will be $1/M$ of the current flowing through R_T and NM21.

In addition to the input voltage V_I, another input for resetting the entire VFC is required, i.e., V_{INIT}, which will be described later with the VWC circuitry. The charge-discharge operation besides the initialization stage is described as follows.

charging operation : The switch SW1 is shorted to node a1. Then, the storage capacitor, C_T, starts to be charged via saturated PM23.

discharging operation : As soon as the voltage of the C_T, V_{cap}, reaches VH, the output of WC, VOUT, is switched low to short-circuit SW1 to node b1. NM23 is tuned to be able to sink a current which is twice of the charging current provided by PM23. As soon as the V_{cap} is pulled down to VL, VOUT will be turned high to start another cycle of charging-and-discharging operations.

It is concluded that the oscillation frequency of VOUT is governed by the following equation,

$$f_{out} = \frac{V_I}{2 \cdot C_T \cdot R_T \cdot (\mathrm{VH} - \mathrm{VL}) \cdot M} \tag{1}$$

Notably, since all of the parameters, i.e., M, C_T, R_T, VH, and VL, can be pre-determined. Eqn. (1) is reduced to be $f_{out} = K \cdot V_I$, where K is a constant derived from all of the mentioned parameters.

2.3. All-MOS voltage-to-current converter (VCC)

As mentioned in the previous sections, a converter to convert the input voltage into a current linearly is required at the input stage of the entire design. We modify Fotouchi's design [4] to replace the foot-switch MOS with a small resistor since TSMC 1P5M CMOS process provides very accurate resistors made with polysilicon. Besides, a folded-cascode type of OPA [1] is used to drive NM31 in Fig. 3. Hence, the generated current is summarized to be

$$I_{conv} = \frac{V_I}{R_T} \tag{2}$$

The simulated V-I curve is given in Fig. 4. The linearity is very much ensured, which implies the sensitivity of the current in PM32 is 316.25 μA/V in the range of [0, 1.2] V.

2.4. All-MOS voltage window comparator (VWC)

Referring to Fig. 5, since SW1 is switched to set the VOUT= 2.5 V initially as we mentioned, SW2 is connected to a2 while SW3 is to a3 at this moment. The differential AMP formed by PM51, PM52, NM54, and NM55 is driven by VH and V_{cap} which is the voltage of C_T. The C_T is charged gradually. As soon as V_{cap} is larger than VH, most of the current supplied by VDD is switched to I_{52} such that I_{51} approaches nil to pull up the gate drive of the inverter composed of PM55 and NM58. The VOUT is thus switched low.

When VOUT is pulled low, SW2 is connected to b2 while SW3 is to b3. The differential AMP formed by PM53, PM54, NM56, and NM57 is driven by VL and V_{cap}. The C_T is discharged gradually. As soon as V_{cap} is smaller than VL, most of the current supplied by VDD is switched to I_{54} to apply a low gate drive of the inverter composed of PM55 and NM58. Certainly, I_{53} becomes nil at the same time. Hence, the VOUT is switched high.

The two differential AMPs execute the comparison of voltages alternatively such that the oscillations of VOUT are ensured. The purposes of adding an inverter at the output are flipping the state to generate the oscillation and increasing the driving current to the output. On top of that, the zero-delay hazard is also avoided.

It is noted that V_{INIT} in Fig. 5 is reset initially such that it is out of the range defined by VL and VH. Hence, the VOUT at the initialization is pulled high to 2.5 V.

3. PHYSICAL MEASUREMENT

The layout as well as the die photo of the physical VFC on silicon is shown in Fig. 6. The chip size is 440×460 μm^2, while the core size is 374.5×353.5 μm^2. The worst-case working range of the input voltage is 0 to 0.9 V, while the output frequency is 0 to 55.40 MHz. Tektronix TDS 680B oscilloscope, HP 8594E Spectrum Analyzer, and HP 1660CP Logic Analyzer are used to measure the performance of the proposed VFC. Fig. 7 and 8 are the measured outputs in the time domain and frequency domain, respectively, given 0.4 V input. The overall output frequency vs. input voltage measurement is summarized in Fig. 9, while Fig. 10 reveals the error in Fig. 9. The maximum error is less than 8.5%.

The overall characteristics of the proposed design by measurement is tabulated in Table 1. The measured sensitivity is derived to be $\frac{52.95}{0.9} = 58.83\,\mathrm{MHz/V}$. We also make a comparison of our design and several prior VFC designs in Table 2. It is obvious that our design outperforms the rest in the categories of the maximum output bandwidth, and sensitivity.

4. CONCLUSION

We have proposed a high-bandwidth VFC in this paper. Not only the sensitivity and the output frequency is dramatically improved, the overall manufacturing cost is reduced by not using BiCMOS, clock control circuitry, and many large capacitors. The accuracy of the chip is constrained be be less than 10 percent.

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	By Simulation	By Measurement
V_{in}	0 to 0.9 V	0 to 0.9 V
Temperature	-25^oC to 75^oC	-25^oC to 75^oC
Max. O/P freq	55.40 MHz	52.95 MHz
Error	$\leq$ 8.5%	$\leq$ 8.5%
Sensitivity	$\geq$ 58 MHz/V	$\geq$ 58 MHz/V
Power max. f_{out}	0.17533 mW	0.218 mW
Chip area	440×460 μm^2	440×460 μm^2

Table 1: Characteristics of the proposed VFC design

	ours	[2]	[7]	[6]
Tech.	CMOS	BiCMOS	CMOS	CMOS
f_{out}	52.95 MHz	100 KHz	N/A	100 KHz
V_{in}	0 to 0.9	0 to 6	0.1 to 10	0 to 10
Sens.	58 MHz/V	16 KHz/V	N/A	10 KHz/V

Table 2: Comparison to prior designs

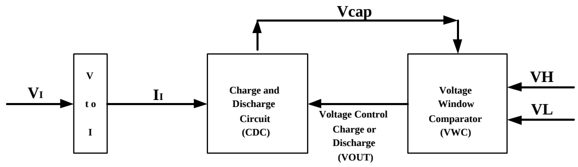

Figure 1: Architecture of the proposed VFC

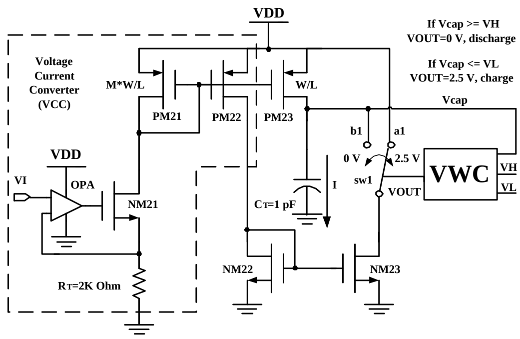

Figure 2: Schematic of the proposed VFC

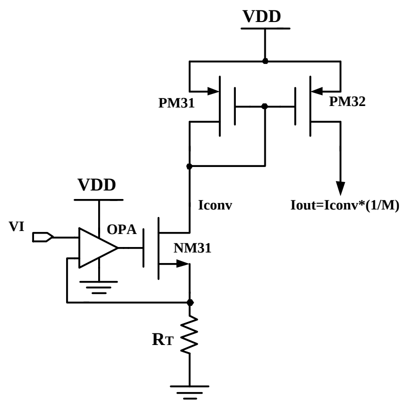

Figure 3: V-to-I converter (i.e. VCC in Fig. 2)

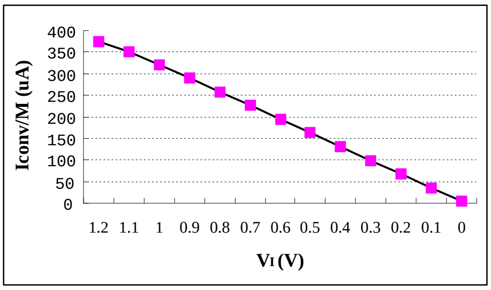

Figure 4: I_{conv} vs. V_I

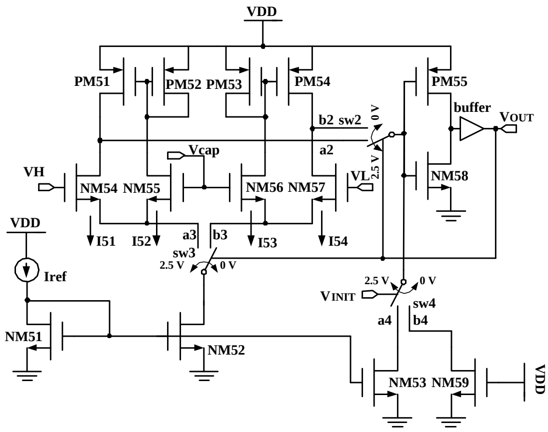

Figure 5: Detailed schematic of the VWC

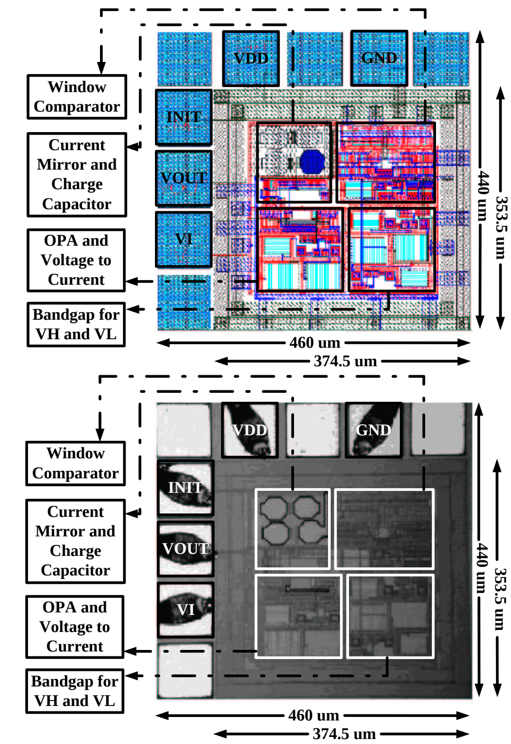

Figure 6: Die photo of the proposed VFC

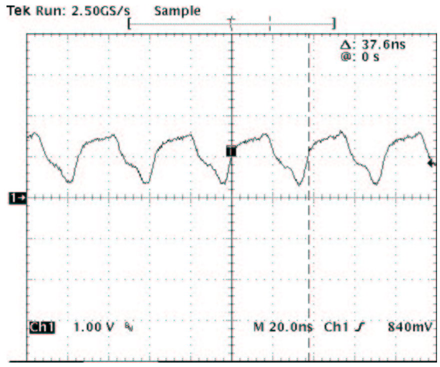

Figure 7: Output waveform given 0.4 V input

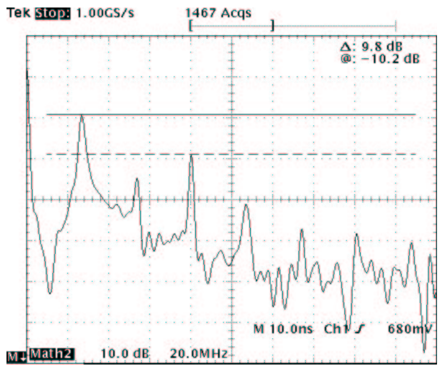

Figure 8: Output spectrum given 0.4 V input

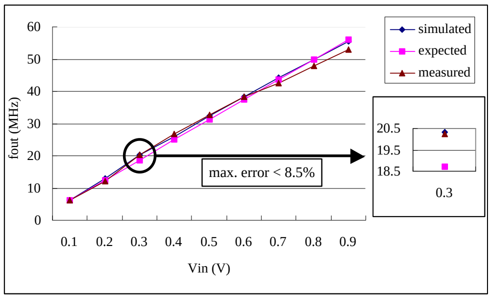

Figure 9: Comparison of the measured, the expected, and the simulated f_{out}

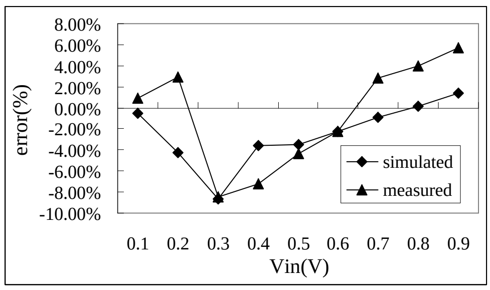

Figure 10: error (accuracy) of f_{out}