38.9 μW/MHZ SMALL-AREA DIGITAL I/O CELL[§]

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ABSTRACT

A novel low-power and small-area digital I/O cell is proposed in this work. The new I/O cell drastically reduces the I/O power consumption, which has been considered as the major power dissipation of the whole chip, with little sacrifice of speed or delay. Physical measurements of the proposed I/O cells show that the delays of the transmitter and the receiver are 1.1 ns and 1.8 ns, respectively. The largest power/bandwidth of the proposed design is 38.9 μW/MHz when transmitting.

1. INTRODUCTION

A bottle neck in the digital transmission of chips via longs wires on PCB is the I/O cells which are responsible for voltage level shifting and ESD protection [5]. Besides, long wires are huge R and C load to the chips. The I/O cells, namely I/O pads, are asked to supply sufficient current to drive these large loads. Hence, not only is the pad area large, but also the power consumption occupied a great portion of the overall power. Most of prior CMOS I/O cells utilized very large area to accommodate large driving transistors as well as large passive elements [2], [7]. The price to pay is more power dissipation. We have been told that voltage scaling is one of the most effective strategies to reduce power [1]. However, should the supply voltage of the chip is dropped, the switching speed of the I/O pads is reduced proportionally which in turn neutralize the high-speed performance of any CMOS digital core design. In this paper, we tend to propose a novel I/O cell design to resolve the dilemma. The output voltage swing in the transmitter of our new cell is reduced to about half of the supply voltage. In the mean time, the high-speed and high-throughput digital core design is not affected by using a feedback loop containing transistors with different threshold voltages. The power dissipation is also drastically reduced. The receiver of the proposed I/O cell, on the other way around, restores the signal level such that it can be faithfully decoded to be the original data. Neither reference bias nor passive element is required in the proposed design.

[§] This research was partially supported by National Science Council under grant NSC 91-2218-E-110-001 and 91-2622-E-110-004.

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2. LOW-POWER I/O CELL DESIGN

A typical I/O cell design in digital data transmission is shown in Fig. 1. The predriver, when enabled, supplies the gate drive to the driver composed a pair of huge PMOS and NMOS transistors to steer a large current to or from the long wire. This traditional design can not directly be voltage scaled so as to achieve the power saving by $P = f \cdot C \cdot V^2$, where f is the switching frequency, C is the load, and V is the supplied voltage. The reason is obvious : if the supplied voltage of the driver is shifted form VDD to $\frac{1}{2}$VDD, the drain current of M11 becomes

$$I_D = \frac{\beta}{2}(V_{SG} + V_{thp})^2 \left[1 + \lambda(V_{SD} - V_{SD,sat})\right] \quad (1)$$

where V_{SG} is the voltage drop between the source and the gate of M11, V_{SD} is that between the source and the drain of M11. The decrease of V_{SD} caused by the shrinkage of the supplied voltage results in the decrease of I_D. Thus, the driving capability as well as the speed is deteriorated.

Adding a reference $\frac{1}{2}$VDD bias to the driver pair might be considered as a good idea. Regardless of using a bandgap bias or a second voltage supply, the area penalty is highly unacceptable since the load is large. On top of this drawback, the reference $\frac{1}{2}$VDD bias usually has a poor driving capability which severely affects the supplied voltage of the driver pair. The consequence could be malfunction and large power dissipation.

2.1. Transmitter of the proposed I/O cell

Thanks to advanced processes provided by TSMC, transistors with various threshold voltages are feasible in 0.25 μm or better CMOS technology. The proposed I/O cell consists of a transmitter (TX) and a receiver (RX) which will be introduced in the following text.

Referring to Fig. 2 which is the proposed transmitter, Data and Enable are signals generated by the digital core. ESD is the electro-static discharging circuitry for the purpose of protection. The model of the pad as well as the bonding wire and package will be discussed in Section 3. The operation of the transmitter is described as follows.

T1). When Data is low and Enable is high, inverter INV1 turns on M23 and M24 which in turn pull down node C and A, respectively, to ground. Then, the low voltage at node A turns on M26 via INV0.

T2). As soon as Data turns high, a wide M26 turns on M21 right away. Node C, thus, will be charged to around 0.1 V very shortly which turns on the zero-V_{th} NMOS, M22. The voltage at node A then is boosted to VDD. Thus, M26 is off and M25 is turned on to ground node B which in turn shuts down M21. The charging operation to node C is then terminated. The final voltage level of node C after the mentioned procedure will be kept around $\frac{1}{2}\times$VDD.

Since neither reference bias nor passive element is used in the design, the transmitter size is extremely small. Notably, in order to avoid the racing problem which might occur in the procedure of shutting down M21. We have to ensure that M26 is turned off before M25 is on. Otherwise, a large DC current will be induced. The design of inverter INV0 is different from the rest of the inverters. The pulldown transistor in INV0 is a zero-V_{th} NMOS, as shown in Fig. 3, which provides a high sensitivity to the variation of the voltage at node A. Hence, the gate drive at M26 will be discharged very quickly.

The final voltage level at node C does not have to be very precisely a $\frac{1}{2}\times$VDD, which is the "high" of the output of the transmitter. It will drift due to the temperature, process variation, or loading. As long as it is in the range of 0.7 to 1.5 V for all process corners, it can be recovered correctly by the sophisticated receiver design which will be illustrated in the following section.

2.2. Receiver of the proposed I/O cell

The signal delivered by the transmitter will be contaminated seriously by the noise and crosstalk of the transmission lines. The quality of the signal present at the receiver is expected to be poor. Referring to Fig. 4, the received signal appears at the gate of M43 via pad and ESD circuitry. The threshold voltage of M43 is chosen to be a medium $V_{th} \approx 0.4$V. (Note : The medium-V_{th} transistors are available in TSMC 0.25 μm 1P5M process and better processes.) The function of the receiver is described as follows.

R1). When the gate drive of M43 is low to turn off M43, node A is charged to VDD. Hence, the To_Chip signal is low. The weak feedback latch composed of INV2 and M42 stabilizes the signal to the digital core.

R2). If the gate drive of M43 turns high, M43 will be turned on to discharge node A. To_Chip signal, thus, is pulled high.

As long as the voltage of the gate drive of M43, which is the received signal via pad and ESD, is higher than the pre-determined 0.4 V, the voltage level of the signal sent to the internal digital core can be restored to VDD.

3. PHYSICAL MEASUREMENTS

The proposed I/O cell is implemented by TSMC 0.25 μm 1P5M CMOS technology to verify the performance. The bonding, packaging, and wiring model between the I/O pads is modeled in Fig. 5 [6]. The layout of the proposed I/O design is given in Fig. 6. The die photo of the proposed I/O cell as well as the serial adder circuit is shown in Fig. 7. Tektronix TDS 680B oscilloscope, HP 33120A Function Generator, Agilent 33250A, HP 54616C, and HP 1660CP Logic Analyzer are used to measure the performance of the proposed I/O cell. Fig. 8 and 9, respectively, demonstrate the measurement waveforms of the outputs of the transmitter and the receiver. Fig. 10 is the output of the serial adder of which the input is increasing from 000 to 111 monotonically. All of the functions are verified to be correct. The overall characteristics of the I/O cell is summarized in Table 1.

By given the same testing condition (namely, 25^oC, transmitter load = 10 pF, and receiver load = 1.0 pF), we have compared the performance of our proposed I/O cell with two prior designs in Table 2. Except that the delay is a little worse than that of LVDS I/O cells, our design outperforms in the power and area categories.

4. CONCLUSION

We propose a novel I/O cell design taking advantage of transistors with different threshold voltages to achieve low power and small area. Besides, the sacrifice in terms of delay is obscure. Thorough post-layout simulations and the physical measurements confirm the superiority of our design regarding power dissipation and area.

5. REFERENCES

[1] R. J. Baker, H. W. Li, and D. E. Boyce, "CMOS - circuit design, layout, and simulation," Reading: IEEE Press, 1998.

[2] A. Boni, A. Pierazzi, and D. Vecchi, "LVDS I/O interface for Gb/s-per-pin operation in 0.35-um

CMOS," *IEEE J. of Solid-State Circuits,* vol. 36, no. 4, pp. 706-711, Apr. 2001.

[3] M.-D. Ker, and C.-H. Chuang, "Stacked-NMOS triggered silicon-controlled rectifier for ESD protection in high/low-voltage-tolerant I/O interface," *IEEE Electron Device Letters,* vol. 23, no. 6, pp. 363-365, June 2002.

[4] M.-D. Ker, and C.-H. Chuang, "Electrostatic discharge protection design for mixed-voltage CMOS I/O Buffers," *IEEE Trans. on J. of Solid-State Circuits,* vol. 37, no. 8, pp. 1046-1055, Aug. 2002.

[5] M. M. Lee, "Secondary protection scheme for CMOS I/O buffers and core circuits and their ESD sensitivity," *1997 6th Inter. Physical & Failure Analysis of Integrated Circuits Symp.,* pp. 109 - 114, 1997.

[6] Philips Semiconductor Inc., "IBIS model of 74AHCT04," Version 1.3, Dec. 15, 2000.

[7] F. Wajsburt, K. Dioury, and F. Petrot, "Low power, process independent, full transistor controlled slew rate, PCI compliant I/O pads," *1997 21st International Conference on Microelectronics,* vol. 2, pp. 811-814, Sep. 1997.

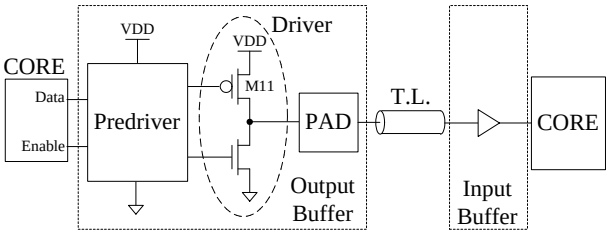

Figure 1: Traditional I/O cells

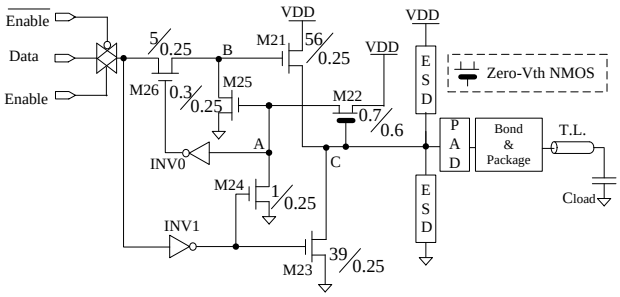

Figure 2: Trasmitter of the proposed I/O cell

	transmitter	receiver
input swing	2.5 V	0.8 V
power	7.78 mW	4.26 mW
	@ 200 MHz	@ 200 MHz
area	73.5×56.7 μm^2	80.3×79.3 μm^2
propagation delay	1.1 ns	1.8 ns
max. current	3.11 mA	1.70 mA
V_{IH}	> 1.3 V	> 0.52 V
V_{IL}	< 1.0 V	< 0.48 V
V_{OH}	[0.75, 1.25] V	[2.33, 2.9] V
V_{OL}	[-0.3, 0.2] V	[-0.5, 0.25] V

Table 1: Physical measurements of the proposed design

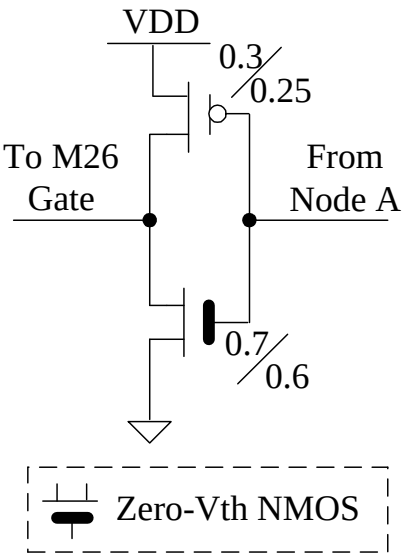

Figure 3: Schematic of INV0

	Power (μW/MHz)		Area (mm^2)		Delay (ns)	
	transmitter	receiver	transmitter	receiver	transmitter	receiver
TSMC I/O	215.88 (PCI66DGZ)		0.0188 (PCI66DGZ)		1.84	1.4
LVDS I/O [2]	43	33	0.175	0.081	0.8	1.4
Ours	38.9	21.3	0.00416745	0.0063678	1.1	1.8

Table 2: Comparison to prior designs (Note : PCI66DGZ is a bidirectional I/O cell)

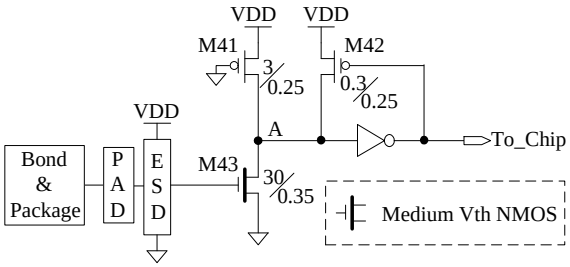

Figure 4: Receiver of the proposed I/O cell

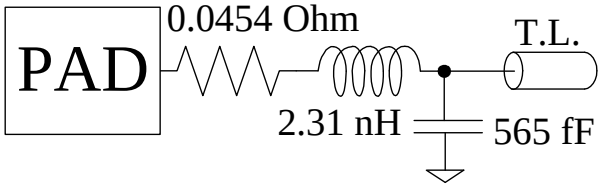

Figure 5: Wiring model between the pads

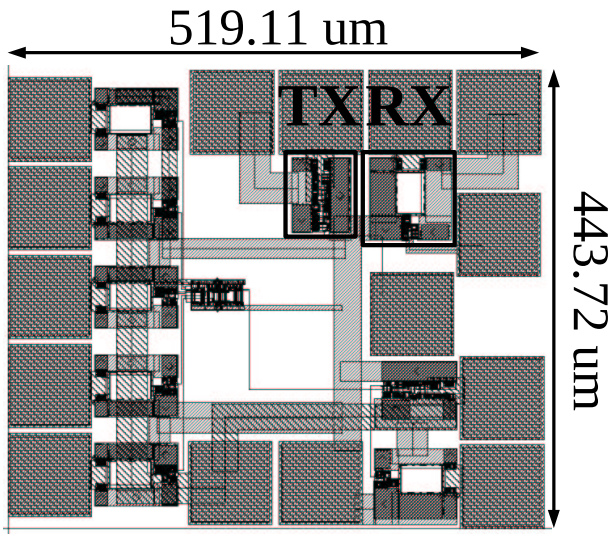

Figure 6: Layout of the proposed I/O cell

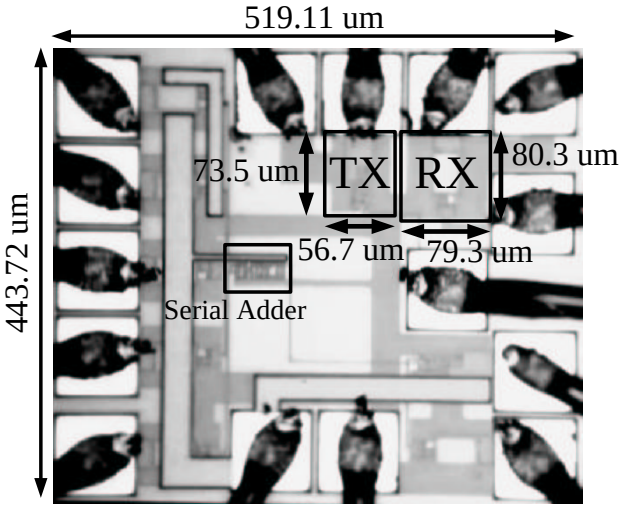

Figure 7: Die photo of the proposed I/O cell

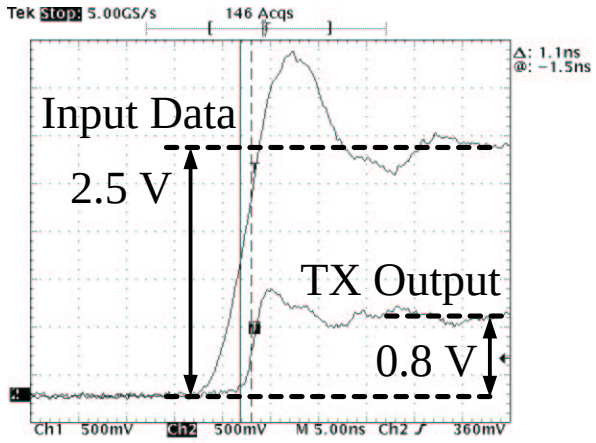

Figure 8: Measured output of the transmitter

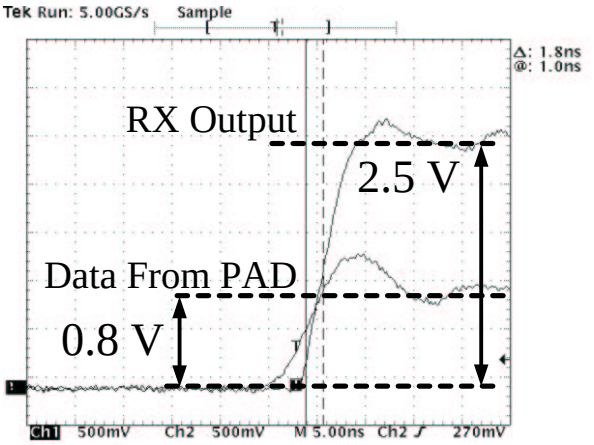

Figure 9: Measured output of the receiver

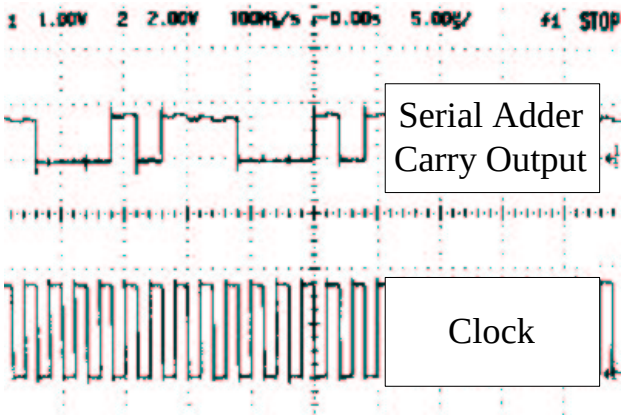

Figure 10: Measured output of the built-in serial adder