A 1.26 NS ACCESS TIME CURRENT-MODE SENSE AMPLIFIER DESIGN FOR SRAMS[§]

Chua-Chin Wang† , Yih-Long Tseng, Chih-Chen Li, and Ron Hu¶

Department of Electrical Engineering
National Sun Yat-Sen University
Kaohsiung, Taiwan 80424
email : ccwang@ee.nsysu.edu.tw

ABSTRACT

A CMOS high-speed current-mode sense amplifier (SA) design is proposed in this work. The SA is composed by cascading a current-mode sense amplifier and a voltage-mode sense amplifier. The small input impedance of the current-mode amplifier alleviates the loading effect on the bitlines of SRAM cells such that the sensing speed is enhanced. The voltage-mode amplifier is responsible for boosting the logic levels to full swing. The loop gain as well as the unit gain bandwidth (GBW) are analyzed and derived. The worst access time of the proposed design is found to be less than 1.26 ns with a 1 pF load on outputs. The power dissipation is merely 0.835 mW at 793 MHz.

Keywords : SRAM, sense amplifier, current-mode, feedback compensation, buffering

1. INTRODUCTION

The trend toward portable and small digital equipments or systems is rapidly booming [7], [1]. Microprocessor systems as well as the SOC (system-on-chip) demand large-capacity high-speed low-power on-chip memories. Particularly, embedded SRAMs and caches. Although 4-T SRAM, [10], [9], [5], [13], and 1-T SRAM, [3], have been announced to reduce the area cost, all of these designs require either extra circuitry to resolve the weak "0" (or weak "1") problem, poor driving and retention capability, or extra process to increase the capacitance at the data node. What even worse is some of the prior designs might need extra voltage sources, [5]. When it comes to the access time, the critical design is the sense amplifiers (SAs), not the cells [7]. Most of prior SAs are latch-based designs, which amplify the "voltage"difference between the bitlines. However, when the device size as well as the VDD shrinks, the voltage-mode SAs are prone to crosstalkings, substrate current variations and voltage modulations, which lead to the degradation of reliability [12]. In this paper, we propose a novel current-mode SA to resolve the mentioned difficult while preserve the speed of the accessing operations of memories. By taking advantage of the low input impedance of current sensing circuitry, the access time is drastically reduced. Besides, a voltage-mode amplifier is cascaded with the current-mode SA to restore the signal voltage swing such that the proposed design can be easily integrated with other parts of digital systems.

[§] This research was partially supported by National Science Council under grant NSC 91-2218-E-110-001 and 91-2622-E-110-004.

†the contact author, who is also the Chief Technology Officer of Asuka Semiconductor Inc., Taiwan

¶Dr. Ron Hu is the General Manager of Asuka Semiconductor Inc., Taiwan.

2. CURRENT-MODE SA DESIGN

The basic reason using a current-mode input stage in sensing circuitry is their small input impedance and cross-coupled feedback configuration. These features leads to the significant reductions in bitlines' sensing delays, voltage swings, crosstalkings, etc. [6]. The model of the bitlines coupled to the input of the SA is shown in Fig. 1. The propagation delay is derived to be

$$t_p \approx \frac{n^2RC}{2}\frac{r_{bo}+\frac{nR}{3}+r_{SA}}{r_{bo}+nR+r_{SA}} + r_{bo}r_{SA}nC\frac{1}{r_{bo}+nR+r_{SA}}, \quad (1)$$

where r_{bo} is the output impedance of the bitlines, r_{SA} is the input impedance of the SA, R and C are respectively the unit resistance and capacitance of the wire, and n is the number of the wire unit along the bitlines.

For voltage SA, $r_{SA} \to \infty$, while for current SA, $r_{SA} \to 0$. Hence, we conclude that

$$t_{pv} = t_p\,|_{r_{SA}=\infty} \approx \frac{n^2RC}{2}(1+\frac{2r_{bo}}{nR})$$
$$t_{pc} = t_p\,|_{r_{SA}=0} \approx \frac{n^2RC}{2}\frac{r_{bo}+\frac{nR}{3}}{r_{bo}+nR} \quad (2)$$

where t_{pv} and t_{pc} are respectively the sensing delay given by a voltage-mode SA and a current-mode SA. Since $nR << r_{bo}$, then we have a superiority of the current-mode SA, $t_{pc} << t_{pv}$.

2.1. Operation of the Proposed Design

A simple thought to boost the operating speed of accessing the stored data in memory cells is to fully take advantage of the low input impedance of a current-mode SA as described in Eqn. (2). Hence, a block diagram of an enhanced SA is shown in Fig. 2. The detailed schematic of Fig. 2 is illustrated in Fig. 3. PM21 - PM24 consists the precharge circuit in Fig. 3, while NM21, NM22, NM23, and NM24 are the current-mode amplifier stage of the proposed SA.

1). As soon as BLEQ turns low, BL and BLB are equally precharged to $\frac{1}{2}$ VDD.

2). Assume that the data kept in the memory cell after BLEQ turns high to start the accessing operation drive the current of BL higher than that of BLB. That is, $I_{NM24} > I_{NM21}$. Due to the current mirroring, NM23 sinks more current from BLB than NM22 from BL. A positive feedback loop is, thus, composed of two current mirror pairs. i.e., NM23 and NM24, NM21 and NM22.

3). NM21 will eventually turn into the triode region, while NM24 stays saturatedly. $V_{DS,NM24} \rightarrow 0$, and $V_{DS,NM21} \rightarrow VDD$.

4). The voltage difference between BL and BLB is magnified.

The voltage-mode AMP composed of NM25, NM26, PM25, and NM26, then reads the voltage difference between BL and BLB to generate the final Data O/P.

1). As soon as NM21 runs into the triode region and NM24 is saturated, NM21 has no charging path. The near-zero voltage at the gate drive of the inverter composed of NM26 and PM26 turns on PM26 to accelerate the pull-high of the drain voltage of NM21. Hence, it is also a positive feedback loop.

2). Similarly, NM25 and PM25 provide the same positive feedback loop function to NM24 when the current of BLB higher than that of BL.

3). PM27 and NM27 consist of a buffer to generate a regular square waveform.

2.2. Analysis of the Current-Mode AMP

Referring to Fig. 3, the input stage of the current-mode SA is composed of NM21, NM22, NM23, and NM24 of which the respective transconductance is gm_{NM21}, gm_{NM22}, gm_{NM23}, and gm_{NM24}.

DC analysis : The input impedance looking from the bitlines into the drain of NM21 and NM24 is merely two parallel GD-short transistor-based diodes, which lead to the following result,

$$\begin{aligned} R_{in} &\approx \frac{1}{gm_{NM24}} \text{ or } \frac{1}{gm_{NM21}} \\ &= \frac{1}{gm}, \quad \text{if } gm = gm_{NM2i}, \forall i = 1, \ldots 4 \end{aligned} \tag{3}$$

Thus, by adjusting the size of the 4 NMOS transistors, we can have a very low input impedance to overcome the slow response problem of prior voltage-mode latch-based SAs.

AC analysis : If we take the voltage-mode SA in Fig. 3 into consideration, the loop gain of the entire SA can be found. Assume the transconductance of PM26 is $L \cdot gm$ by widening its width to be L times of that of NM26. Similarly, the widths of NM22 and NM23 are increased to be K times of that of NM21 and NM24. The small signal model of Fig. 3 is summarized in Fig. 4. Hence, the loop gain A_{loop} is derived to be as follows,

$$A_{loop} = \left[\frac{\frac{(L-1)gm \cdot R_d}{1+\frac{gm \cdot R_d}{K}}}{1 + s\left(\frac{C_d \cdot R_d}{1+\frac{gm \cdot R_d}{K}}\right)} \right]^2, \tag{4}$$

where R_d is the load at the drain of the input stages, and C_d is the equivalent capacitance at the output node of the SA, including the Miller capacitance from C_{gd}, the diffusion capacitances, and the bitline capacitances C_{bl}. In this scenario, $C_d \approx C_{bl}$. The gain-bandwidth product of the proposed design is further concluded.

$$GBW_{ours} = \frac{(L-1) \cdot gm}{C_d} \tag{5}$$

The best part of the proposed design can be found in Eqn. (4). By manipulating the $gm \cdot R_d$ to be very small compared to 1 to take out the K factor, $A_{loop} \rightarrow \left(\frac{(L-1)gmR_d}{1+s \cdot C_d R_d}\right)^2$, which is clearly adjustable by tuning L. The GBW, however, will not be affected at all.

3. SIMULATION AND IMPLEMENTATION

TSMC 0.25μm 1P5M CMOS technology is used to carry out the proposed current-mode SA. A conventional 4-T SRAM cell is employed as the memory cell. C_{BL} and C_{load} are added to the bitlines and output pads to emulate the worst-case condition.

Fig. 5 shows the worst working condition at C_{load}=20.0 pF, C_{BL} = 3.0 pF, SS transistor model, 75^{0}C, VDD=2.25 V. The accessing delay is measured to be 3.2 ns. By contrast, Fig. 6 is the normal environment at C_{load}=20.0 pF, C_{BL} = 1.0 pF, TT transistor model, 25^{0}C, VDD=2.5 V. The accessing delay is reduced to 1.26 ns. The layout of the the proposed design is given in Fig. 7. The size of the proposed current-mode SA is 35.1×54.85 μm^2. The performance comparison of the proposed current-mode

SA and several prior works are tabulated in Table 1 as well as Fig. 8.

	access delay	power	# MOS
proposed	1.26 ns	0.835 mA	11
Uetake's [11]	7.20 ns	N/A	8
Huang's [4]	1.40 ns	0.210 mA	19
Sasaki's [8]	2.50 ns	N/A	22

Table 1: Comparison to prior designs (All designs are implemented by 0.25 μm CMOS @ C_{BL} = 1 pF.)

4. CONCLUSION

A novel current-mode SA is proposed in this work. The accessing delay is further reduced to merely 1.26 ns given 1.0 pF bitline loads. The low input impedance of the current-mode SA is fully taken advantage of to achieve high speed memory accessing. The GBW and the loop gain are both analyzed such that the AC response is well predictable and controllable.

5. REFERENCES

[1] R. J. Baker, H. W. Li, and D. E. Boyce, "CMOS - circuit design, layout, and simulation," Reading: IEEE Press, 1998.

[2] I. Fukushi, R. Sasagawa, M. Hamaminato, T. Izawa, and S. Kawashima, "A low-power SRAM using improved charge transfer sense amplifiers and a dual-V_{th} CMOS circuit scheme," *1998 Symp. on VLSI Circuits Digest of Technical Papers,* pp. 142-145, 1998.

[3] P. N. Glaskowsky, "MoSys explains 1T-SRAM technology," *Microprocessor Report,* vol. 13, no. 12, pp. 1-2, Sep. 1999. Reading: IEEE Press, 1998.

[4] H.-Y. Huang, and S.-L. Chen, "Self-isolated gain-enhanced sense amplifier," *2002 IEEE Asia-Pacific Conf. on ASIC,* pp. 57-60, 2002.

[5] H.-Y. Huang, and X.-Y. Su, "Low-power 2P2N SRAM with column hidden refresh," *2001 The 12th VLSI Design/CAD Symposium,* C3-8, pp. 64, Aug. 2001.

[6] T. P. Haraszti, "CMOS Memory Circuits," Reading: published by Kluwer Academic Publishers, 2000.

[7] B. Prince, "Semiconductor memories," Reading: John Wiley & Sons Ltd., 1991.

[8] K. Sasaki, K. Ishibashi, K. Ueda, K. Komiyaji, T. Yamanaka, N. Hashimoto, H. Toyoshima, F. Kojima, and A. Shimizu, "A 7-ns 140-mW 1-Mb CMOS SRAM with current sense amplifier," *IEEE J. Solid-State Circuits,* vol. 27, no. 11, pp. 1511-1518, Nov. 1992.

[9] K. Sato, K. Kenmizaki, S. Kubono, T. Mochizuki, H. Aoyagi, M. Kanamitsu, S. Kunito, H. Uchida, Y. Yasu, A, Ogishima, S. Sano, and H. Kawamoto, "A 4-Mb SRAM operating at 2.6±1 V with 3-μA data retention current," *IEEE J. Solid-State Circuits,* vol. 26, no. 11, pp. 1556-1562, Nov. 1991.

[10] K. Takeda, Y. Aimoto, N. Nakamura, H. Toyoshima, T. Iwasaki, K. Noda, K. Matsui, S. Itoh, S. Masuoka, T. Horiushi, A. Nakagawa, K. Shimogawa, and H. Takahashi, "A 16-Mb 400-MHz loadless CMOS four-transistor SRAM macro," *IEEE J. Solid-State Circuits,* vol. 35, no. 11, pp. 1631-1640, Nov. 2000.

[11] T. Uetake, Y. Maki, T. Nakadai, Y. Yoshida, M. Susuki, and R. Nanjo, "A 1.0 ns access 770 MHz 36 Kb SRAM macro," *1999 Symp. on VLSI Circuits,* pp. 109-110, 1999.

[12] B. Wicht, S. Paul, and D. Schmitt-Landsiedel, "Analysis and compensation of the bitline multiplexer in SRAM current sense amplifier," *IEEE J. Solid-State Circuits,* vol. 36, no. 11, pp. 1745-1755, Nov. 2001.

[13] C.-C. Wang, H.-Y. Leo, and R. Hu, "A 4-Kb 500-MHz 4-T CMOS SRAM using low-Vthn bitline drivers and high-Vthp latches," *The third 2002 IEEE Asia-PacificConference on ASICs (AP-ASIC2002),* pp. 49-52, Aug. 2002.

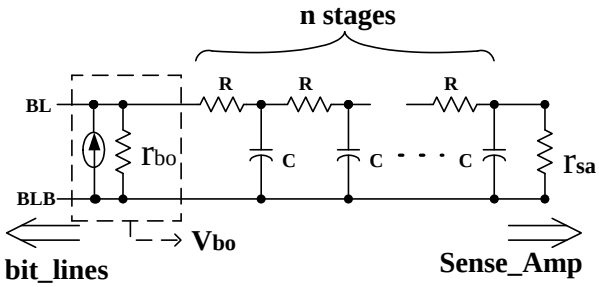

Figure 1: A bitline model for SA analysis

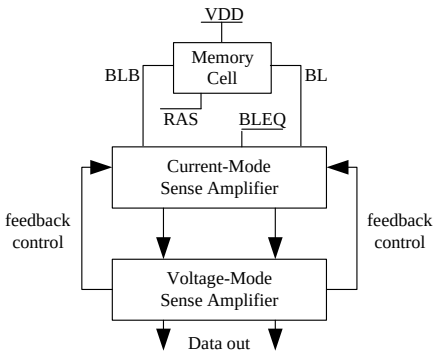

Figure 2: Proposed current-mode SA diagram

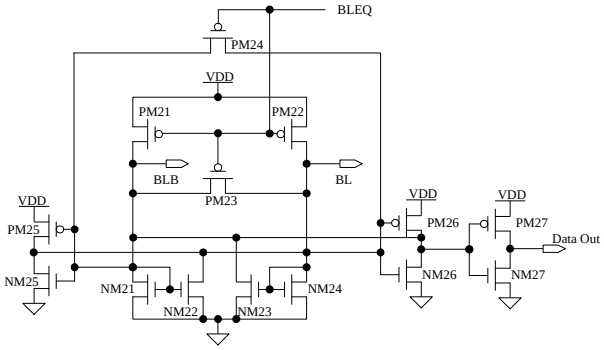

Figure 3: Proposed current-mode SA schematic

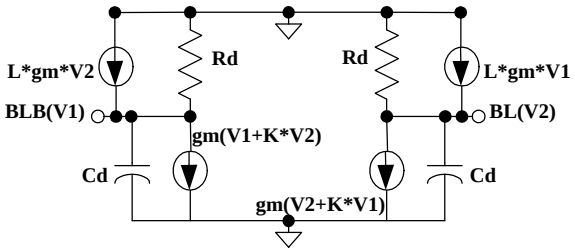

Figure 4: Small signal model

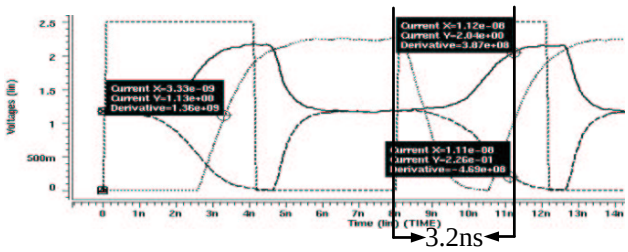

Figure 5: Performance at the worst-case condition (C_{load}=20.0 pF, C_{BL} = 3.0 pF, SS model, 75^{0}C, VDD=2.25 V)

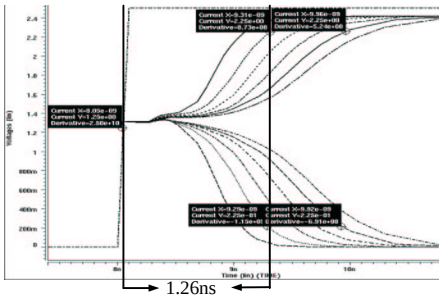

Figure 6: Performance at the normal condition (C_{load}=20.0 pF, C_{BL} = 1.0 pF, TT model, 25^{0}C, VDD=2.5 V)

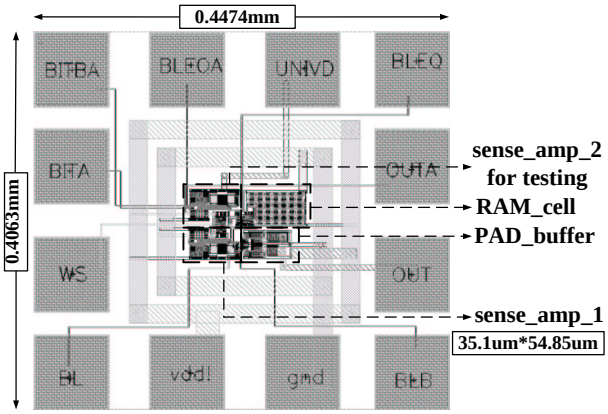

Figure 7: Layout of the current-mode SA

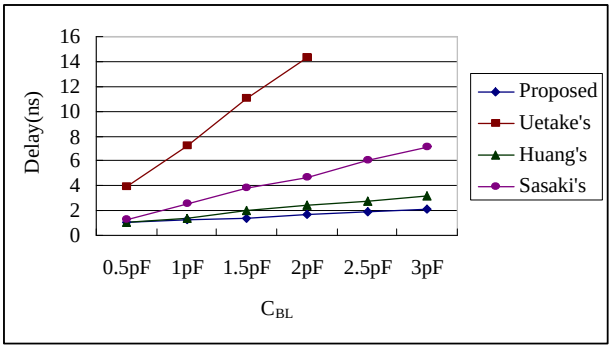

Figure 8: Comparison with the prior works